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EFFICIENT SCAN BASED TESTING FOR MEMORIES

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ABSTRACT

We all know that embedded systems have built in memory within the processor. But this memory should be tested by someone in order to store the data in a efficient manner. For this purpose we have built in self test repair (BISTR) technique, which is widely used to test repair embedded random access memories. This paper proposes a reconfigurable built in self test repair (ReBISTR) technique for test repair of RAMs with different sizes and redundancy organizations. An effective and efficient BIST algorithm has been proposed to allocate redundancies of defective RAMs. In this reconfigurable built in self test repair redundancy analysis is performed by using redundancy algorithm for various RAMs. When the RAMs are operated in normal mode, reconfigurable built in self repair technology is used to reduce the set up time. Due to the complexity of memory architecture, the possibilities of occurring manufacture defects are more. So memory testing is necessary, BISTR technique is cost effective but widely used as solution for memory testing. And the architecture are simulated in Xilinx ISE 14.7.

I. INTRODUCTION

Several commercial tools are nowadays available for the automatic insertion of the RAM BISTing. This paper presents the efforts and the results obtained in designing a proprietary BIST architecture to fulfill a peculiar industrial scenario.

In the target industrial scenario, the test engineer has to define the BIST strategy of a complex System-on-Chip including several SRAMs of different sizes (number of bits, number of words), access protocol (asynchronous, synchronous), and timing. Apart from the required design time, the mentioned task usually poses many issues, as the BIST area and routing overhead, the number of BIST controller to be used, the power budget constraints, and the diagnostic capabilities of the approach.

The BIST architecture proposed in this paper is characterized by fallowing:

- A single *BIST Processor*, able to perform the test of all (or a subset of) the SRAMS of the system. It is implemented as a micro-programmable machine executing elementary test primitives stored in a dedicated memory and implementing any required March algorithm

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- A *Wrapper* placed around each SRAM, including standard memory BIST blocks (i.e., an address generator, a background pattern generator, and a comparator), and an interface block designed to manage the communications between the SRAM and the BIST Processor independently from the memory access protocol;
- A minimal set of *communication signals* that allows the BIST Processor to execute and synchronize the test algorithm of all the memories under test;
- A scan chain connecting all the Wrappers in order to allow full diagnosis of the memories under test.

The proposed scheme presents several advantages. To begin with, it allows running concurrently the BIST of a set of SRAMs of different sizes, accessing protocols and timing. Moreover, the set of memories to be tested can be flexibly defined by the user, using either ad-hoc test primitives stored in the test program, or a dedicated scan chain configuring a status bit in each memory.

The use of a single BIST controller and a minimum set of communications signal allow minimizing the BIST area overhead and the routing around each SRAMs. Finally, implementing the BIST Processor as a micro programmable machine provides the test engineer with a flexible and reusable block, which can be used to manage the BIST of any number of memories of any size, and it is independent from the test algorithm.

II. The BIST Processor

As introduced in the previous section, the proposed scheme is based on a single BIST Processor used to test all the memories of the system. To increase flexibility, the BIST execution is based on a micro-programmable approach.

The *test algorithm* (a March Algorithm) is stored in a dedicated *mProgram-Memory*, coded using a set of *test primitives*. The mProgram-Memory can be either a ROM (in this way the test program is fixed at project time) or a programmable memory (in this way the appropriate test algorithm can be loaded into the memory at test time).

The BIST Processor reads one test primitive at a time, forwards it to all the Wrappers of the SRAMs under test using a synchronization signal, and waits for all the enabled SRAMs to complete the test primitive before sending the next one. When the test program is completed (all the test primitives have been applied), the BIST Processor reads the test results from each RAM. If a fault is detected, the faulty RAM can be located resorting to a set of diagnostic facilities.

III. The memory Wrappers

The Wrapper placed around each memory has to execute the test primitives received by the BIST Processor, independently of the memory access protocol. Moreover, the Wrapper is the only element in the architecture that must know the dimension and the access protocol of the memory it is placed around.

The Wrapper generates the correct test patterns and memory addresses required to execute the received test primitive, and evaluates the output results of a *read and verify* primitive.

The *Address Generator* (AG) is in charge of generating the correct address where the test pattern, provided by the *Background*

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Pattern Generator (BPG), has to be written or verified. The BPG can generate "1…1" and "0…0" test patterns as well as the background.

2. The correctness of the content of a memory cell is evaluated using a simple *comparator*. Two Status Bits are used to set the memory in *transparent* or in *test mode* (the *Mode Status Bit*) and to store the *test results* at the end of the BIST algorithm (the *Result Status Bit*), respectively. In order to load and read their content, the status bits of all the Wrappers are connected by two different scans chain, named *Normal_Test_Scan_Chain* (NTScan) and *Results_Scan_Chain* (Resscan).

Finally, each Wrapper includes an *Interface Block* able to receive the test primitives from the BIST Processor, and to produce the status signals needed by the BIST Processor to schedule the next test primitive to be executed.

In particular, the Interface Block generates the following information:

- End of Instruction (EOIN): asserted when the last received test primitive is thoroughly executed;
- End of Address Space (EOAD): asserted when the address generator reaches the end of its addressing space;
- End of Patterns (EOPG): asserted when the BPG has generated the whole set of background patterns;
- Read-and-Verify Result (GO): asserted when the content of the addressed memory cell matches the value expected by the test algorithm.

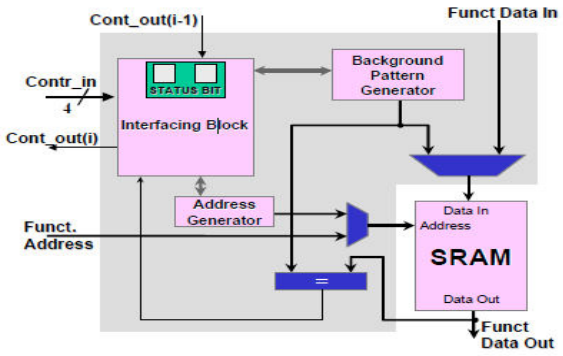

Fig1. Wrapper Structure

The BIST Processor receives the logic-AND of the signals generated by the memories under test. In this way, for example, the input EOAD signal of the BIST Processor switches to '1' only when all the EOAD signals of the memories under test have been set to '1', i.e., all the memory Wrappers reached the end of their address space.

Consequently, from the BIST Processor point of view, the system under test consists in a single memory, whose size is equal to the maximum size of the memories under test. To minimize the routing overhead, the signals exchanged between the BIST Processor and the memory Wrappers (command signals, synchronization signal, scan chain signals) are multiplexed and all the information items routed using only five signals (four command signals and one synchronization signal).

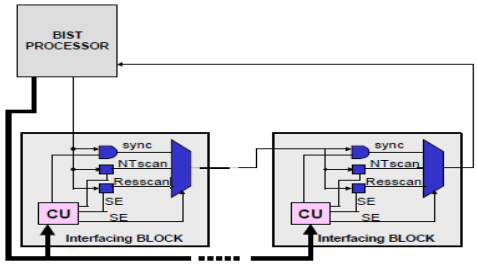

Fig 2. Multiplexing of command and Synchronization signals

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IV. RESULTS

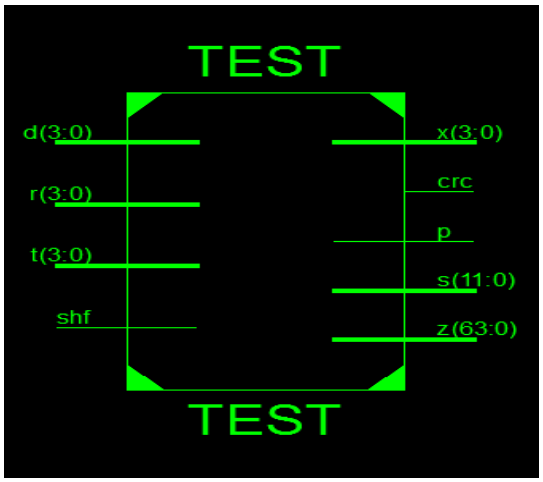

Fig.3. RTL Schematic.

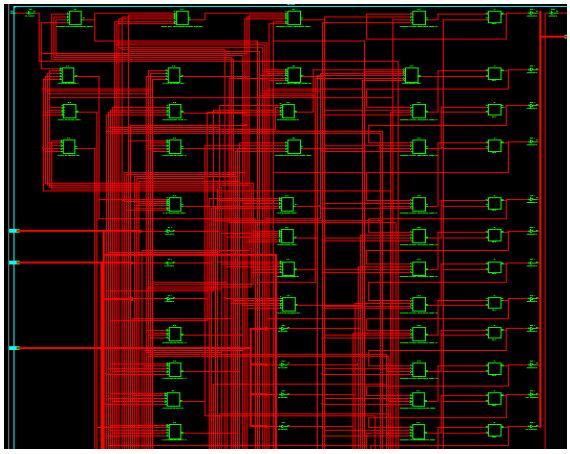

Fig.4. Technology Schematic.

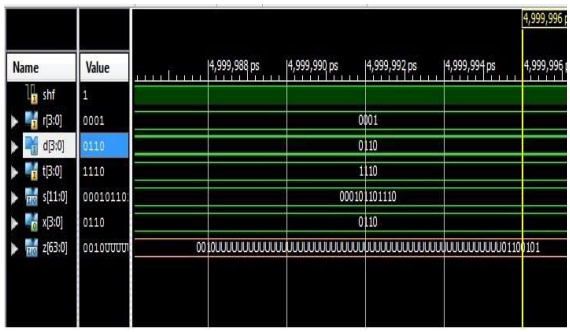

Fig.5. Output.

V. CONCLUSION

The proposed approach shows reducing generated test pattern transitions. By increasing the correlation between the successive bits, the transition is reduced. How the test patterns are generated for the applied seed vector shows in simulation results. This paper presents the implementation with regard to VHDL language. The Synthesizing and implementation of the code is carried out on the Xilinx - Project Navigator, ISE suite. The power reports show that the power consumption is less in the proposed architecture during. There is a chance to reduce the somewhat more power by doing modifications in the proposed architecture.

VI. REFERENSES

[1] Michał Filipek, Grzegorz Mrugalski, Senior Member, IEEE, Nilanjan Mukherjee, Senior Member, IEEE, Benoit NadeauDostie, Senior Member, IEEE, Janusz Rajski, Fellow, IEEE, Je˛drzej Solecki, and Jerzy Tyszer, Fellow, IEEE, —Low-Power Programmable PRPG With Test Compression Capabilities, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 23, No. 6, June 2015.

[2] A. S. Abu-Issa and S. F. Quigley, —Bit-swapping LFSR for low-power BIST, Electron. Lett., vol. 44, no. 6, pp. 401–402, Mar. 2008.

[3] C. Barnhart et al., —Extending OPMISR beyond 10x scan test efficiency, IEEE Design Test, vol. 19, no. 5, pp. 65–73, Sep./Oct. 2002.

[4] S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, —Low-power scan design using first-level supply gating, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 3, pp. 384–395, Mar. 2005.

[5] M. Chatterjee and D. K. Pradham, ―A novel pattern generator for near perfect fault-coverage, in Proc. 13th IEEE Very Large Scale Integr. (VTSI) Test Symp., Apr./May 1995, pp. 417–425.
[6] F. Corno, M. Rebaudengo, M. S. Reorda, G. Squillero, and M. Violante, ―Low power BIST via non-linear hybrid cellular automata, in Proc. 18th IEEE Very Large Scale Integr. (VTSI) Test Symp., May 2000, pp. 29–34. [7] D. Das and N. A. Touba, ―Reducing test data volume using external/LBIST hybrid test patterns, in Proc. Int. Test Conf. (ITC), 2000, pp. 115–122.

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