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RECURSIVE APPROACH TO THE DESIGN OF A PARALLEL SELF-TIMED ADDER

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ABSTRACT:

This brief presents a parallel single-rail self-timed adder. It is based on a recursive formulation for performing multi bit binary addition. The operation is parallel for those bits that do not need any carry chain propagation. Thus, the design attains logarithmic performance over random operand conditions without any special speedup circuitry or look-ahead schema. A practical implementation is provided along with a completion detection unit. The implementation is regular and does not have any practical limitations of high fanouts. A high fan-in gate is required though but this is unavoidable for asynchronous logic and is managed by connecting the transistors in parallel. Simulations have been performed using an industry standard toolkit that verify the practicality and superiority of the proposed approach over existing asynchronous adders.

1INTRODUCTION

Binary addition is the single most important operation that a processor performs. Most of the adders have been designed for synchronous circuits even though there is a strong interest in clockless/ asynchronous processors/circuits. Asynchronous circuits do not assume any quantization of time. Therefore, they hold great potential for logic design as they are free from several problems of clocked (synchronous) circuits. In principle, logic flow in asynchronous circuits is controlled by a request-acknowledgment handshaking protocol to establish a pipeline in the absence of clocks. Explicit handshaking blocks for small elements, such as bit adders, are expensive. Therefore, it is implicitly and efficiently managed using dual-rail carry propagation in adders. A valid dual-rail carry output also provides acknowledgment from a single-bit adder block. Thus, asynchronous adders are either based on full dual-rail encoding of all signals (more formally using null convention that uses symbolically correct logic instead of

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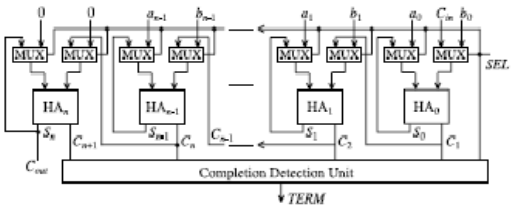
Boolean logic) or pipelined operation using single-rail data encoding and dual-rail carry representation for acknowledgments. While these constructs add robustness to circuit designs, they also introduce significant overhead to the average case performance benefits of asynchronous adders. Therefore, a more efficient alternative approach is worthy of consideration that can address these problems. This brief presents an asynchronous parallel self-timed adder (PASTA) using the algorithm originally proposed. The design of PASTA is regular and uses half-adders (HAs) along with multiplexers requiring minimal interconnections. Thus, it is suitable for VLSI implementation. independent carry chain blocks. The implementation in this brief is unique as it employs feedback through XOR logic gates to constitute a single-rail cyclic asynchronous sequential adder. Cyclic circuits can be more resource efficient than their acyclic counterparts. On the other hand, wave pipelining (or maximal rate pipelining) is a technique that can apply pipelined inputs before the outputs are stabilized. The proposed circuit manages automatic single-rail pipelining of the carry inputs separated by propagation and inertial delays of the gates in the circuit path. Thus, it is effectively a single rail wave-pipelined approach and quite different from conventional pipelined adders using dual-rail encoding to implicitly represent the pipelining of carry signals.

2 BACKGROUND

There are a myriad designs of binary adders and we focus here on asynchronous self-timed adders. Self-timed refers to logic circuits that depend on and/or engineer timing assumptions for the correct operation.



ig. 1. General block diagram of PASTA.

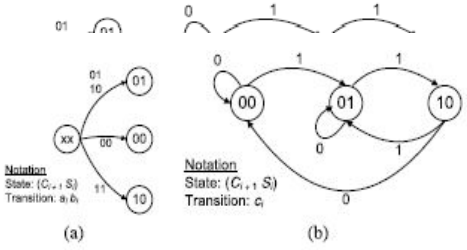


Fig. 2. State diagrams for PASTA. (a) Initial phase. (b) Iterative phase. Se

lf-timed adders have the potential to run faster averaged for dynamic data, as early completion sensing can avoid the need for the worst case bundled delay mechanism of synchronous circuits. They can be further classified as follows.

A. Pipelined Adders Using Single-Rail Data Encoding The asynchronous Req/Ack handshake can be used to enable the adder block as well as to establish the flow of carry

signals. In most of the cases, a dual-rail carry convention is used for internal bitwise flow of carry outputs. These dual-rail signals can represent more than two logic values (invalid, 0, 1), and therefore can be used to generate bit-level acknowledgment when a bit operation is completed. Final completion is sensed when all bit Ack signals are received (high). The carry-completion sensing adder is an example of a pipelined adder , which uses full adder (FA) functional blocks adapted for dual-rail carry. On the other hand, a speculative completion adder is proposed in. It uses so-called abort logic and early completion to select the proper completion response from a number of fixed delay lines. However, the abort logic implementation is expensive due to high fan-in requirements.

B. Delay Insensitive Adders Using Dual-Rail Encoding Delay insensitive (DI) adders are asynchronous adders that assert bundling constraints or DI operations. Therefore, they can correctly operate in presence of bounded but unknown gate and wire delays. There are many variants of DI adders, such as DI ripple carry adder (DIRCA) and DI carry look-ahead adder (DICLA). DI adders use dual-rail encoding and are assumed to increase complexity. Though dual-rail encoding doubles the wire complexity, they can still be used to produce circuits nearly as efficient as that of the single-rail variants using dynamic logic or nMOS only designs. An example 40 transistors per bit DIRCA adder is presented in while the conventional CMOS RCA uses 28 transistors. Similar to CLA, the DICLA defines carry propagate, generate, and kill equations in terms of dual-rail encoding. They do not connect the carry signals in a chain but rather organize them in a hierarchical tree. Thus, they can potentially operate faster when there is long carry chain. A further optimization is provided from the observation that dual rail encoding logic can benefit from settling of either the 0 or 1 path. Dual-rail logic need not wait for both paths to be evaluated. Thus, it is possible to further speed up the carry look-ahead circuitry to send carry-generate/carry-kill signals to any level in the tree. This is elaborated and referred as DICLA with speedup circuitry (DICLASP).

3 DESIGN OF PASTA

In this section, the architecture and theory behind PASTA is presented. The adder first accepts two input operands to perform half additions for each bit. Subsequently, it iterates using earlier generated carry and sums to perform half-additions repeatedly until all carry bits are consumed and settled at zero level. A. Architecture of PASTA The general architecture of the adder . The selection input

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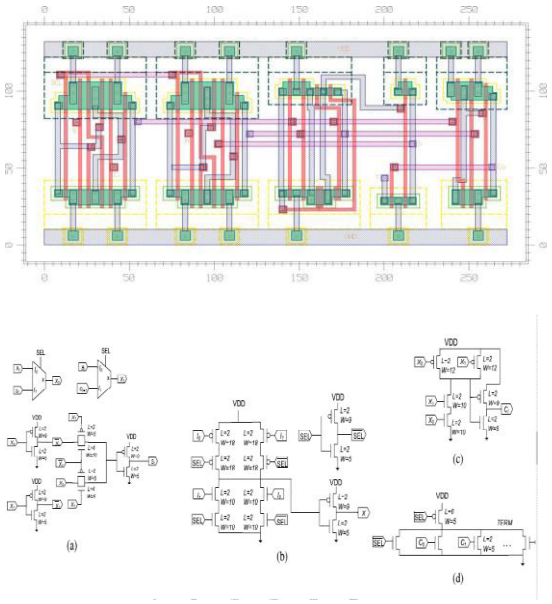
for two-input multiplexers corresponds to the Req handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially select the actual operands during SEL = 0 and will switch to feedback/carry paths for subsequent iterations using SEL = 1. The feedback path from the HAs enables the multiple iterations to continue until the completion when all carry signals will assume zero values. B. State Diagrams , two state diagrams are drawn for the initial phase and the iterative phase of the proposed architecture. Each state is represented by (Ci+1 Si) pair where i+1, Si represent carry out and sum values, respectively, from the ith bit adder block. During the initial phase, the circuit merely works as a combinational HA operating in fundamental mode. It is apparent that due to the use of HAs instead of FAs, state (11) cannot appear. During the iterative phase (SEL = 1), the feedback path through multiplexer block is activated. The carry transitions (Ci) are allowed as many times as needed to complete the recursion. From the definition of fundamental mode circuits, the present design cannot be considered as a fundamental mode circuit as the input–outputs will go through several transitions before producing the final output. It is not a Muller circuit working outside the fundamental mode either as internally, several transitions will take place.

4.IMPLEMENTATION

A CMOS implementation for the recursive circuit. For multiplexers and AND gates we have used TSMC library implementations while for the XOR gate we have used he faster ten transistor implementation based on transmission gate XOR to match the delay with AND gates. The completion detection is negated to obtain an active high completion signal (TERM). This requires a large fan-in *n*-input NOR gate. Therefore, an alternative more practical pseudo-nMOS ratio-ed design is used. The resulting design. Using the pseudo-nMOS design, the completion unit avoids the high fan-in problem as all the connections are parallel. The pMOS transistor connected to *V*DD of



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this ratio-ed design acts as a load register, resulting in static current drain when some of the nMOS transistors are on simultaneously. In addition to the *Ci* s, the negative of SEL signal is also included for the TERM signal to ensure that the completion cannot be accidentally turned on during the initial selection phase of the actual inputs. It also prevents the pMOS pull up transistor from being always on. Hence, static current will only be flowing for the duration of the actual computation. VLSI layout has also been performed for a standard cell environment using two metal layers. The layout occupies 270 λ × 130 λ for 1-bit resulting in 1.123 Mλ2 area for 32-bit. The pull down transistors of the completion detection logic are included in the single-bit layout (the T terminal) while the pull-up transistor is additionally placed for the full 32-bit adder. It is nearly double the area required for RCA and is a little less than the most of the area efficient prefix tree adder, i.e., Brent–Kung adder (BKA).

5 SIMULATION RESULTS

In this section, we present simulation results for different adders using Mentor Graphics Eldo SPICE version 7.4_1.1, running on 64-bit Linux platform. For implementation of other adders, we have used standard library implementations of the basic gates. The custom adders such as DIRCA/DICLASP are implemented based on their most efficient designs. Initially, we show how the present design of PASTA can effectively perform binary addition for different temperatures and process corners to validate the robustness under manufacturing and operational variations. In Fig. 4, the timing diagrams for worst and average cases corresponding to maximum and average length carry chain propagation over random input values are highlighted. The carry propagates through successive bit adders like a pulse as evident. The best-case corresponding to minimum length carry chain (not shown here) does not involve any carry propagation, and hence incurs only a single-bit adder delay before producing the TERM signal. The worst-case involves maximum carry propagation cascaded delay due to the carry chain length of full 32 bit. The independence of carry chains is evident from the average 8and *C*26 are shown to trigger at nearly the same time. This circuit works correctly for all process corners. For SF corner cases, one *C*out rising edge a short dynamic hazard. This has no follow on effects in the circuit nor are errors induced by the SF extreme corner case. The delay performances of different adders. We have used 1000 uniformly distributed random operands to represent the average case while best case,

worst case correspond to specific test-cases representing zero, 32-bit carry propagation chains respectively. The delay for combinational adders is measured at 70% transition point for the result bit that experiences the maximum delay. For self-timed adders, it is measured by the delay between SEL and TERM signals, as depicted The 32-bit full CLA is not practical due to the requirement of high fan-in, and therefore a hierarchical block CLA (B-CLAis implemented for comparison. The combinational adders, SPICE timing diagram for PASTA implementation using TSMC 0.35 μm process. The *C*out and *C*12 for worst case and average case, respectively, are shown for different conditions where TT, SF, and FS represents typical–typical, slow-fast, and fast–slow nMOS–pMOS conditions in these figures.

(a) Worst-case carry propagation while adding operands *(*FFFF FFFF*)*16 and *(*0000 0001*)*16.

(b) Average-case carry propagation while adding random operands of *(*3F05 0FC0*)*16 and *(*0130 0041*)*16.

Such as RCA/B-CLA/BKA/ Kogge–Stone adder (KSA)/Sklansky's conditional sum adder (SCSA) can only work for the worst-case delay as they do not have any completion sensing mechanism. Therefore, these results give an empirical upper bound of the performance enhancement that can be achieved using these adders as the basic unit and employing some kind of completion sensing technique. In the worst case, KSA performs best as they (along with SCSA) have the minimal tree-depth [10].

On the other hand, PASTA performs best among the self-timed adders. PASTA performance is comparable with the best case performances of conventional adders. Effectively, it varies between one and four times that of the best adder performances. It is even shown to be the fastest for TSMC 0.35 μm process.

For average cases, PASTA performance remains within two times to that of the best average case performances while for the worst case, it behaves similar to the RCA. Note that, PASTA completes the first iteration of the recursive formulation when "SEL = 0." Therefore, the best case delay represents the delay required to generate the TERM signal only and of the order of picoseconds.

Similar overhead is also present in dual-rail logic circuits where they have to be reset to the invalid state prior to any computation.

The dynamic/nMOS only designs require a precharge phase to be completed during this interval. These overheads are not included in this comparison.

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6 CONCLUSION

This brief presents an efficient implementation of a PASTA. Initially, the theoretical foundation for a single-rail wave-pipelined adder is established. Subsequently, the architectural design and CMOS implementations are presented. The design achieves a very simple *n*-bit adder that is area and interconnection-wise equivalent to the simplest adder namely the RCA. Moreover, the circuit works in a parallel manner for independent carry chains, and thus achieves logarithmic average time performance over random input values. The completion detection unit for the proposed adder is also practical and efficient. Simulation results are used to verify the advantages of the proposed approach.

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