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A CRITICAL EVALUATION OFISLANDING AND SEAMLESS RECONFIGURATION TECHNIQUE FOR MICROGRID SYSTEMWITH FUZZY LOGIC CONTROLLER BASED UPQC SCHEME

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ABSTRACT
In this project a powerful control and integration technique of the proposed UPQC in a distributed generation (DG)-based grid connected micro generation (μG) system is presented. The control technique of the presented UPQC μG is enhanced by implementing an intelligent islanding and novel reconnection technique with reduced number of switches that will ensure seamless operation of the μG without interruption. The shunt part of the UPQC Active Power Filter is placed at the Point of Common Coupling (PCC) and series part of the UPQC is connected before the PCC and in series with the grid. The dc link can also be integrated with the storage system. An intelligent islanding detection and reconnection technique (IR) are introduced in the UPQC as a secondary control. Hence, it is termed as UPQCμG−IR. The advantages of the proposed UPQCμG−IR over the normal UPQC are to compensate voltage interruption in addition to voltage sag/swell, harmonic, and reactive power compensation in the interconnected mode. During the interconnected and islanded mode, DG converter with storage will supply the active power only and the shunt part of the UPQC will compensate the reactive and harmonic power of the load. It also offers the DG converter to remain connected during the voltage disturbance including phase jump. An intelligent islanding detection and reconnection technique (IR) are introduced in the UPQC along with fuzzy logic as a secondary control. Hence, it is termed as UPQCμG−IR. During the interconnected and islanded mode, DG converter with storage will supply the active power only and the shunt part of the UPQC will compensate the reactive and harmonic power of the load. The simulation results are presented by using Matlab/Simulink software.

Key words: Distributed generation (DG), intelligent islanding detection (IsD), microgrid, power quality, smart grid, unified power quality compensator (UPQC), fuzzy logic controller.

I. INTRODUCTION
The challenging issues of a successful placement andintegration of unified power quality conditioner (UPQC) in adistributed generation (DG)-based grid connected microgrid (μG)system are1) Control complexity for active power transfer; 2) ability tocompensate non-active power during the islanded mode; and 3)difficulty in the capacity embellishment in a modular way [1].For a smooth power transfer between the grid-connected systemand islanded mode, various operational changes are presented,such as switching between the current and voltage control mode,robustness against the islanding detection and reconnectiondelays and method and so on [2], [4]. Clearly, these further increase the control complexity of the microgrid systems.To extend the operational flexibility and to improve the powerquality in

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grid connected microgrid systems, a new controlstrategy placement and integration technique of UPQC have beenproposed in [3], which is termed as UPQCμG.In the UPQCμGintegrated distributed system, micro grid (with storage) and shuntpart of the UPQCμG are placed at the Point of common coupling.The series of the UPQC is placed before the Point of commoncoupling and in series with the grid. DC link is connected to thestorage also, if present. In this paper, the control technique of the presented UPQC μG and fuzzy logic controller in [4] is enhancedhence; it is termed as UPQC μG−IR. The benefits offered by the proposed UPQC μG−IR over the conventional UPQCare as follows .To observe the effect on the characteristic of voltage sag / swell and interruption for the techniques.Both in the interconnected and islanded modes, the μG provide only the active power to the load. Therefore, it can reduce the control complexity of the DG converters. Islanding detection and reconnection technique are introduced inthe proposed UPQC as a secondary control. To maintain the operation in islanded mode andreconnection through the UPQC and fuzzy, communicationprocess between the UPQC μG and μG system is mentionedin [5]. In this paper, thecontrol technique of the presentedUPQC μG and fuzzy logic controller in[6] is enhanced byimplementing an intelligent islanding and novel reconnectiontechnique with reduced number of switches that will ensureseamless operation of the μG without interruption [7].Hence, it is termed as UPQC μG−IR. The benefits offered bythe proposed UPQC μG−IR over the conventional UPQC areas follows.

- It can compensate voltage interruption/sag/swell andnon-active current in the interconnected mode.
- Therefore, the DG converter can still be connected to the system during these distorted conditions. Thus, it enhances the operational flexibility of the DG converters/μG system to a great extent, which is furtherelaborated in later section.
- Shunt part of the UPQC Active Power Filter (APFsh) can maintain connection during the islanded mode and also compensates the non-active Reactive and HarmonicPower (QH) power of the load.
- Both in the interconnected and islanded modes, the μG provides only the active power to the load. Therefore, it can reduce the control complexity of the DG converters.
- Islanding detection and reconnection technique areintroduced in the proposed UPQC as a secondary control. A communication between the UPQC and μG is also provided in the secondary control. The DG converters may not require having islanding detection and reconnection features in their control system [8-12].

II WORKING PRINCIPLE

The integration technique of the proposed $UPQC_{\mu G-IR}$ to a grid connected and DG integrated μG system is shown inFig. 1(a). S2 and S3 are the breaker switches that are usedto island and reconnect the μG system to the grid as directedby the secondary control of the $UPQC_{\mu G-IR}$. The workingprinciple during the interconnected and islanded mode for thisconfiguration is shown in Fig.1 (b) and (c). The operation of $UPQC_{\mu G-IR}$ can be divided into two modes.

A. Interconnected Mode

In this mode, as shown in Fig. 1(b), the following holds:

1) The DG source delivers only the fundamental activepower to the grid, storage, and load;

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2) TheAPFsh compensates the reactive and harmonic (QH)power of the nonlinear load to keep the Total HarmonicDistortion at the PCC within the IEEE standard limit;
3) Voltage sag/swell/interruption can be compensated bythe active power from the grid/storage through the APFse,t. The DG converter does not sense any kindof voltage disturbance at the PCC and hence remainsconnected in any condition;
4) If the voltage interruption/black out occurs, UPQC sendsa signal within a preset time to the DG converter to beislanded.

B. Islanded Mode

In this case, as shown in Fig. 1(c), the following holds:
1) TheAPFse is disconnected during the grid failure and DGconverter remains connected to maintain the voltage atPCC;
2) TheAPFsh still compensates the nonactive power of the nonlinear load to provide or maintain undistorted currentat PCC for other linear loads (if any);
3) Therefore, DG converter (with storage) delivers only theactive power and hence does not need to be disconnectedfrom the system;
4) TheAPFse is reconnected once the grid power isavailable.
From Fig.1(a)–(c), it is clear that the UPQCμG−IR requirestwo switches compared with four, as required for UPQCμG in [4]. A detail of the switching mechanism is discussed inthe controller design section.

III. DESIGN ISSUES AND RATING SELECTION

The fundamental frequency representation of the system is shown in Fig. 1(d) and the voltage and current relations are derived in (1) and (2). According to the working principle, the APFse is able to work during voltage interruption/sag/swellup to a certain level before it is islanded. The APFsh always compensates QH power of the load. Therefore, design andrating selection for the APFse, APFsh, and series transformertogether with the sizing of dc link capacitor are very important.

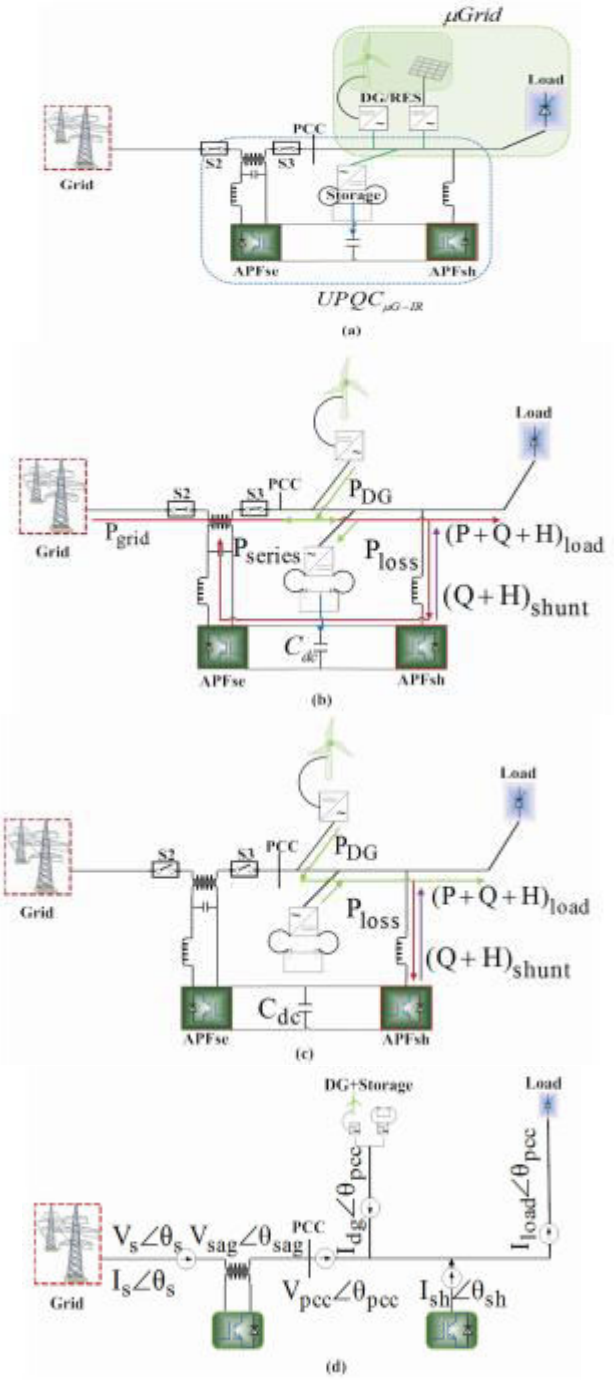

Fig.1. (a) Integration technique of the UPQCμG−IR. Working principle in(b) interconnected mode, (c) islanded mode, and (d) fundamental frequencyrepresentation.

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These are discussed in the following section:

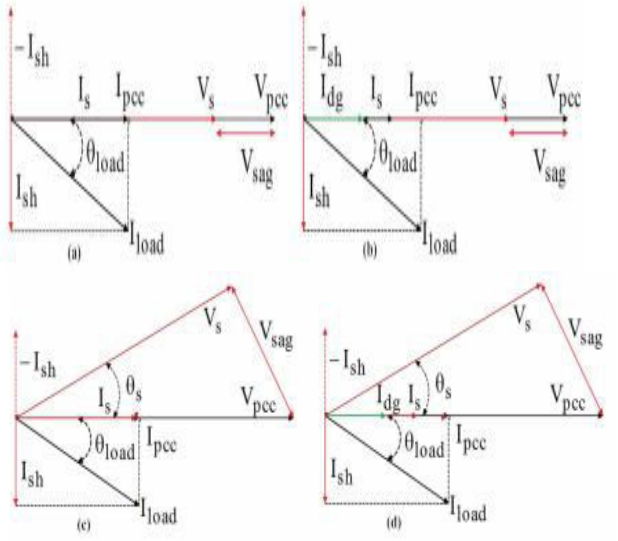
$$V_{pcc}\angle\theta_{pcc} = V_s\angle\theta_s + V_{sag}\angle\theta_{sag} \quad (1)$$

$$I_{load}\angle\theta_{load} = I_s\angle\theta_s + I_{dg}\angle\theta_{pcc} + I_{sh}\angle\theta_{sh} \quad (2)$$

Under any condition assume that $V_{pcc} = V_{dg} = V_{load}$ and$\theta_{pcc}= 0°$. The phasor diagrams of the proposed system indifferent conditions are shown in Fig.2.

A. Shunt Part of U P QC µG−I R (APFsh)

It is shown in Fig.2 that for any condition, APFsh compensates the non-fundamental current of the load by injecting Ishin quadrature to Vpcc. When voltage sag appears in the supplyside, APFse compensates the sag by injecting the requiredvoltage to maintain the constant voltage and zero-phase atPCC. To complete the task, APFsh draws additional current from the source, to supply power to the APFse. The increased source current *I′s*still remains in phase to the Vpcc. But thischanges the magnitude and phase angle of the compensating current, Ish as an additional active component of current (x) is added to the shunt compensator current now, as shown in Fig.2(e).



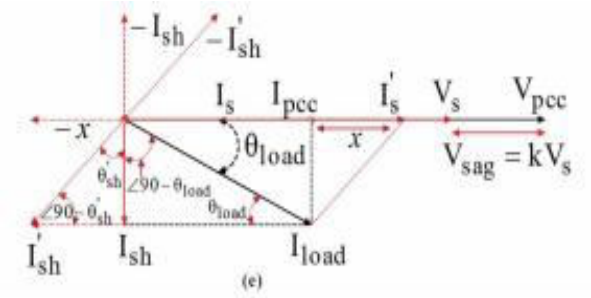


Fig.2. Phasor diagram of UPQCµG−IR when (a) no DG andθs =θpcc, (b) with DG and θs =θpcc, (c) no DG and θs≠θpcc, (d) with DG and θs ≠θpcc, and (e) in-phase voltage compensation mode.

In this case

$$I_s' = I_{pcc} + I_{sh}' \sin(\theta_{sh}') \quad (3)$$

$$I_{sh}' = I_{sh}/\cos(\theta_{sh}') \quad (4)$$

This ultimately increases the current at PCC and thus creates a VA loading impact on the APFsh, which is also observed in [6].

B. Series Part of UPQCµG−IR (APFse)

The APFse always appears in series with the grid. In the proposed integration technique when no energy is available from the DG unit and shunt the APF compensates the reactive and harmonic part of the load current, the active fundamental part of the load current (I_{loadfp}) flows through the APFse. Therefore, the APFse must have at least the same current rating as the active load fundamental requirement

$$I_{APF_{se,min}} = I_{loadfp} \quad (5)$$

From Fig.2(c) and (d), the general equation for voltage sag compensation by the APFse can be written as

$$V_{sag} = \sqrt{V_s^2 + V_{pcc}^2 - 2V_sV_{pcc}\text{Cos}(\theta_s - \theta_{pcc})}. \quad (6)$$

The voltage rating of the APFse should be equal to the highest value of the injected sag voltage, thus

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$$V_{\mathrm{APF_{se,rated}}} = V_{\mathrm{sag,max}} = kV_{\mathrm{load,rated}} \quad (7)$$

Assume k is the fraction of Vs that appears as a voltage sag

$$V_{\mathrm{sag}} = kV_s = kV_{\mathrm{load}} \text{ and } k < 1$$

Therefore, the VA rating of the APFse, can be calculated as

$$S_{\mathrm{APF_{se,rated}}} = I_{\mathrm{APF_{se,rated}}} V_{\mathrm{APF_{se,rated}}} = kP_{\mathrm{loadf,rated}} \quad (8)$$

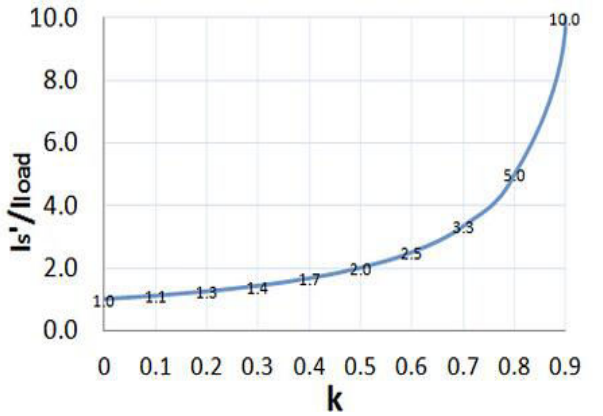

Fig.3. Relation between source current, load current, andkfor voltage sag compensation.

From Fig.2, the active power transfer through the APFse can be calculated for the case when Idg=0

$$P_{\mathrm{APF_{se}}} = P_{\mathrm{loadf}} \left[\frac{kV_s}{V_{\mathrm{load}}} \cos(\theta_s - \theta_{\mathrm{pcc}}) \right] \quad (9)$$

Under stable and in-phase operating conditions, assume that $\theta_s = \theta_{pcc} = 0$

$$P_{\mathrm{APF_{se}}} = \frac{kP_{\mathrm{loadf}} V_s}{V_{\mathrm{load}}} \quad (10)$$

Therefore, during voltage sag compensation, the source current that is transferred through the series transformer of the APFse, as shown in Fig.2(e), can be calculated as

$$I_s' = \frac{P_{\mathrm{loadf}}}{(1-k)V_s} = \frac{1}{(1-k)} I_{\mathrm{loadfp}} \quad (11)$$

Thus, the size and VA rating of the series transformer depends on the amount of sag to be compensated. Fig.3. shows how the source current increases with the value of k. Based on (6)–(11), and for a given value of k, there can be of multiple solutions for Vsag, I's, and P_{APFse}. Control strategies are based on the minimization of the energy exchange during compensation or by reducing the voltage rating [5]–[11].

The voltage rating of the APFse is an important design parameter, as it determines some other characteristics, such as the compensating range, the need to include (and size of) energy storage devices, and the overall size of the series transformer. In addition, losses tend to increase if the voltage rating of the A_{PFse} is increased. Therefore, the voltage injection capability should be chosen as low as necessary to reduce equipment cost and standby losses.

C. DC Link Capacitor

According to the working principle, the APFse should be able to work during a high-sag/swell condition and even in the case of interruption (depending on the interruption time) before it goes to the islanded mode. At this stage, the dc link capacitor should be able: 1) to maintain the dc voltage with minimal ripple in the steady state; 2) to serve as an energy storage element to supply the nonactive power of the load as a compensation; and 3) to supply the active power difference between the load and source during the sag/swell or interruption period. For a specific system, it is better to consider the higher value of C_{dc} so that it can handle all of the above conditions. It also helps to get a better transient response and lower the steady-state ripples. According to the calculation in [12], for the proposed system, the required capacitor size will be

$$C_{\mathrm{dc}} = \frac{2S_{\mathrm{load}} \cdot n \cdot T}{4 \cdot c \cdot V_{\mathrm{dc}}^2} \quad (12)$$

Where $S_{load}$is the total VA rating of the load, n is the number of cycles to perform the task, T is the time period, and c is the percentage of Vdc.

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It indicates that the size of the capacitor can be adjusted by the selection of cycles (n) for which the APFse will compensate. One of the purposes of the proposed integration technique of the UPQCμG−IR is to maintain smooth power supply duringsag/swell/interruption and extend the flexibility of the DG converters operation during interconnected and islanded modes. For the supply continuity, DG storage system has also been introduced. Therefore, a dc link connection between the capacitor and the DG storage has been proposed for the system. It will help to reduce the size of the capacitor and provide power during the sag/interrupt condition. Therefore, the source current will maintain the required load current active component and the additional current will be provided by the DG converters and storage. Thus, it will ultimately help to reduce the rating of the APFse converter.

IV. CONTROLLER DESIGN

The block diagram of the proposed UPQCμG−IR controller is shown in Fig.4. It has the same basic functionality as the UPQC controller except for the additional islanding detection and reconnection capabilities. A communication channel (signals transfer) between the proposed UPQCμG−IR and the μG is also required for the smooth operation. These signals generation are based on the sag/swell/interrupt/supply failure conditions. This task is performed in Level 2 (secondary control) of the hierarchical control. Level 1 deals with the primary control of the UPQC to perform their basic functions in the interconnected and the islanded mode. The overall integration technique and control strategy are to improve the power quality during interconnected and islanded modes. This involves detecting islanding and reconnection that ensures the DG converter remains connected and supply active power to the load. This reduces the control complexity of the converter as well as the power failure possibility in the islanded mode. The five main elements of the proposed UPQC$_{\mu G-IR}$ controller are: 1) positive sequence detection; 2) series part (APF$_{se}$) control; 3) shunt part (APF$_{sh}$) control; 4) intelligent islanding detection (IsD); and 5) synchronization and reconnection (SynRec). As the IsD and SynRec features are new in UPQC, therefore, these have been described in details.

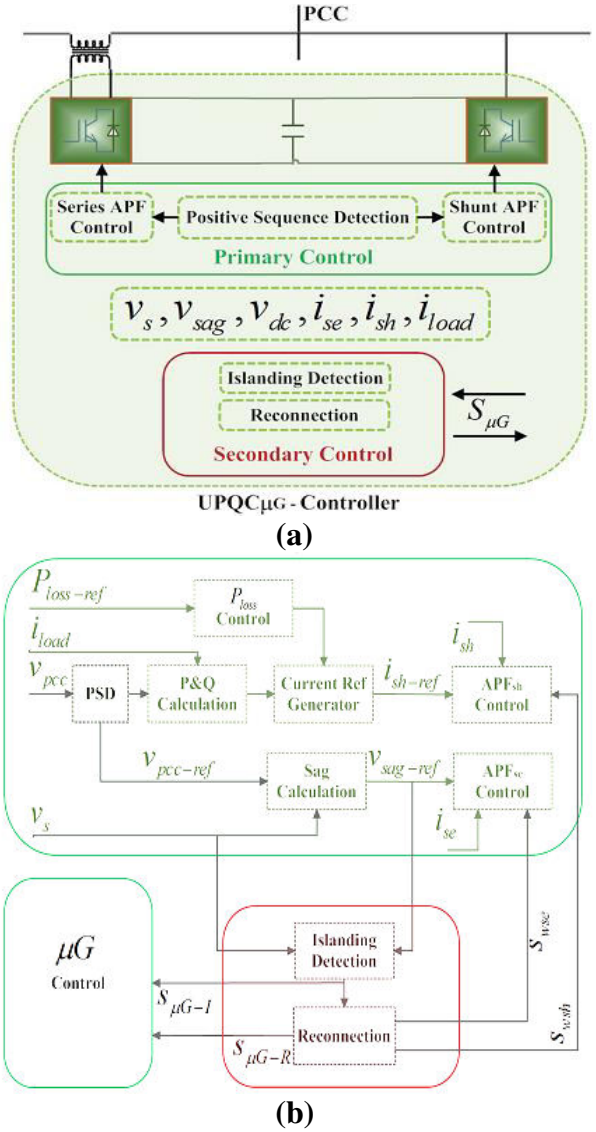

Fig.4. Block diagram of the UPQCμG−IR.(a) Controller. (b) Control algorithm.

A.Intelligent Islanding Detection

Considering the future trends toward the smart-grid and μG operation in connection with

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the distribution grid, the capability of: 1) maintaining connection during grid fault condition; 2) automatically detecting the islanded condition; and 3) reconnecting after the grid fault are the most important features of theμG system. In that case, the placement of APFse in the proposed integration method of the system plays an important role by extending the operational flexibility of the DG converter in the μG system. In addition to the islanding detection, changing the control strategy from current to voltage control may result in serious voltage deviations and it becomes severe when the islanding detection is delayed in the case of hierarchical control.Therefore, seamless voltage transfer control between the grid connected and isolated controlled modes is very important. Both indirect and direct current control techniques are proposed in [2] to mitigate the voltage transients in transition mode, but these then increase the control complexity of the μG converters.

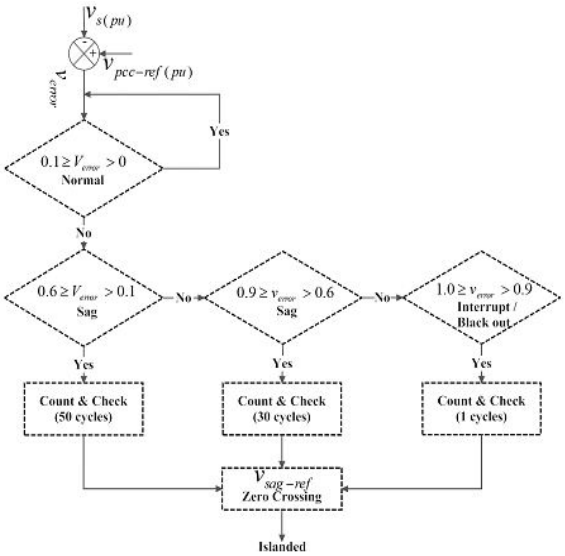

Fig.5. Algorithm for IsD method in UPQCμG−IR.

In the case of power quality problems, it is reported that more than 95% of voltage sags can be compensated by injecting a voltage of up to 60% of the nominal voltage, with a maximum duration of 30 cycles. Therefore, based on the islanding detection requirement and sag/swell/interrupt compensation, islanding is detected and a signal SμG−I, as shown in Fig.4(b), is also generated in the proposed UPQCμG−IR to transfer it to the DG converters. As the APIn the case of power quality problems, it is reported that more than 95% of voltage sags can be compensated by injecting a voltage of up to 60% of the nominal voltage, with a maximum duration of 30 cycle. Therefore, based on the islanding detection requirement and sag/swell/interrupt compensation, islanding is detected and a signal SμG−I,as shown in Fig.4(b), is also generated in the proposed UPQCμG−IR to transfer it to the DG converters. As the APFse takes the responsibilityfor compensating voltage sag/swell/unbalancedisturbances(depending on the controller), IsD algorithm in the proposed UPQCμG−IR can be simple yet quite flexible. On the other hand, it will help to reduce the complexity of islanding detection technique or even can be removed from all the DG converters in a μG system.Fse takes the responsibility for compensating voltage sag/swell/unbalance disturbances (depending on the controller),IsD algorithm in the proposed UPQCμG−IR can be simple yet quite flexible. On the other hand, it will help to reduce the complexity of islanding detection technique or even can be removed from all the DG converters in a μG system.

Fig.5 shows a simple algorithm (with example) that has been used to detect the islanding condition to operate the UPQC in islanded mode. The voltage at PCC is taken as the reference and it is always in phase with the source and the DG converters, the difference between the Vpcc-ref (pu) and Vs (pu) is V error. This error is then compared with the preset values (0.1–0.9) and a waiting period (user defined n cycles) is used to determine the sag/interrupt/islanding condition. In this example: 1) if Verror is less than or equal to

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0.6, then 60% sag will be compensated for up to 50 cycles; 2) if Verror is in between 0.6 and 0.9, then compensation will be for 30 cycles; and 3) otherwise (ifVerror≥0.9) it will be interrupt/black out for islanding after 1 cycle.

This signal generation method is simple and can be adjusted for any time length and Verror condition. Thus, the intelligence can be achieved by introducing the operational flexibility of time and control of sag/interrupt compensation before islanding. As the seamless voltage transfer from grid connected to isolated mode is one of the critical tasks in transition period, the transfer is completed at the zero-crossing position of the APFse. Therefore, no voltage fluctuation or abrupt conditions occur.

It is to be noted that, this is the first time the algorithm and islanding techniques are introduced in the control part of the UPQC, which are intelligent and flexible in operation. According to Fig.1, the proper control and operation of the switches are very important for intelligent islanding and seamless reconnection. In that case, this paper presents a topology that represents a step forward compared with the use of intelligent connection agents (ICA) as presented, an additional module named ICA is connected to an existing μG with a number of current sources. The ICA module acts as voltage source to fix the voltage and frequency in islanding mode and is able to guarantee seamless connection/disconnection of the μG from the main grid. The UPQCμG−IR presented in this paper is not only able to perform these seamless transitions, but also improve the power quality with some operational flexibility. In addition, the UPQC having a series element (APFse) can perform the role of voltage source of the μG, and easily PCC voltage observation-based anti-islanding algorithm can be implemented, as shown in Fig.5. Notice that using conventional equipment, e.g., in grid connected PV systems, the non-detection zone (NDZ) increases with the number of PV inverters, since they are not able to distinguish between the external grids or other PV inverters output voltage, thus may remain connected for a dangerously long time. With the proposed UPQC control strategy, we can add it in an existing PV plant, and this unit will be the only one responsible of the voltage support and islanding detection, thus being more effective and reducing drastically the NDZ.

VI.FUZZY LOGIC CONTROL

Many applications, such as robotics and factory automation, require precise control of speed and position. Speed Control Systems allow one to easily set and adjust the speed of a motor. The control system consists of a speed feedback system, a motor, an inverter, a controller and a speed setting device. A properly designed feedback controller makes the system insensible to disturbance and changes of the parameters.

A.PI Controller:

The purpose of a motor speed controller is to take a signal representing the demanded speed, and to drive a motor at that speed. Closed loop speed control systems have fast response, but become expensive due to the need of feedback components such as speed sensors. Speed controller calculates the difference between the reference speed and the actual speed producing an error, which is fed to the PI controller. PI controllers are used widely for motion control systems. They consist of a proportional gain that produces an output an output proportional to the input error an integration to make the steady state error zero for a step change in the input. PI controller is a generic control loop feedback mechanism (controller) widely used in industrial control systems – a PI is the most commonly used feedback controller and calculates an "error" value as the difference between a measured process variable and a desired set point. The controller attempts to minimize the error by adjusting theprocess control inputs. The PI

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controller calculation (algorithm) involves two separate constant parameters, and is accordingly sometimes called two-term control: the proportional, the integral values, denoted P, I. Heuristically, these values can be interpreted in terms of time: P depends on the present error, I on the accumulation of past errors, based on current rate of change. The weighted sum of these three actions is used to adjust the process via a control element such as the position of a control valve. There are several methods for tuning a PI loop.

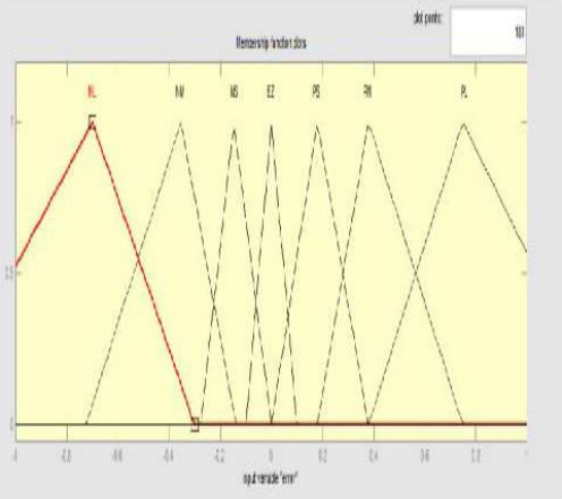

Fig.6. Membership functions of FLC

B.FLC Controller:

Fuzzy logic is widely used in control technique. The term "fuzzy" refers to the fact that the logic involved can deal with concepts that cannot be expressed as "true" or "false" but rather as "partially true". Although alternative approaches such as genetic algorithms and neural networks can perform just as well as fuzzy logic in many cases, fuzzy logic has the advantage that the solution to the problem can be cast in terms that human operators can understand, so that their experience can be used in the design of the controller of BLDC. The linguistic variables are defined as (NB, NS, Z, PS, PB) which mean big, negative small, zero, positive small and positive big respectively. The membership functions are shown in Fig. 6.

u	e						
	NB	NM	NS	Z	PS	PM	PB
PB	Z	PS	PM	PB	PB	PB	PB
PM	NS	Z	PS	PM	PB	PB	PB
Δe PS	NM	NS	Z	PS	PM	PB	PB
Z	NB	NM	NS	Z	PS	PM	PB
NS	NB	NB	NM	NS	Z	PS	PM
NM	NB	NB	NM	NM	NS	Z	PS
NB	NB	NB	NB	NB	NM	NS	Z

Table 1.The decision table of FLC.

As seen from table 1, each interval of each variable is divided into seven membership functions:
Negative Big (NB), Negative Medium (NM), Negative Small (NS), Zero (Z), Positive Small (PS), Positive Medium (PM) and Positive Big (PB).

C. Hybrid Fuzzy-PID Controller

Although it is possible to design a fuzzy logic type of PID controller by a simple modification of the conventional ones, via inserting some meaningful fuzzy logic IF- THEN rules into the control system, these approaches in general complicate the overall design and do not come up with new fuzzy PID controllers that capture the essential characteristics and nature of the conventional PID controllers. Besides, they generally do not have analytic formulas to use for control specification and stability analysis. The fuzzy PD, PI, and PI+D controllers to be introduced below are natural extensions of their conventional versions, which preserve the linear structures of the PID controllers, with simple and conventional analytical formulas as the final results of the design. Thus, they can directly replace the conventional PID controllers in any operating control systems (plants, processes).
The main difference is that these fuzzy PID controllers are designed by employing fuzzy

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logic control principles and techniques, to obtain new controllers that possess analytical formulas very similar to the conventional digital PID controllers.

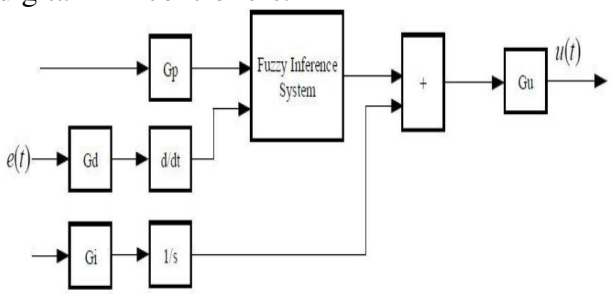

Figure.7. Hybrid Fuzzy PID Controller

IV.MATLAB/SIMULATION RESULTS

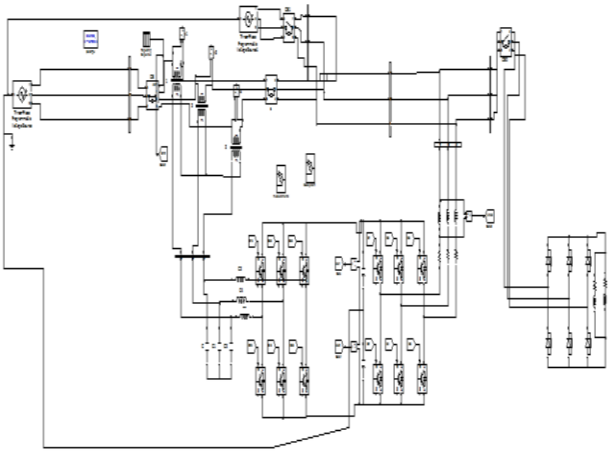

Fig.8 MATLAB/SIMULINK Circuit for the UPQCμG−IR

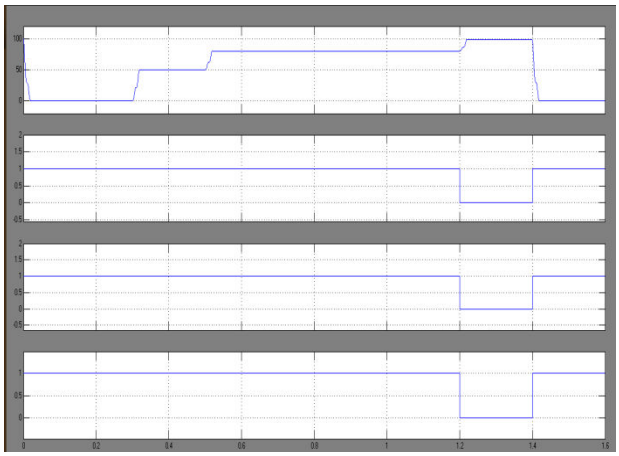

Fig.9 Error voltage, Switch 2 voltage, Switch 3 voltage and Islanding reconnection

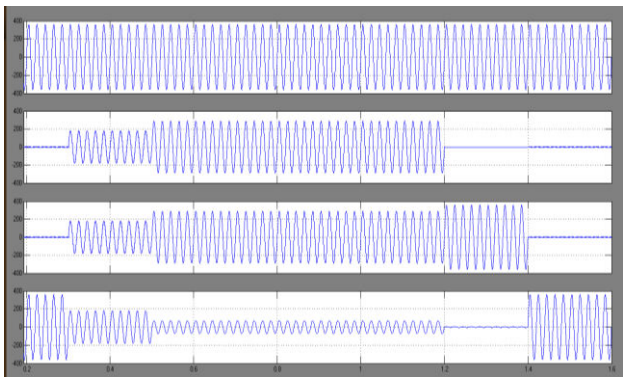

Fig.10 Point of Common Coupling (PCC) voltage, Sag Voltage, Reference sag voltage and supply voltage

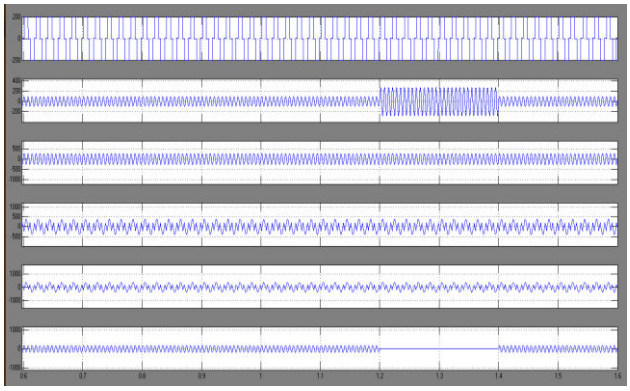

Fig.11 Load current, Distributed Generation current, Point of Common Coupling (PCC) current, Shunt current, Reference shunt current and Source current

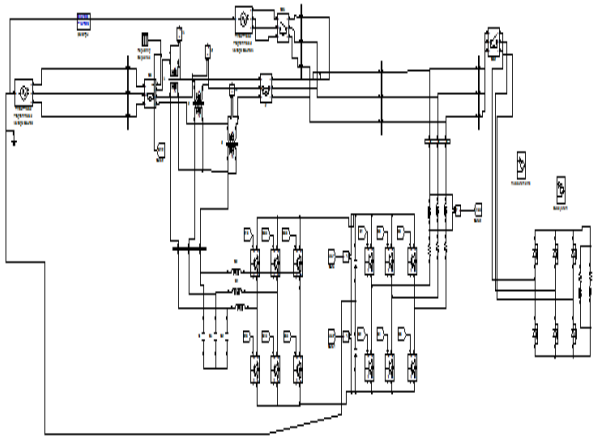

Fig.12 MATLAB/SIMULINK Circuit for the UPQCμG−IR performance

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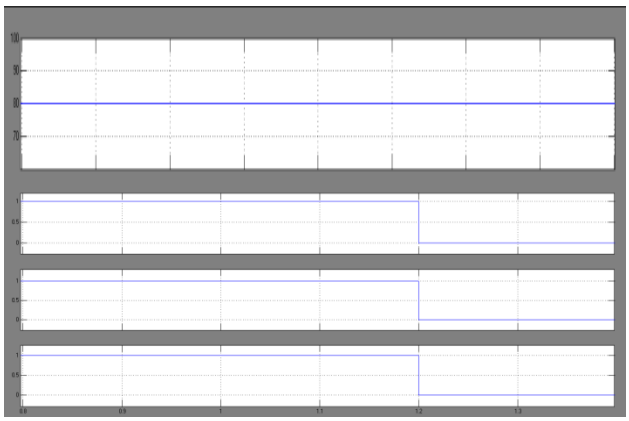

Fig.13 Error voltage, Switch 2 voltage, Switch 3 voltage and Islanding reconnection

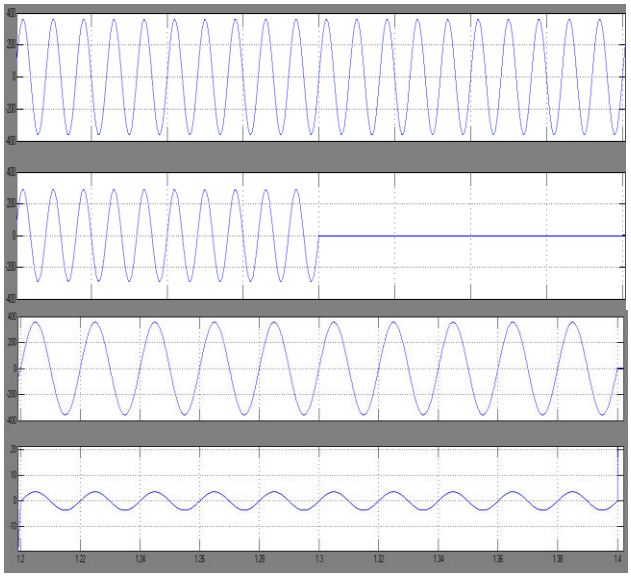

Fig.14Point of Common Coupling (PCC) voltage, Sag Voltage, Reference sag voltage and supply voltage

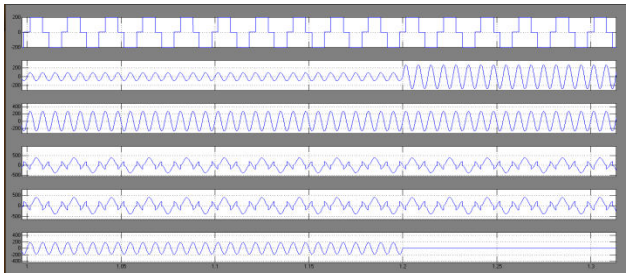

Fig.15Load current, Distributed Generation current, Point of Common Coupling (PCC) current, Shunt current, Reference shunt current and Source current

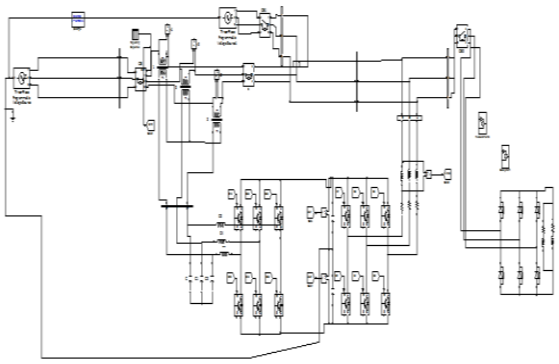

Fig.16MATLAB/SIMULINK Circuit for the UPQCμG−IR reconnection

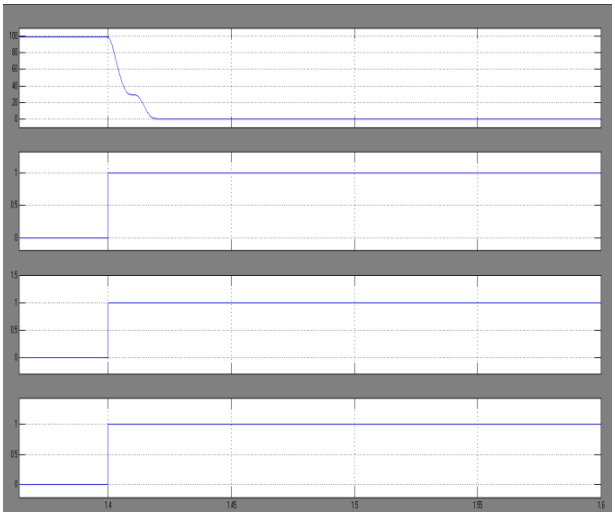

Fig.17Error voltage, Switch 2 voltage, Switch 3 voltage and Islanding reconnection

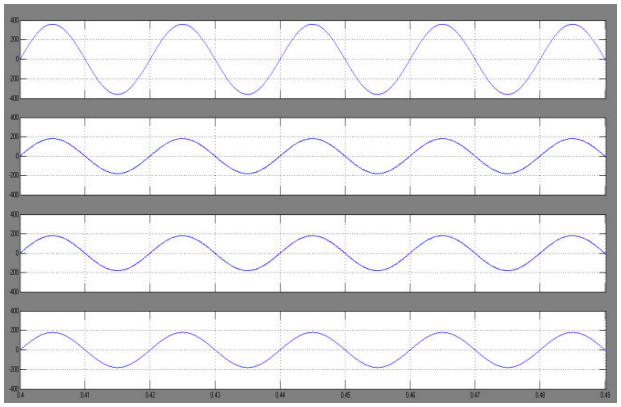

Fig.18Point of Common Coupling (PCC) voltage, Sag Voltage, Reference sag voltage and supply voltage

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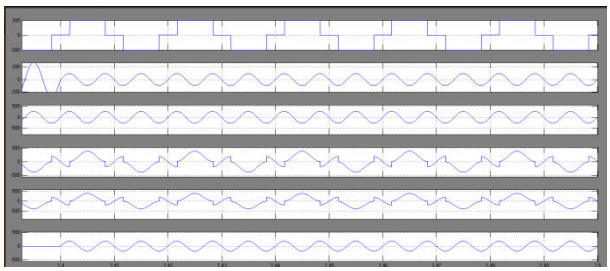

Fig.19Load current, Distributed Generation current, Point of Common Coupling (PCC) current, Shunt current, Reference shunt current and Source current

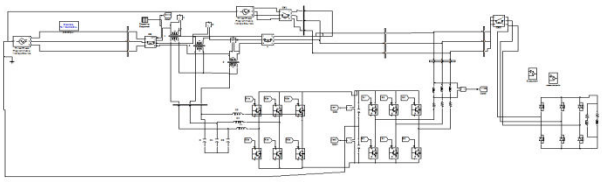

Fig.20MATLAB/SIMULINK Circuit for the UPQCμG−IR with PI controller

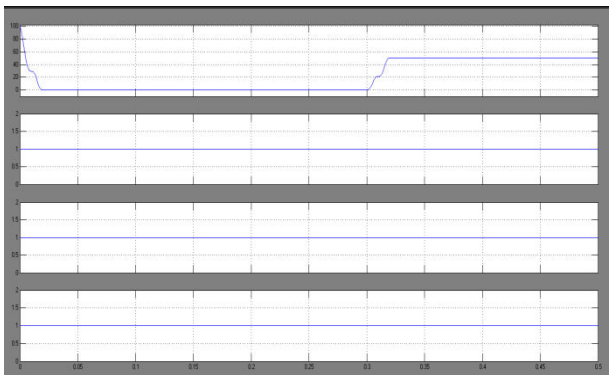

Fig.21Error voltage, Switch 2 voltage, Switch 3 voltage and Islanding reconnection

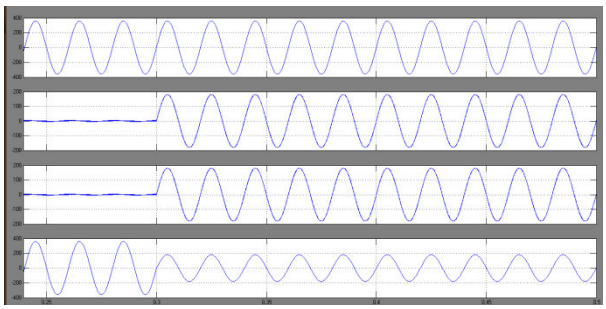

Fig.22Point of Common Coupling (PCC) voltage, Sag Voltage, Reference sag voltage and supply voltage

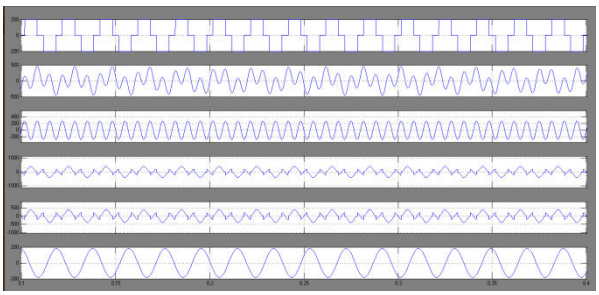

Fig.23 Load current, Distributed Generation current, Point of Common Coupling (PCC) current, Shunt current, Reference shunt current and Source current

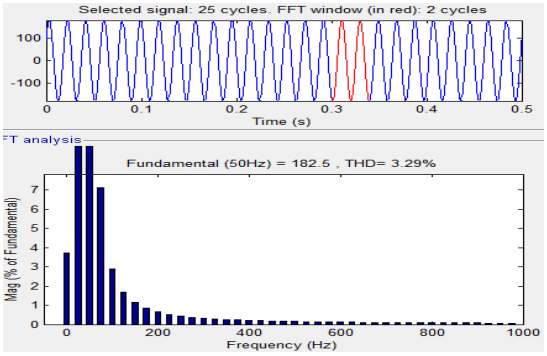

Fig.24Source current THD

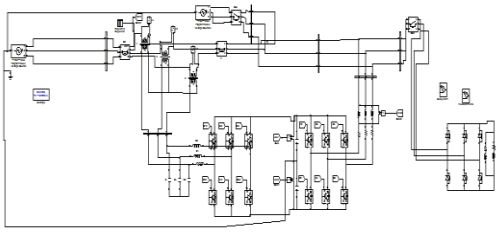

Fig.25MATLAB/SIMULINK Circuit for the UPQCμG−IR with FUZZY Logic controller

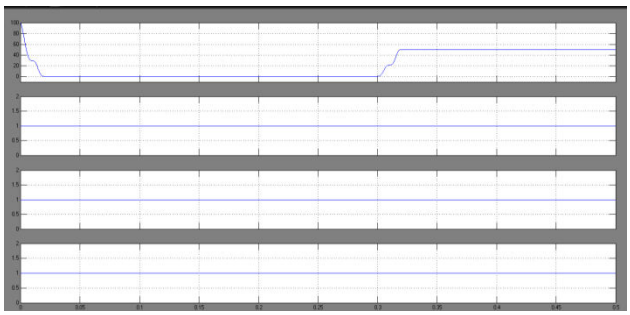

Fig.26Error voltage, Switch 2 voltage, Switch 3 voltage and Islanding reconnection

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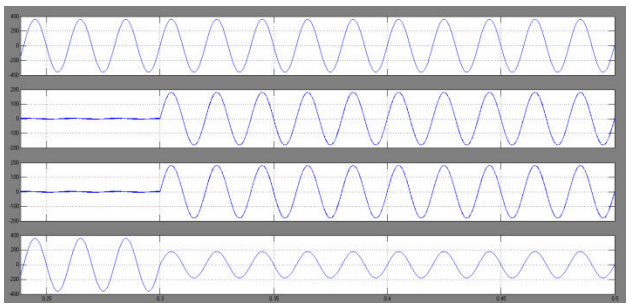

Fig.27Point of Common Coupling (PCC) voltage, Sag Voltage, Reference sag voltage and supply voltage

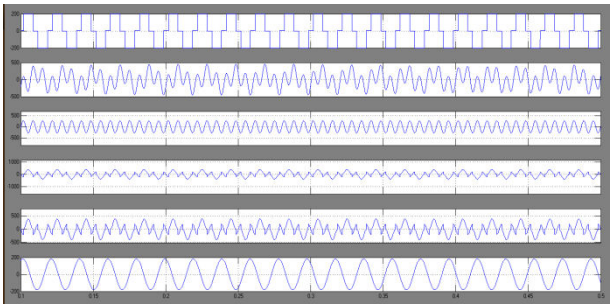

Fig.28 Load current, Distributed Generation current, Point of Common Coupling (PCC) current, Shunt current, Reference shunt current and Source current

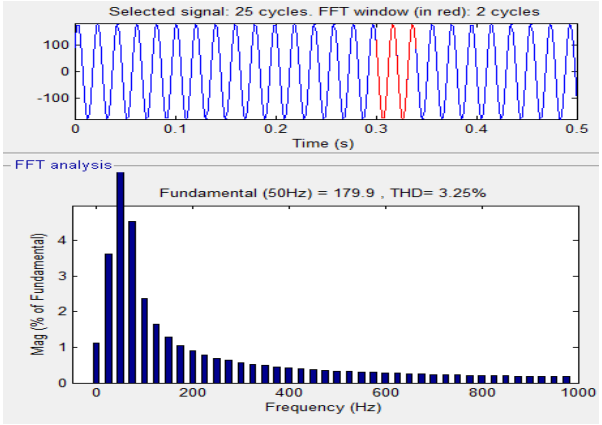

Fig.29Source current THD

V.CONCLUSION

In this thesis a new proposal for the placement, integration, and control of unified power quality conditioner (UPQC) in distributed generation (DG)-based grid connected/autonomous micro grid/micro generation (µG) system hasbeen proposed along with fuzzy logic controller. The performance withoff-line simulation has been obtained. The results show that theUPQCmicrogrid-IR can compensate the voltage and currentdisturbance at the Point of Common Coupling during theinterconnected mode. In islanded mode, the DG converters onlysupply the active power. Therefore, the DG converters need notto be disconnected or change their control strategy to keep theMicroGrid operating in any time with any condition.This paper describes integration technique of the proposedUPQCµG−IR in the grid connected µG condition using fuzzy logic controller. The performance with off-linesimulation has obtained by using MATLAB. The results show that the UPQCµG−IR can compensate the voltage andcurrent disturbance at the PCC during the interconnected mode.

REFERENCES

[1] S K Khadem, M Basu, M F Conlon, UPQC for Power Quality Improvementin DG Integrated Smart Grid Network – A Review, Int Journal of Emerging Electric Power Systems, Vol. 13(1), 2012, Art 3

[2] X. Yu, A.M. Khambadkone, H. Wang, S. Terence, Control of ParallelConnectedPower Converters for Low-Voltage Microgrid—Part I: A HybridControl Architecture, IEEE Trans

[3] S K Khadem, M. Basu, M.F. Conlon, A new placement and integrationmethod of UPQC to improve the power quality in DG network, Universities Power Engineering Conference

[4] A Kahrobaeian, Y Mohamed, Interactive distributed generation interface forflexible microgrid operation in smart distribution systems, IEEE TransSustainable Energy, vol.3(2), pp.295-305, 2012 Power Electronics , vol.25(12), 2010, pp.2962-2970 , UPEC, Vol.1, Sept 2013.

[5] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuña, and M. Castilla, "Hierarchical control of droop-controlled AC and DC micro grids—A general approach toward standardization," IEEETrans. Ind. Electron., vol. 58, no. 1, pp. 158–172, Jan. 2011.

[6] B. Han, B. Bae, H. Kim, and S. Baek, "Combined operation of unified power-quality conditionerwith distributed generation," IEEE Trans. Power Del., vol. 21, no. 1, pp. 330–338, Jan. 2006.

[7] J. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensate voltage sags with phase jump," in Proc.16th APEC, vol. 2. 2001, pp. 1267–1273.

[8] D. M. Vilathgamuwa, A. R. Perera, and S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer," IEEE Trans.Power Del., vol. 18, no. 3, pp. 928–936, Jul. 2003.

[9]S.S.Choi, J.D.Li, and D.M.Vilathgamuwa,―A generalized voltage compensation strategy for mitigating the impacts of voltagesags/swells,‖ IEEE Trans. Power Del., vol. 20, no. 3, pp. 2289–2297, Jul. 2005.

[10] M. R. Banaei, S. H. Hosseini, S. Khanmohamadi, and G. B. Gharehpetian, ―Verification of a new control strategyfor dynamic voltage restorer by simulation, ‖Simul. Model. Pract. Theory, vol. 14, no. 2, pp. 112–125, 2006.

[11] M. Moradlou and H. R. Karshenas, ―Design strategy for optimum rating selection of interline DVR,‖ IEEE Trans.Power Del., vol. 26, no. 1, pp. 242–249, Jan. 2011.

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