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Volume 06, Issue 04,Page No: 1157 - 1164.

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EFFICIENT SHIFT REGISTER FOR LOW-POWER AND LOW-AREA USING PULSED LATCHES

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ABSTRACT:

A low-Power and low- area efficient shift register using pulsed latches. A shift register is the basic building block in a VLSI circuit. The architecture of a shift register is quite and simple. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signal instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shift register and using additional temporary storage latches. A 256 bit shift register using pulsed latches was fabricated using a CMOS process.

Keywords: Area-Efficient, Flip-Flop, Pulsed Clock, Pulsed Latch, Shift Register.

I. INTRODUCTION:

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches. This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single

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pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches

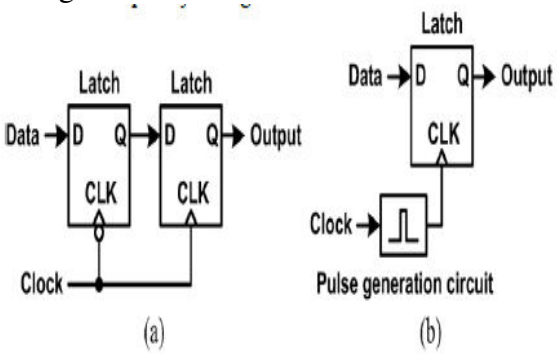

Fig.1. (a) Master-slave flip-flop (b) Pulsed latch

Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process scaled down according to Moore‘s Law, designers are able to integrate many numbers of transistors onto the same die. The more transistors there will be more switching and more power dissipated in the form of heat or radiation. Heat is one of the phenomenon packaging challenges in this epoch; it is one of the main challenges of low power design methodologies and practices. Another driver of low power research is the reliability of the integrated circuit. More switching implies higher averagecurrent is expelled and therefore the probability of reliability issues occurring rises. We are moving from laptops to tablets and even smaller computing digital systems. With this profound trend continuing and without a match trending in battery life expectancy, the more low power issues will have to bead dressed. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today‘s and future integrated chips. Power consumption of Very Large Scale Integrated design is given by generalized relation, P = CV2f. Since power is proportional to the square of the voltage as per the relation, voltage scaling is the most prominent way to reduce power dissipation. However, voltage scaling is results in threshold voltage scaling which bows to the exponential increase in leakage power. Though several contributions have been made to the art of single edge triggered flip-flops, a need evidently occurs for a design that further improves the performance of single edge triggered flip flops patterns. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

II. SHIFT REGISTERS

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers and image processing ICs Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register A 16- megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register

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become important design considerations. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing

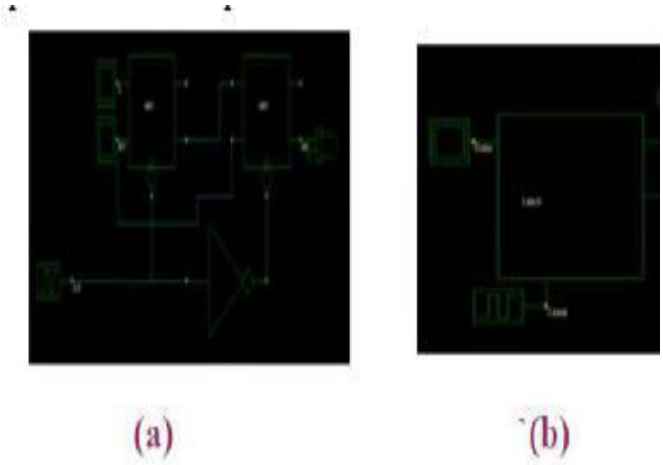

Fig.1.1. Schematic diagrams of (a) master-slave flip flop. (b) Pulsed latch.

This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Shift registers can have both parallel and serial inputs and outputs. These are often configured as _serial-in, parallel-out' (SIPO) or as _parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also _bidirectional' shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a _circular shift register'

previous work often measured energy consumption using a limited set of data patterns with the clock switching every cycle. But real designs have a wide variation in clock and data activity across different TE instances. For example, low power microprocessors make extensive use of clock gating resulting in many TEs whose energy consumption is dominated by input data transitions rather than clock transitions. Other TEs, in contrast, have negligible data input activity but are clocked every cycle. Shift registers, like counters, are a form of sequential logic. Sequential logic, unlike combinational logic is not only affected by the present inputs, but also, by the prior history.

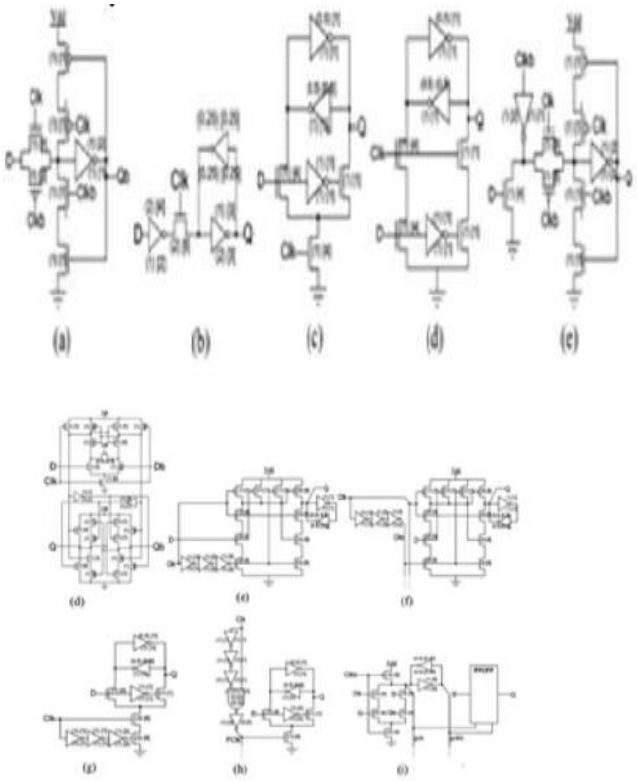

Fig.3. High-enabled latch designs. Transistor sizes are shown for a low-power design (in parentheses: ( )) and a high-speed design (in brackets: [ ]). A transistor labeled with size. (a) PPCFF. (b) SSAFF. (c) SAFF. (d)

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MSAFF. (e) HLFF. (f) HLSFF. (g) SSAPL. (h) SSASPL. (i) CCPPCFF.

In other words, sequential logic remembers past events. Pulsed latch structures employ an edge-triggered pulse generator to provide a short transparency window. Compared to master–slave flip-flops, pulsed latches have the advantages of requiring only one latch stage per clock cycle and of allowing time-borrowing across cycle boundaries. The major disadvantages of pulsed latch structures are the increased susceptibility to timing hazards and the energy dissipation of the local clock pulse generators.Pulse generators can be shared among a few latch cells to reduce energy, if care is taken that the pulse shape does not degrade due to wire delay, signal coupling and noise. We measured designs both with individual pulse generators and with pulse generators shared among four latch bits, in which case we divide the pulse generator energy among the four latch instances. HLFF [see Fig. 3(e)] operates as a pulsed transparent latch and is regarded as one of the fastest known flip-flop designs HLSFF [see Fig. 3(f)] is HLFF with a shared inverter chain. SSAPL [see Fig. 3(g)] is a pulsed version of SSALA with individual pulse generators, while SSASPL [see Fig. 3(h)] has a shared pulse generator. Note that the two series transistors in SSAPL are replaced by a single transistor in SSASPL. Traditionally, the power consumption of flip-flop and latch designs has been measured using an unrated clock and a small number of input activation patterns. Instead, we adopt a more accurate methodology in which all possible states (e.g., clock value, input value, output value) of the TE are enumerated and the energy consumption of each state transition is measured. Some designs perform extremely well in certain regimes, but extremely poorly in others. For example, in test2 the low power SSAFF design uses eight times less energy than the HLFF structure, but in test 3 it uses seven times more energy. Another good example of a TE specialized for an operating regime is CPNLA. This latch design is by far the best choice for test 3, but by far the worst choice in all other cases. Finally, CCPPCFF [see Fig. 3(i)] is a conditional clocking flip-flop based on the design presented in, which in turn is an improvement. The goal of this design is to reduce energy when the input data does not change by gating the clock within the flip-flop.

III. LITERATURE REVIEW A. Progress with Physically and Logically Reversible Superconducting Digital Circuits

Jie Ren and Vasili K. Semenov had proposed this. We continue to develop a new Superconductor Flux Logic (SFL) family based on nSQUID gates with fundamentally low energy dissipation and the ability to operate in irreversible and reversible modes. Prospective computers utilizing the new gates can keep conventional logically irreversible architectures. In this case the energy dissipation is limited by fundamental thermodynamic laws and could be as low as a few s per logic operation. Highly exotic and less practical logically and physically reversible circuit architectures are more attractive for us because they enable a reduction of the specific energy dissipation well below the thermodynamic threshold. The reversible option is of interest to us because we can then experimentally demonstrate that all technical mechanisms of the energy dissipation could be cut below the fundamental thermodynamic limit. In other words, we like to set the energy dissipation record for all conventional digital technologies that (if measured in) is about one million times below the best figures achieved in commercially available semiconductor circuits. Besides, we believe that diving below the thermodynamic threshold would have impressive scientific and philosophical impacts.

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In this paper we introduce a new timing belt clocking scheme and present new circuits. While we still work with test circuits, some of them contain two 8- stage shift registers, one with direct and the other with inverted outputs. The energy dissipation per nSQUID gate per bit measured at 4 K temperature is already below the thermodynamic threshold. We are confident that we passed through the critical phase of the paper and we simply need more time to make more sophisticated circuits. The extremely low energy dissipation converts our circuits into a natural candidate to support circuitry for any sensors operating at mille-Kelvin temperatures

.B. Reversible AC Drive Systems Based on Parallel AC– AC DC-Link Converters

Cursino Brandão Jacobina had proposed this. In this paper, two reversible single-phase-to-three phase ac drive systems are proposed. They are composed of an induction motor fed by two parallel single-phase-to-three-phase dc-link converters without isolation transformers. Suitable modeling and control strategy of the systems based on odq approach, including the unbalanced case, are developed. The proposed topologies permit reducing the harmonic distortion and presents fault tolerance characteristics. Even if the number of switches is increased, the total energy loss of the proposed systems can be lower than that of a conventional one. It is shown that the reduction of the circulating current is an important objective for the system design. A single-phase-to-three-phase dc-link converter generalization has been proposed as well. Simulated and experimental results are presented.

1. Testing of Quantum Cellular Automata

Mehdi B. Tahoori, Jing Huang, Mariam Momenzadeh, and Fabrizio Lombardi had proposed this. There has been considerable research on quantum dot cellular automata (QCA) as a new computing scheme in the nano-scale regimes. The basic logic element of this technology is the majority vote. In this paper, a detailed simulation-based characterization of QCA defects and study of their effects at logic level are presented. Testing of these QCA devices at logic level is investigated and compared with conventional CMOS-based designs. Unique testing features of designs based on this technology are presented and interesting properties have been identified. A testing technique is presented; it requires only a constant number of test vectors to achieve 100% fault coverage with respect to the fault list of the original design. A design-for-test scheme is also presented, which results in the generation of a reduced test set at 100% fault coverage.

2. Constructing Online Testable Circuits using Reversible Logic

Sk. Noor Mahammad and Kamakoti Veezhinathan had proposed this. With the advent of nanometer technology, circuits are more prone to transient faults that can occur during its operation of the different types of transient faults reported in the literature, the single event upset (SEU) is prominent. Traditional techniques such as triple-modular redundancy (TMR) consume large area and power. Reversible logic has been gaining interest in the recent past due to its less heat dissipation characteristics. This paper proposes the following:

a novel universal reversible logic gate (URG) and a set of basic sequential elements that could be used for building reversible sequential circuits, with 25% less garbage than the best reported in the literature;

(2) a reversible gate that can mimic the functionality of a lookup table (LUT) that can

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be used to construct a reversible field-programmable gate array (FPGA);

(3) automatic conversion of any given reversible circuit into an online testable circuit that can detect online any single-bit errors, including soft errors in the logic blocks, using theoretically proved minimum garbage, which is significantly lesser than the best reported in the literature. Conservative logic is called reversible conservative logic when there is a one-to-one mapping between the inputs and the outputs vectors along with the property that there is equal number of 1s in the outputs as in the inputs. Conservative logic circuits are not reversible, if one-to-one mapping between the inputs and the outputs vectors is not preserved. Conservative logic can be reversible in nature or may not be reversible in nature. Reversibility is the property of circuits in which there is one to- one mapping between the inputs and the output vectors that is for each input vector there is a unique output vector and vice-versa. QCA is one of the emerging nanotechnologies in which it is possible to implement reversible logic gates.

QCA makes it possible to achieve circuit densities and clock frequencies beyond the limits of existing CMOS technology. In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell. Thus, when the bit is flipped from 1 to 0 there is no actual discharging of the capacitor as in conventional CMOS. Hence, QCA does not have to dissipate all its signal energy during transition. Further, propagation of the polarization from one cell to another is because of interaction of the electrons in adjacent QCA cells. As there is no movement of electrons from one QCA cell to the other, there is no current flow. Therefore, QCA has significant advantage compared to CMOS technology in terms of power dissipation. Due to high error rates in nano-scale manufacturing, QCA and other nanotechnologies target reducing device error rates.

IV. RESULTS

The proposed 256-bit shift register with K =4 was fabricated using a 0.18μm CMOS process. Table I lists the features of the shift register chip. The chip occupies 6600μm2 and consumes 1.2 mW at VDD=1.8V and fCLK=100MHz. Fig.4 shows a microphotograph of a chip. Figs. 5(a) and 5(b) show the measured waveforms of the shift-register at fCLK=100MHz and fCLK=10MHz, respectively. In the simulations, the shift register with K =4 operates up to fCLK=840MHz, but in the measurements, the clock frequency was 100 MHz due to the frequency limitation of the experimental equipment. Fig. 5(a) represents a clock signal of 100 MHz, an input signal (IN), two output signals from the first sub shift resister (Q1 and Q2). Fig. 5(b) shows a clock signal of 10 MHz, an input signal (IN), eight output signals from the first and second sub shift resisters (Q1– 8), the last output signal of the 256-bit shift register (Q256).

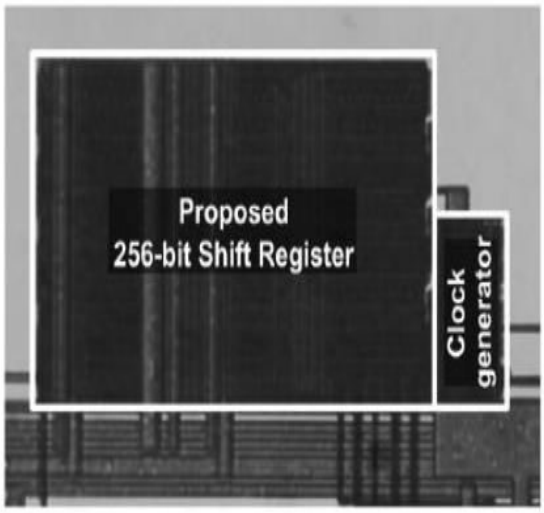

Fig.4. Chip microphotograph.

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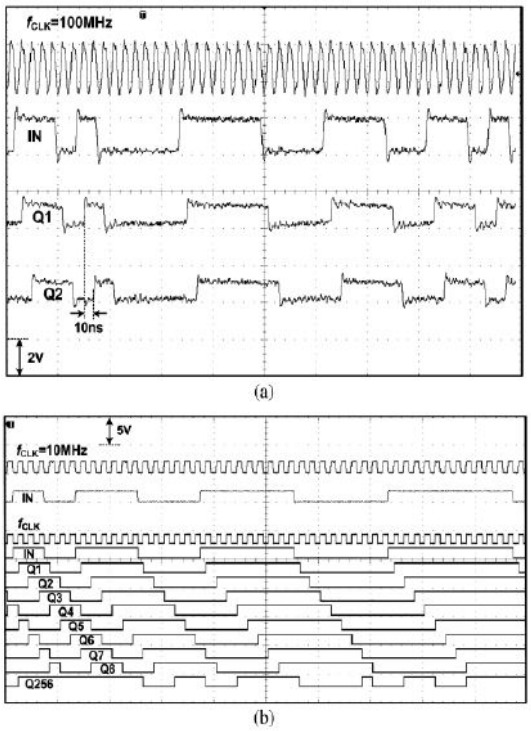

Fig.5. Measured waveforms of the proposed shift-register at (a) *f*CLK=100MHz; (b) *f*CLK=10MHz

Type of pulsed latch	SSASPL
Word length of shift register (N)	256
Word length of sub shift registers (K)	4
Total number of pulsed latches	320
Area	6,600μm^2
Power @ f_{CLK}=100MHz	1.2mW
Max. Clock frequency	840MHz @ sim. 100MHz @ meas.

Table I. Features of the Shift Register Chip

V. CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches.

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