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Volume 06, Issue 04,Page No: 1147 – 1156.
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NOVEL THREE PHASE CASCADED MULTILEVEL INVERTER WITH REDUCED SWITCH COUNT

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ABSTRACT
the demand for high power rating machines has been increasing in the industries for the last decade. To meet this requirement, multilevel inverter topology is developed and became popular due its own advantages. Even though, there are different types of multilevel inverter topologies, cascaded H-Bridge (CHB) type got its existence. With this cascaded H-Bridge, we could able to get more number of levels in the output voltage with less total harmonic distortion (THD). But, the major drawback of this CHB is, it requires more number of switches to get more levels. Therefore, a new basic unit is proposed to get same number of levels with less number of switches. Using proposed topology, we could able to get 15 level output voltage with two basic units consisting of 16 switches and seven DC voltage sources. In this paper, the proposed topology is modified to increase the voltage levels without increasing the number of switches and voltage sources. The number of levels has been enhanced to 21 by using asymmetrical configuration. The three phase multilevel inverter is developed with new topology and the output is fed to 3-phase induction motor, the performance characteristics are also analyzed. The total circuit configuration is developed and results are analyzed using Matlab/Simulink software.

Keywords: Multilevel inverter cascaded H-Bridge inverter, Symmetrical, Asymmetrical, Induction motor.

1. INTRODUCTION

In the industries, the applications like mills, laminators, conveyors, fans and pumps etc require high power and medium voltage. Such a high power applications the multilevel inverter (MLI) [2-3]topology is extending the usage because of its own advantages. The conventional square wave inverter produces more harmonics and in multilevel inverter the output voltage wave shape is nearly sinusoidal with number of levels. The advantages of multilevel inverter are listed below.

1. The stress of the motor is reduced and protects the motor against damage.
2. Multilevel inverters draw the current from source with less distortion.
3. These can operate at high as well as lower frequencies.
4. The total harmonic distortion (THD)[4-6] is less in the output voltage wave form without using any filter.

Owing to these advantages different types of multilevel inverters are introduced in to the market such as diode clamped type, flying capacitor type and cascaded multilevel inverter. The diode clamped and flying capacitor type multilevel inverters need more number of diodes and capacitors? So, most commonly used topology is the cascade H-Bridge inverter topology. The number of levels can be increased by increasing the number of H-Bridges by using the formula number of levels= 2n+1. Here, n is the number of H-Bridges. In CHB also there are two configurations like symmetrical [7] and asymmetrical [8]. When the magnitude of dc

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voltage source is same in each bridge, then that configuration is called symmetrical and if the magnitude of dc voltage source is not equal it is called as asymmetrical configuration. For the same number of bridges, the asymmetrical configuration gives more levels as compared to symmetrical configuration. The series-parallel connection of voltage sources in each bridge is also developed to get the more voltage levels.

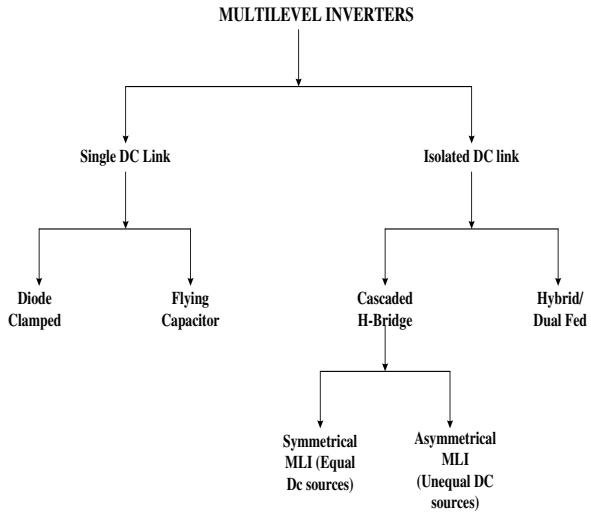

Fig.1. Classification of multilevel Inverters.

However, in order to get more levels the number of H-Bridges has to be added in the circuit which causes to increase the number of switch count. Further, the cost, size and number of gate driver circuits increases. To overcome this drawback, in this paper it is proposed a new multilevel inverter with reduced switch count. This topology is developed in both symmetrical and asymmetrical configuration. The circuit models for CHB [8-11] and proposed topology are modelled in both symmetrical and asymmetrical configuration for 15 and 21 levels of output voltage. The results are analyzed and compared. With the proposed inverter topology, the MLI fed induction motor drive is also modelled and the performance characteristics are analyzed. All the circuit modelling and result analysis is carried out by using Matlab/Simulink platform.

2. Conventional Cascaded H-Bridge MLI

The cascaded H-bridge multilevel Inverter uses separate dc sources (SDCSs). The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from either batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. Again, the cascaded multilevel inverters are classified depending the type of DC sources used throughout the input.

2.1 Symmetrical 5 level CHB inverter:

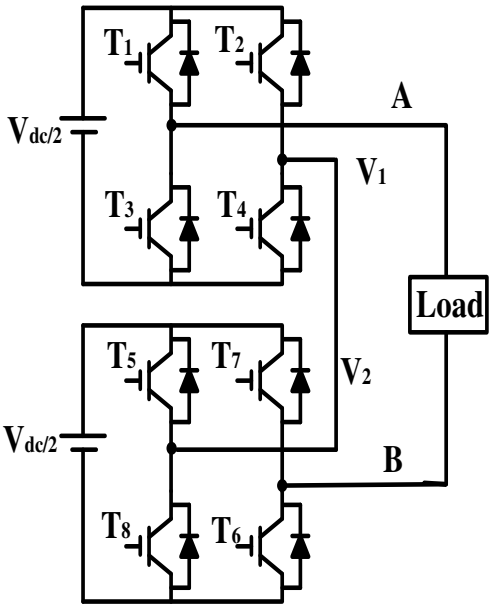

Fig. 2.1 Symmetrical 5 level CHB inverter.

The 5 level cascaded H-Bridge inverter with symmetrical configuration is shown in fig. 2.1. Here, the DC voltage is divided in to two voltage sources as Vdc/2 each and applied as an input for each bridge. In this symmetrical configuration we can get maximum of five levels (Vice, Vdc/2, 0, -Vdc/2,-Vdc) with two bridges. As each bridge requires four switches, the total switches for the configuration is 8.

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2.2 Asymmetrical 7 level CHB inverter:

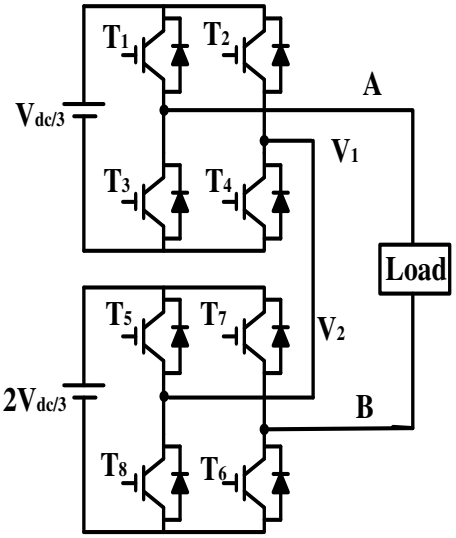

Fig. 2.2 Asymmetrical 7 level CHB inverter.

Fig. 2.2 shows the asymmetrical cascaded H-Bridge inverter topology for 7 level. In this topology, the number of H-bridges used is two, which is same as in case of symmetrical 5 level CHB inverter. But, the dc voltage source for each bridge is not same in magnitude. The first H-Bridge has the voltage source of Vdc/3 and another H-Bridge has the voltage source of 2Vdc/3. We could able to get seven levels with two H-Bridges because of asymmetrical configuration

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3. PROPOSED TOPOLOGY

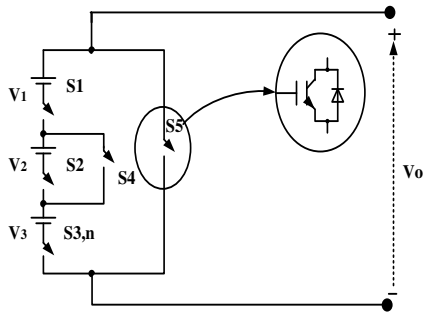

Fig.3.1. Proposed Basic unit.

TABLE I
PERMITTED TURN ON AND OFF STATES FOR SWITCHES IN THE PROPOSED BASIC UNIT

state	Switches state					Vo
	S_1	S_2	S_3	S_4	S_5	
1	off	off	off	off	**on**	0
2	**on**	off	**on**	**on**	off	V_1+V_3
3	**on**	**on**	**on**	off	off	$V_1+V_2+V_3$

Fig.3.1. shows the proposed basic unit. As shown in Fig.3.1. The proposed basic unit is comprised of three voltage sources and five unidirectional power switches. In proposed structure, power switches (S_2,S_4), (S_1,S_3,S_4,S_5), and (S_1,S_2,S_3,S_5) should not be simultaneously turned on to prevent the short circuit. The turn on and off states of the power switches are shown in TABLE I, the proposed basic unit is able to generate three different levels of 0, V_1+V_3, and $V_1+V_2+V_3$ at the output.

It is possible to connect n number of basic units in series. This inverter is able to generate all voltage levels except V_1, Therefore it is necessary to use an additional Dc voltage source with the amplitude of V_1 and two unidirectional switches are connected in series with the proposed basic unit.

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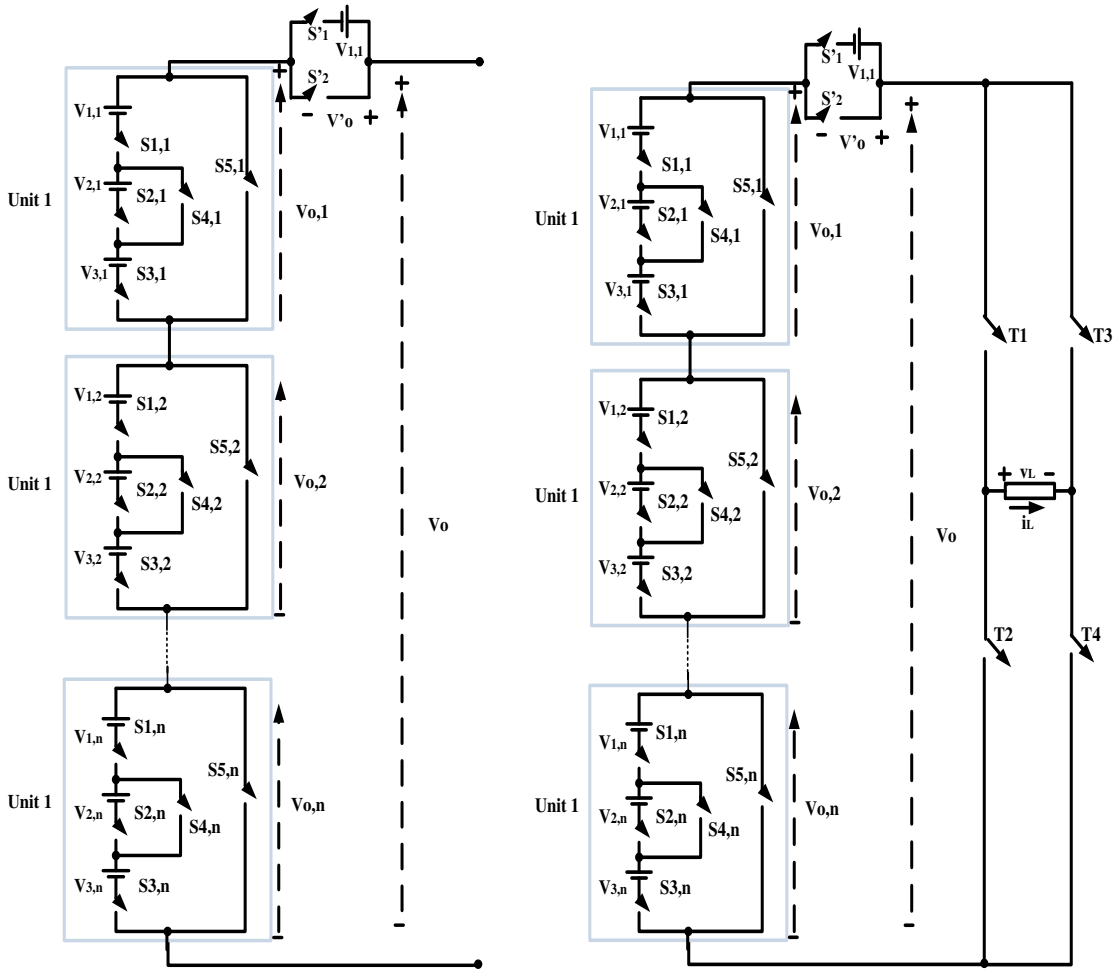

Fig.3.2. Cascaded multilevel Inverter. (a) proposed topology. (b) Developed Proposed topology.

The proposed cascaded inverter that is able to generate all levels is shown in Fig.3.2 (a). Power switches $S_1^{|}$, $S_2^{|}$ and V_1 have been used to produce lowest output level. The amplitude of $V_1=V_{dc}$ and the output voltage level of each unit is indicated by $v_{0,1}, v_{0,2}, \ldots, v_{0,n}$, and $v_0^{|}$. The output voltage level $v_0^{|}$ of the proposed cascaded multilevel inverter is equal to

$$v_0(t) = v_{0,}1(t) + v_{0,}2(t) + \cdots + v_{0,}n(t) + v'_0(t).(1)$$

The generated output voltage levels of the proposed inverter are shown in Table II. According to Table II, the proposed inverter that is shown in Fig.3.2(a) is only able to generate positive levels at the output. Therefore, an H-bridge with four switches T_1-T_4 is added to the proposed topology. This inverter is called the developed cascaded multilevel inverter and is shown in Fig.3.2(b). If switches T_1 and T_4 are turned on, load voltage v_1 is equal to v_0, and if power switches T_2 and T_3 are turned on, the load voltage will be $-v_0$. For the proposed inverter, the number of switches N_{Switch} and the number of dc voltage sources $N_{sources}$ are given by the following equations, respectively,

$$N_{swtich}=5n+6 \quad (2)$$

$$N_{source}=3n+1 \quad (3)$$

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Where n is the number of series connected basic units. As the unidirectional power switches are used in the proposed cascaded multilevel inverter, the number of power switches is equal to the number of IGBTs, power diodes, and driver circuits.

The other main parameter in calculating the cost of the inverter is the maximum amount of blocked voltage by the switches. If the value of the blocked voltage by the switch are reduced, the total cost of the inverter decreases [11]. In addition, this value has the most important effect in selecting the semiconductor devices because this value determines the voltage rating of the required power devices

TABLE II
GENERATED OUTPUT VOLTAGE LEVELS v_0 BASED ON THE OFF AND ON STATES OF POWER SWITCHES

v_o	S'_1	S'_2	$S_{1,1}$	$S_{2,1}$	$S_{3,1}$	$S_{4,1}$	$S_{5,1}$	$S_{1,2}$	$S_{2,2}$	$S_{3,2}$	$S_{4,2}$	$S_{5,2}$	⋯	$S_{1,n}$	$S_{2,n}$	$S_{3,n}$	$S_{4,n}$	$S_{5,n}$
0	off	on	off	off	off	off	on	off	off	off	off	on	⋯	off	off	off	off	on
V_1	on	off	off	off	off	off	on	off	off	off	off	on	⋯	off	off	off	off	on
$V_{1,1}+V_{3,1}$	off	on	on	off	on	on	off	off	off	off	off	on	⋯	off	off	off	off	on
$V_{1,1}+V_{2,1}+V_{3,1}$	off	on	on	on	on	off	off	off	off	off	off	on	⋯	off	off	off	off	on
$V_{1,2}+V_{3,2}$	off	on	off	off	off	off	on	on	off	on	on	off	⋯	off	off	off	off	on
$V_{1,2}+V_{2,2}+V_{3,2}$	off	on	off	off	off	off	on	on	on	on	off	off	⋯	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,3}$	off	on	on	on	on	off	off	on	off	on	on	off	⋯	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,2}+V_{2,3}$	off	on	on	on	on	off	off	on	on	on	off	off	⋯	off	off	off	off	on
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	off	on	on	on	on	off	off	on	on	on	off	off	⋯	off	off	off	off	on
$V_{1,1}+\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	on	off	on	on	on	off	off	on	on	on	off	off	⋯	off	off	off	off	on

TABLE III
PROPOSED ALGORITHMS AND THEIR RELATED PARAMETERS

Proposed algorithm	Magnitude of dc voltage sources	N Level	Vomax	Vblock
First proposed algorithm(P1)	$V_{1,j}=V_{2,j}=V_{3,j}=V_{dc}$ $forj=1,2,\dots,n$	6n+3	(3n+1)V_{dc}	(2ln+6)V_{dc}
Second proposed algorithm(P1)	$V_{1,l}=V_{2,l}=V_{3,l}=V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=2V_{dc}$ $forj=2,3,\dots,n$	12n-3	(6n-2)V_{dc}	(40n-13)V_{dc}
Third proposed algorithm(P3)	$V_{1,l}=V_{2,l}=V_{3,l}=V_{dc}$ $V_{1,j}=\frac{1}{3}V_{2,j}=V_{3,j}$ $=3^{j-2}V_{dc}$ $forj=2,3,\dots,n$	$5((3^{n-1})+4$	$\left[\frac{5(3^{n-1})+3}{2}\right]V_d$	$[82(3^{n-1})-7]V_{dc}$
Fourth proposed algorithm(P4)	$V_{1,j}=0.5V_{2,j}=V_{3,j}$ $=2^{j-1}V_{dc}$ For j=1,2,…,n	$(2^{n+3}-5$	$(2^{n+2}-3)V_{dc}$	$[7(2^{n+2})-22]V_{dc}$

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In order to calculate the blocking voltage, it is necessary to consider the amount of the blocked voltage by each of the switches. According to Fig.3.2(b), the values of the blocked voltage by switches are equal to

$$V_{s'1} = V_{s'2} = V_{1,1} \quad (4)$$

$$V_{s1,j} = V_{s3,j} = \frac{V_{s1,j}+V_{s2,j}+V_{s3,j}}{2} \quad (5)$$

$$V_{s4,j} = V_{s2,j} + V_{2,j} \quad (6)$$

$$V_{s5,j} = V_{1,j} + V_{2,j} + V_{3,j} \quad (7)$$

$$V_{T1} = V_{T2} = V_{T3} = V_{T4} = V_{o,max} \quad (8)$$

Where $V_{0,max}$ is the maximum amplitude of the producible output voltage. Therefore, the maximum amount of the blocked voltage in the proposed inverter V_{block} is equal to

$$V_{block} = \sum_{j=1}^{n} V_{block,j} + V'_{block} + V_{block,H} . \quad (9)$$

In (9), $V_{block,j}$, V'_{block}, and $V_{block,H}$ indicate the blocked voltage by the jth basic unit, the additional dc voltage sources, and the used H-bridge, respectively.

3.1Proposed Symmetrical 15-level MLI:

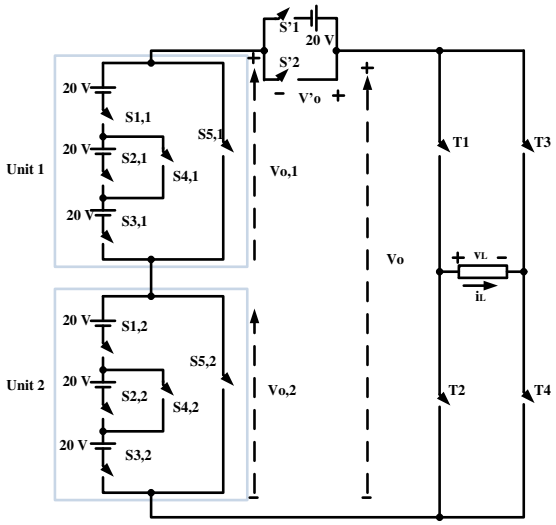

Fig.3.3. Symmetrical 15-level MLI based on the proposed basic unit.

The proposed 15-level inverter shown in Fig.3.3, uses Sixteen power switches and seven dc voltage sources to generate a step waveform with 15-levels and a maximum amplitude of 140 V. In Fig.3.3. There is two basic units connected in series has the same magnitude of dc voltage sources so it is called

In the developed inverter, the number and maximum amplitude of the generated output levels are based on the value of the used dc voltage sources

Therefore, four different algorithms are proposed to determine the magnitude of the dc voltage sources. These proposed algorithms and all their parameters are calculated and shown in Table III.

According to the fact that the magnitudes of all proposed algorithms except the first algorithm are different, the proposed cascaded multilevel inverter based on these algorithms is considered an asymmetrical cascaded multilevel inverter. In addition, based on the equations of the maximum output levels and its maximum amplitude, it is clear that these values in the asymmetrical cascaded multilevel inverter are more than those in the symmetrical cascaded multilevel inverters with the same number of used dc voltage sources and power switches.

symmetrical multilevel inverter. Using proper switching sequence the proposed circuit generates 15-levels output voltage.

In this inverter, power switches S1| and S2| and dc voltage source V1 have been used to produce the lowest output voltage level. The amplitude of this dc voltage source is V1=Vdc. Fig.3.3.generates peak voltage of 140V and each step voltage is 20v.

3.2. Proposed Asymmetrical 21-level MLI:

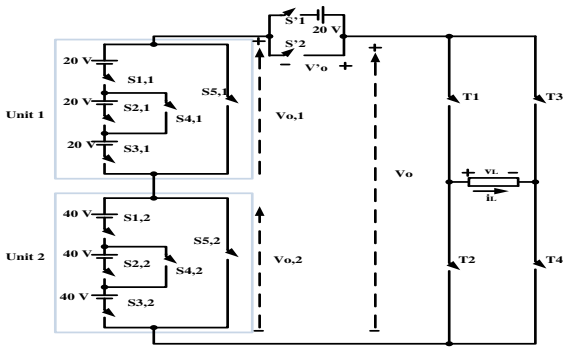

Fig.3.4. Asymmetrical 21-level MLI based on proposed basic unit.

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The Proposed 21-level inverter shown in Fig.3.4, uses same number of power switches as a 15-level proposed inverter but only the change is increasing the magnitude of dc voltage sources in unit 2 of the cascaded multilevel inverter as per the proposed algorithm. Fig.3.4. generates a step waveform of 21-levels with an amplitude voltage of 200V, there are two basic units connected in series having different magnitudes of dc voltage sources so this type of inverter is called as asymmetrical multilevel inverter. Using proper switching sequence the proposed inverter generates 21-level output voltage.

3. MULTILEVEL INVERTER FED INDUCTION MOTOR DRIVE

The proposed multilevel inverter output is applied to an induction motor drive and the performance characteristics are analysed.

4.1. Proposed 21-level Inverter fed Induction Motor Drive:

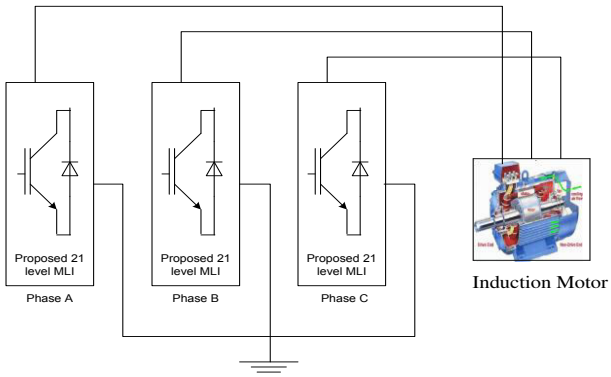

Fig.4.1.Proposed 21 level Inverter fed Induction Motor Drive.

The circuit configuration for 21 level (proposed Asymmetrical) inverter fed induction motor drive is shown in fig. 4.1. Here, each Phase (i.e. Phase A, Phase B, Phase C)represents an individual single phase 21- level inverter as shown in Fig.3.4 and these three modulated with a definite time gap of 120^0 phase displacement each other to obtain three phase output. The three phase output is connected to induction motor, the specifications of motor are given in Table IV

TABLE IV
Specifications of Induction Motor Drive

S.No	PARAMETERS	VALUES
1	Nominal Power	10KW
2	Voltage(Line-Line)	400 V
3	Frequency	50 HZ
4	No of Poles	4
5	Stator Resistance	2.9 Ohms
6	Rotor Resistance	2.2 Ohms
7	Inertia	0.02 Kg-m^2

4. MATLAB/SIMULINK RESULTS

The following Fig.5.1.&Fig.5.2. shows the MAT lab/Simulink model of proposed 15-level MLI and its output waveform.

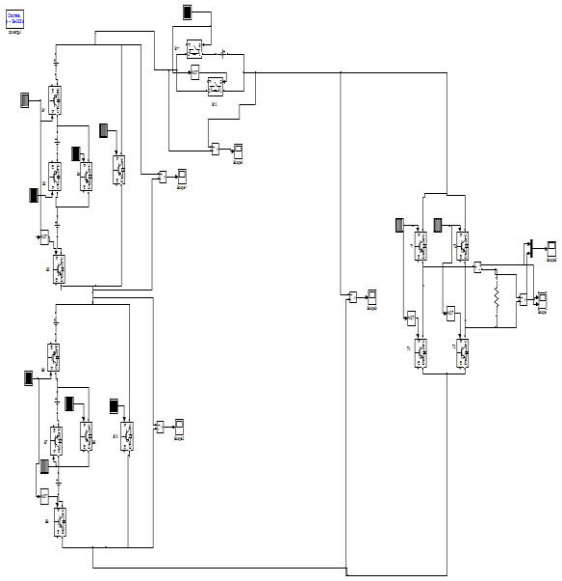

Fig.5.1. MAT lab/Simulink model of 15-level MLI.

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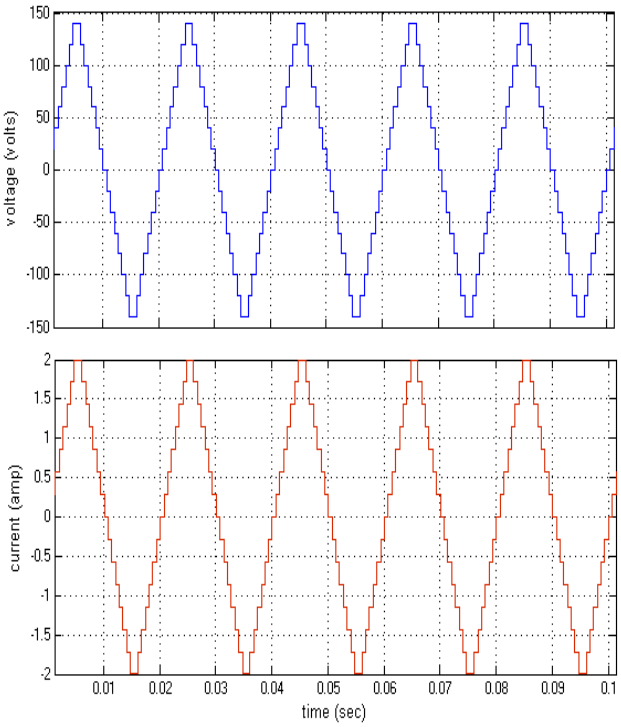

Fig.5.2.15-level inverter output voltage & current.

From Fig.5.2.it is observed that the output voltage of proposed MLI has 15-levels, the output peak voltage V_{max} is 140V and each step voltage is 20V. Fig.9. shows the spectrum analysis of 15-level MLI. From Fig.5.3. THD of proposed 15-level inverter is 13.30%.

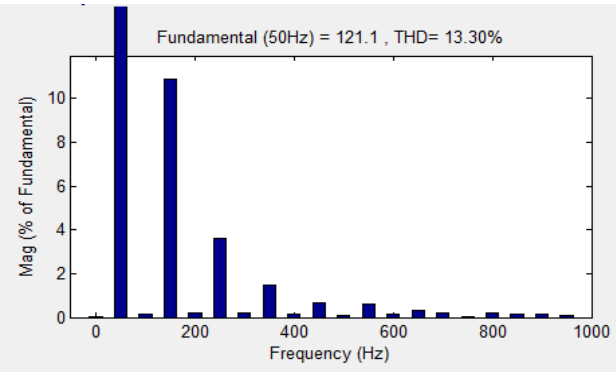

Fig.5.3. THD of proposed 15-level inverter.

The following Fig.5.4 & Fig.5.5 shows the MAT lab/Simulink model of Proposed 21-level MLI and its output waveforms.

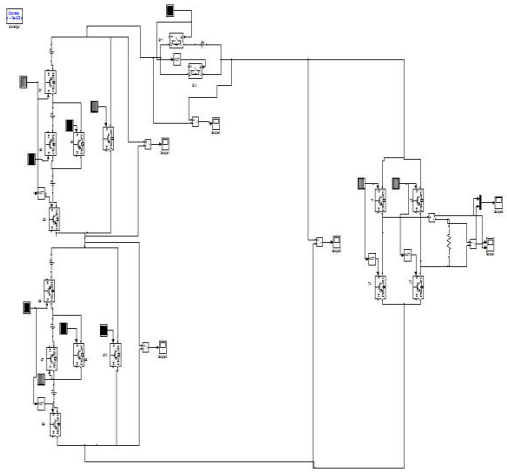

Fig.5.4. MAT lab/Simulink model of 21-level inverter.

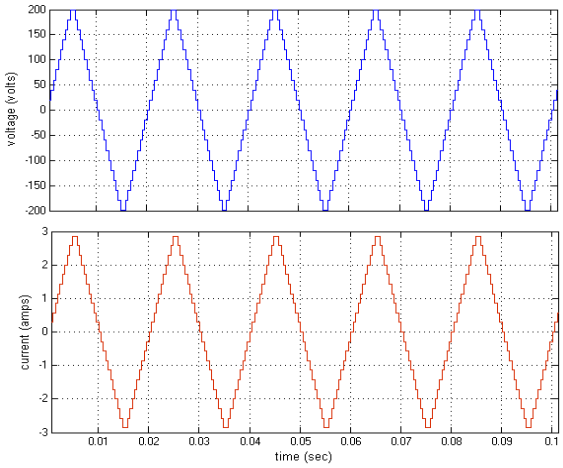

Fig.5.5. 21-level inverter output voltage & current.

From Fig.5.5.it is observed that the output voltage of proposed MLI 21-levels, output peak voltage V_{max} is 200V and each step voltage is 20V. Fig.5.6. shows the spectrum analysis of 21-level MLI. From Fig.5.6. THD of proposed 21-level inverter is 12.85%.

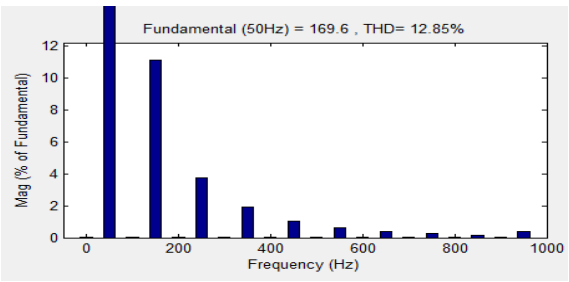

Fig.5.6. THD of proposed 21-level inverter.

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The following Fig.5.7. Shows MAT lab/Simulink model of proposed three phase 21-level multilevel inverter connected to Induction Motor Drive.

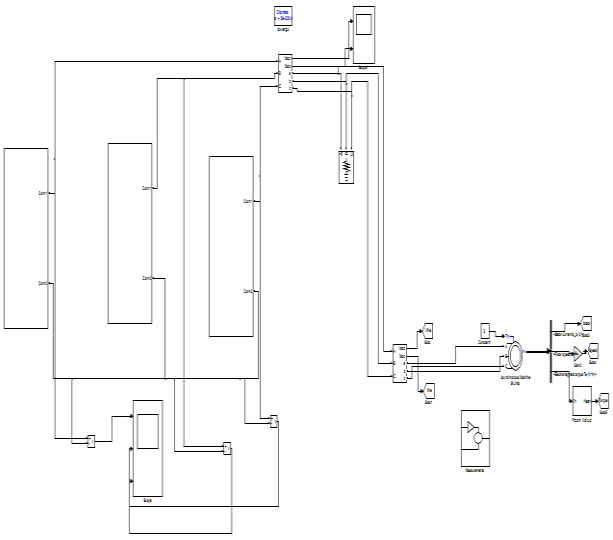

Fig.5.7.Simulink model of proposed 21-level inverter
Fed induction motor.

In above Fig.5.7 each subsystem block (i.e. subsystem A, sub system B and sub system C) represents an individual single phase 21-level inverter as shown in Fig.5.4 and these three modulated with a definite time gap of

120^0 phase displacement each other to obtain three phase output. The three phase output is connected to induction motor.

The following Fig.5.8.shows the output voltage and current waveforms of proposed three phase 21-level MLI

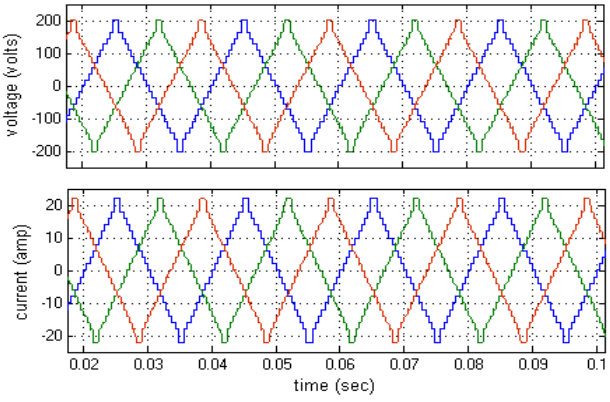

Fig.5.8. Three phase output voltage and currents.

The output peak voltage is V_{max}=200V and each stepping voltage is 20V, similarly the output peak current of 22 amps are observed.

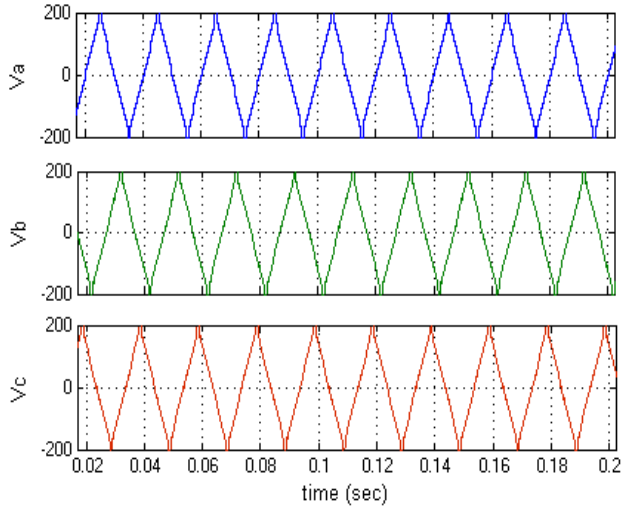

Fig.5.9.Individual phase voltages.

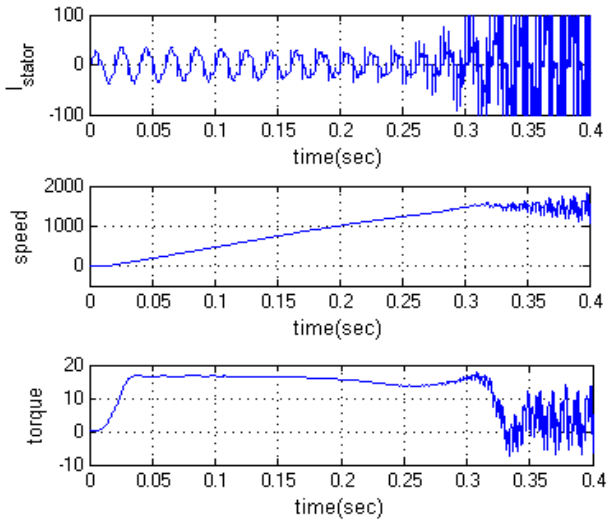

Fig.5.10. Stator current, speed and Torque.

The performance characteristics of induction motor like torque, speed and stator current are shown in fig. 5.10.

TABLE V
Comparison of Proposed Topology

Proposed MLI	Number of levels	Number of Switches	% THD
Symmetrical MLI	15	16	13.30
Asymmetrical MLI	21	16	12.85

5. CONCLUSION

In conclusion, it is strongly confirmed that the proposed topology could get more number of levels with reduced power switches.. The proposed Basic unit is only able to generate positive levels at the output. Therefore, In order to generate all voltage levels (positive and negative) an H-Bridge is added to the proposed topology. This inverter is called developed cascaded multilevel inverter. The proposed inverter has the advantage of reducing the number of power switches and gate drive circuits compared with conventional multilevel inverter. Therefore, the developed proposed inverter has better performance and needs minimum number of power electronic devices that lead to reduction in the installation space and cost of the inverter. Also, the conversion efficiency of the converter increases because of less number of switches. The circuits are modelled and results are displayed. The operation and performance of the proposed multilevel inverter is proved by connecting an induction motor as a load. The stator current, speed and torque characteristics of induction motor are analyzed for proposed Twenty one level inverter topology. The total harmonic distortion is also compared for proposed symmetrical and asymmetrical type MLI.

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