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AN EFFICIENT VLSI ARCHITECTURE FOR THE MODIFIED CONVOLUTIVE BLIND SOURCE SEPARATION

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ABSTRACT

This will presents an efficient Very Large Scale Integration (VLSI) design for Convolutive Blind Source Separation (CBSS). Information maximization (Infomax) approach is adopted for CBSS network. CBSS chip design mainly includes Infomax filtering modules and scaling factor computation modules. In an Infomax filtering module, filtering of input samples are done by Infomax filter with the weights updated by Infomax driven stochastic learning rules. And for scaling factor computation module all operations are implemented by the circuit design based on a piecewise-linear approximation scheme. An efficient and high performance and less delayed blind source separation technique is described.

Key Words- Convolutive Blind Source Separation (CBSS), Infomax, Scaling factor

1. INTRODUCTION

Blind source separation (BSS) is a statistical signal processing method which aims to extract source signals from their observed mixtures, assuming almost no a priori information about the characteristics of the sources or the mixing environment. The only assumption about the source signals is that they are statistically mutually independent. Early BSS algorithms tried to solve the problem exclusively in the time-domain. In realistic environments, one must adapt fairly long separating filters to adequately separate the observed mixtures. Because of this, time-domain approaches converge very slowly, especially when dealing with colored signals. Moreover, many of these algorithms were originally developed to separate i.i.d signals. When applied to colored signals, these methods could not distinguish between time correlations and spatial correlations of the observed signals. As a result, recovered signals have flattened spectra compared to the source signals. Besides, these algorithms have extreme computational complexities. To alleviate the problems of the time-domain and the frequency-domain algorithms, some researches proposed to tackle the BSS problem in the sub band-domain [3, 7, 9, 13]. By use of a reasonable number of sub bands and separating filters of appropriate length in each sub band, the effects of long reverberations can be properly covered. Using shorter separating filters in sub bands and whiter signals to adapt them, the convergence rate is increased considerably. Moreover, applying a time-domain BSS algorithm in each sub band, the permutation problem is avoided within sub bands. Although the permutation problem might occur between sub bands, due to the existence of more information in each subband compared to the frequency-domain algorithms, it is much easier to mitigate the permutation problem [3]. Since the sub bands often heavily overlap in the frequency-domain, likelihood of permutation problem between sub bands greatly decreases. Our extended experiments with sub band-based BSS algorithms also confirm this. Moreover, whiter signals are used in sub band-based methods to adapt separating filters, and the whitening artifact of the time-domain algorithms arises independently in each sub band. Thus, the whitening distortion yields less overall artifacts in the recovered signals. Blind source separation is a kind of a filtering process used to separate different sources from the mixed signals in which most of the information about sources and mixed signals is not known. This restriction makes the blind source separation a challenging task. Blind source separation becomes a very important research topics in a lot of fields such as audio signal processing, biomedical signal processing, communication systems and image processing. Simple version of mixing process is one in which without filtering effect instantaneous mixing occurs. Convolutive mixing process should be done for the audio source passing through a filtering environment before arriving at the microphones and in order to recover the original audio source convoluted blind source separation should be done. One of the conventional methods is Independent component analysis (ICA) which is used to solve the CBSS problem. Major drawback of software implementation using this technique is often highly computational intensive and more time consuming process. Providing hardware solutions for ICA-based blind source separation has drawn considerable attention because of the hardware solution achieves optimal parallelism. An analog BSS

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chip can be designed using above-and–sub threshold CMOS circuit techniques which integrates an i/o interface of analog, weight coefficients and adoption blocks

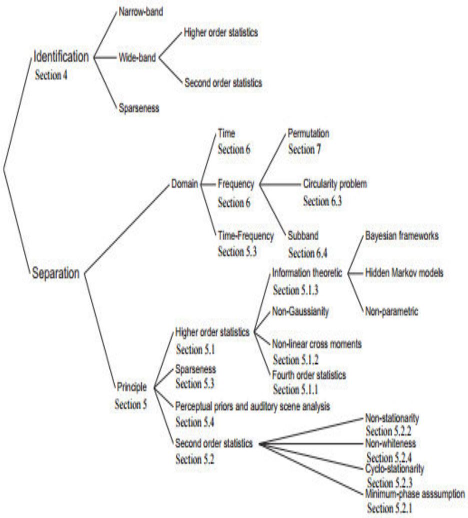

FIG 1: Overview of important areas within blind separation of convolutive sources.

2. PROPOSED VLSI BLIND SOURCE SEPARATOR

The proposed CBSS system is shown in the FIG.2. The CBSS chip mainly consists of two functional cores: Infomax filtering module and scaling factor computation module. Additionally, the Infomax filtering outputs are added with the help of two small carry-save adders (CSAs). The current prototype chip is used for two sources and two sensors by utilizing four Infomax filtering modules along with two scaling factor computation modules.

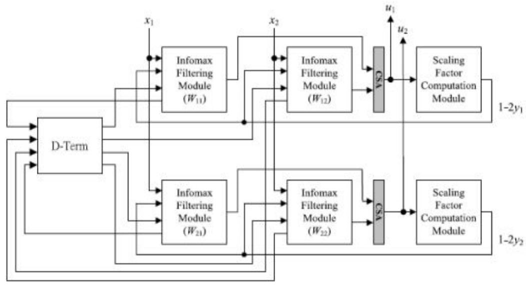

FIG 2: The block diagram of a proposed CBSS system.

3. INFOMAX FILTERING MODULE

The Infomax filtering module for the proposed system is shown in fig.3. In the fig. 1, the CBSS separation network contains four causal FIR filters. These filters are adaptive because stochastic learning rules which are derived from the Infomax approach will alter the tap coefficients and are thus referred to herein as the Infomax adaptive filter or the Infomax filter. The Infomax filtering module is exemplified with six taps. In the Infomax filtering module, an input sample passes through lower and upper register chains. These samples are multiplied with filter weights and scaling factors, respectively. The multiplication results of all of the taps are accumulated by a two-stage summation. The first stage adopts carry look ahead adders to generate the intermediate addition results for multiplication of every two successive taps. The above intermediate addition results are summed up by using a carry save addition

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scheme. A CSA(carry save adder) can accept more than two data inputs.

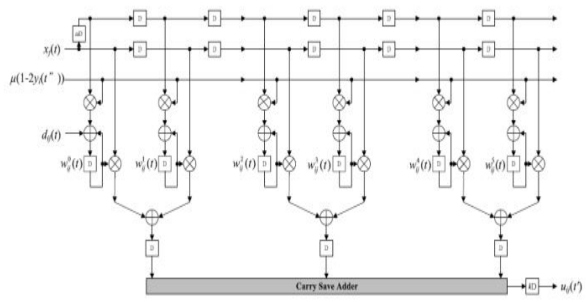

FIG 3: Infomax filtering module.

4. SCALING FACTOR COMPUTATION MODULE

Fig.4 describes the proposed circuit for the scaling factor computation module. The linear equation evaluation with input ui(t) and ai and bi are equation parameters and are implemented using a multiplier and an adder. In order to choose corresponding ai and bi, a line segment has to be selected by two multipliers. The scaling factor is calculated by using the formula s(t) = 1 − 2y(t), where y(t) = (1+e -u(t)) -1. If y(t) is known, −2y(t) can be generated first using 2's complement and a left shift to y(t). The scaling factor s(t) is then obtained by adding −2y(t) and one. The above procedure is simple. The scaling factor commutation is approximated directly rather than performing logistic sigmoid computation first and then calculating 1 − 2y(t).

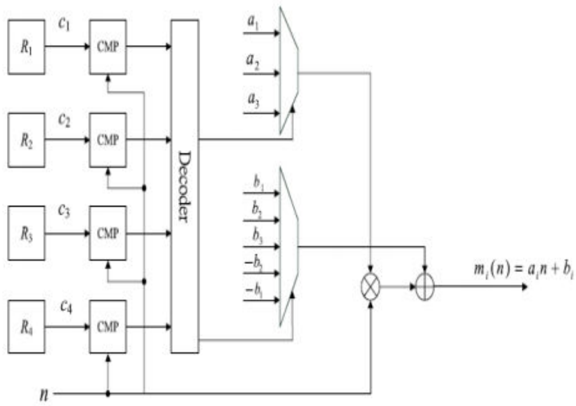

FIG 4: SCALING FACTOR COMPUTATION MODULE

To implement the line-segment approximation, the circuit design for scaling factor computation is to calculate single variable linear equations. For the equation of lsi which corresponding to mi(n) = ai n + bi, i = 1, 2, . . . , 5, where n = ui(t). As the slopes of ls1 and ls5 are the same, these two line segments share the equation parameters a1. In the same manner, line segments ls2 and ls4 share the equation parameters a2. Furthermore, according to the symmetry in Fig. 5, the bias used for line segment ls5, e.g., −b1, is the negative of the bias b1 used for line segment ls1. In addition, line segments ls4 and ls2 use biases −b2 and b2, respectively .As for the d0 ij(t) , this study designs a Dterm unit to execute dij(t) = cofactor(wij)(detW0) -1. The architecture of the D-term unit is shown in Fig. 6. The Dterm unit consists of a determinant circuit to find. Or to obtain the detW0 and in order to

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generate the inverse of detW0, lookup table is used. Since W is a 2 × 2 matrix, the cofactors(wij) are w22, −w21, −w12, and w11, which are multiplied by (detW0) -1 in parallel using four multipliers.

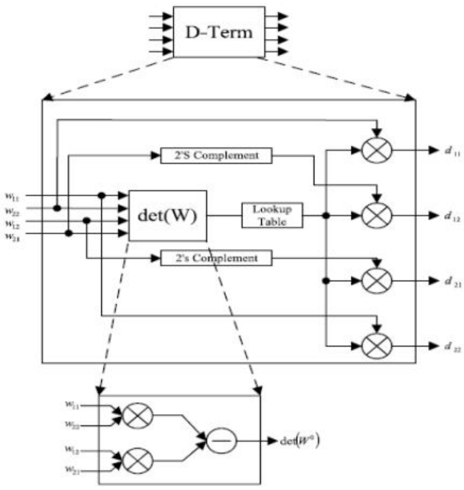

FIG 5: Architecture of a D-term unit

5. SIMULATION WAVEFORM

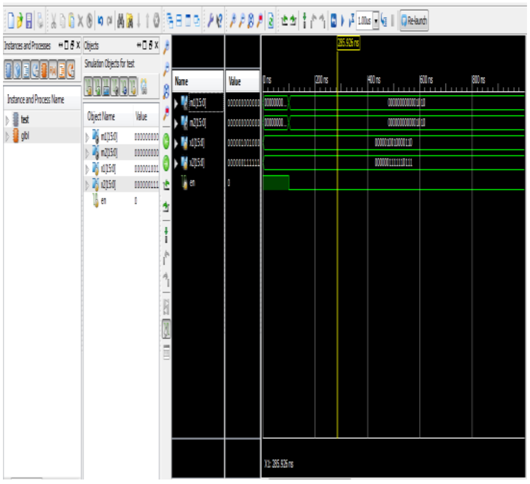

FIG 6: simulation result for the proposed system

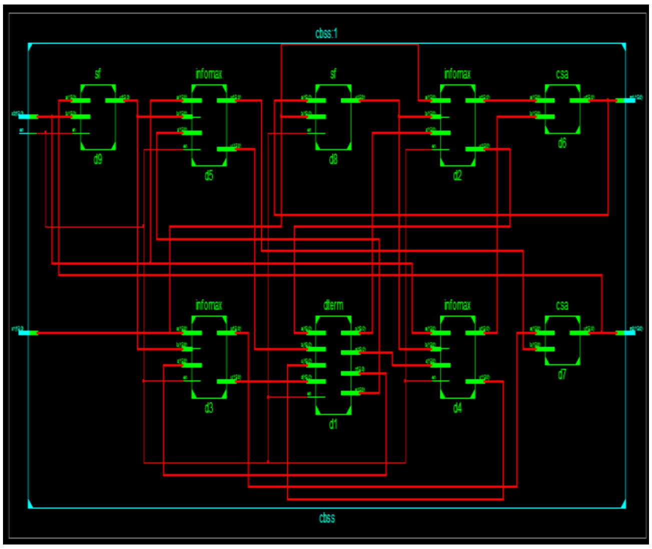

FIG 7: RTL schematic view for the proposed system

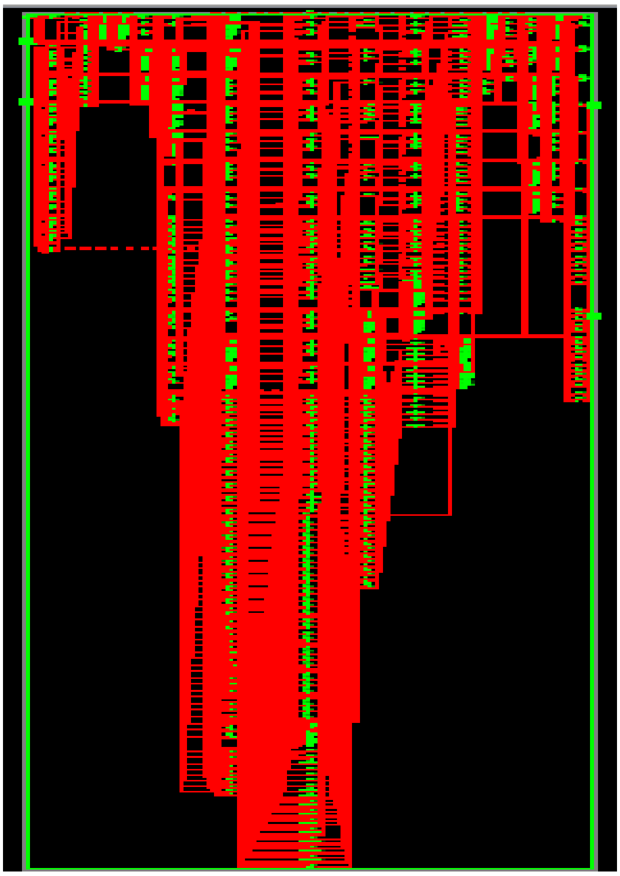

FIG 8: Technology schematic view for the proposed system

6. CONCLUSION

An efficient VLSI architecture design for CBSS with less delay has been presented in this paper. The architecture mainly consists of Infomax filtering modules and scaling factor computation modules and a D-term. CBSS separation network derived from the Infomax approach. The proposed system has high performance and has less delay as compared with the other existing system. By the usage of vedic multiplier in Infomax filter increases the speed as well as performance of the proposed system.

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