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Design Of Low Power Consumption Of 8 Bit Multiplier Using Ns Gate

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ABSTRACT

Increasing demand for reduction in power dissipation in digital computer system has leads to new mode of computation for digital design giving birth to reversible computing. Its main aim is low power dissipation in logical elements but can have some other advantages likeerror preventionand data security. In present-day, reversible logic has bring out to be an optimistic computing model having applications in low power CMOS, nanotechnology, quantum computing and DNA computing.. The main focus of this study involves two primary design implementations. First one reversible gate design and second one multiplier design using reversible gates. Here in this manuscript we implementeda8*8 reversible gate design called "NSG". The total project is implemented in Xilinx 14.7 ISE with Spartan 3E family.

Keywords: Reversibility, NSG, Constant Input, Garbage Output, ALU.

I. INTRODUCTION

Energy loss is a very important factor in modern VLSI design. Irreversible hardware computation results in energy dissipation due to information loss. R.Landauer has shown that for irreversible logic computations, each bit of information lost generated KTln2 joules of heat energy, where K is Boltzmann's constant and T is the temperature at which computation performed. Reversible logic circuit does not have loss of information and reversible computation in a system can be performed only when the system consists of reversible gates. C.H.Bennetshowed that KTln2 energy dissipation would not occur if the computation is carried out in a reversible way. Reversible logic is very crucial for the construction of low power, low loss computational designs which are very essential for the design process of arithmetic circuits used in quantum computation, Nano-technology and other low power digital circuits. Lately, quite a few researchers have been paying their attention on the design, simulation and synthesis of proficient reversible logic circuits. The vital reversible gates [3] used for reversible logic synthesis are Feynman Gate and Fredkin gate [3,4].

Fig 1.1 Block Diagram of Feynman Gate

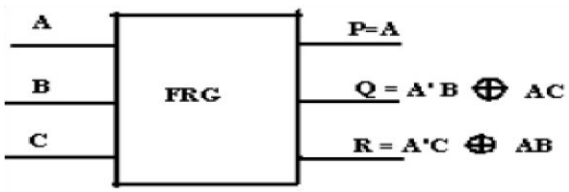

Fig 1.2 Block Diagram of Fredkin Gate

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Reversible logic is emergent and drawing attention in the recent past due to its uniqueness i.e. less heat dissipating characteristics. It has been proved that any Boolean function can be implemented using reversible gates. The NS Gate [5] i.e. "NSG" can singly be implemented in all logical Boolean operations. Reversible logic has publicized possibilities to have widespread purpose in upcoming emerging promising technologies such as quantum computing, optical computing, quantum dot cellular automata in addition to ultra-low power VLSI circuits, DNA computing to generate zero power rakishness under ideal conditions.

In Proposed system, there exists a design of multiplier and adder units by number of reversible gates. In This design, we are using only one reversible gate called NSG gate. By using this gate number of operations will be performed by only single gate and the garbage outputs also minimized. In this paper, we are also proposed a 8-bit MAC unit. MAC unit is an inevitable component in many digital signal processing (DSP) applications involving multiplications and/or accumulations. MAC unit is used for high performance digital signal processing systems. The DSP applications include filtering, convolution, and inner products. Most of digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transforms (DWT).

Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire calculation. The multiplier and adder unit will be designed by NSG gate and accumulator unit will be designed by using Sayem gate [6], Feynman gate and Fredkin gate.

The simulation output is verified using Xilinx ISE 13.2 and the model graph results verified using Modelsim software.

II.8-Bit Mac Unit Using Conventional Multiplier

A MAC unit consists of a multiplier and an accumulator containing the sum of the previous successive products. The MAC inputs are obtained from the memory location and given to the multiplier block. The design consists of 8 bit modified multiplier, 16 bit ripple carry adder and a shift register. The Multiplier-Accumulator (MAC) operation is the key operation not only in DSP applications but also in multimedia information processing and various other applications.

In above MAC unit, we are using the conventional multiplier. The conventional multiplier of width N x N bits will generate the N number of partial products. The partial products are generated by bit wise AND in one multiplier bit with another multiplier. Hence, the N x N bit multiplier uses 2Nmultiplications and N-Adders in the architecture of Conventional multiplier.

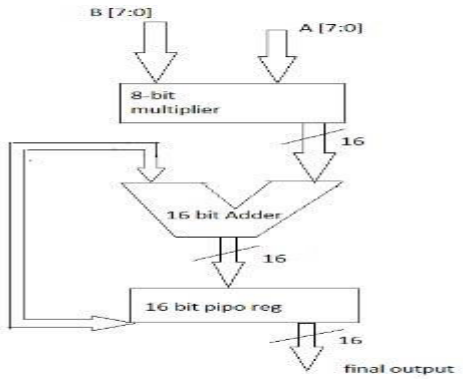

Fig 2.1 Multiplier Block Diagram

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III. PROPOSED DESIGN

In this paper, a 4 * 4 one through reversible gate called NS gate "NSG" is projected. The proposed reversible NSG gate is shown in Figure.3.1. The corresponding truth table of the gate is shown in Table I. It can be established from the Truth Table that the input pattern analogous to a particular output pattern can be exclusively determined [5]. The invented NSG gate can perceive all Boolean logical operators. The input d, c, b and a are termed as input terminal 1, 2, 3 and 4 respectively and the output are termed as output 1, output 2, output3 and output 4 respectively from first to last of the paper.

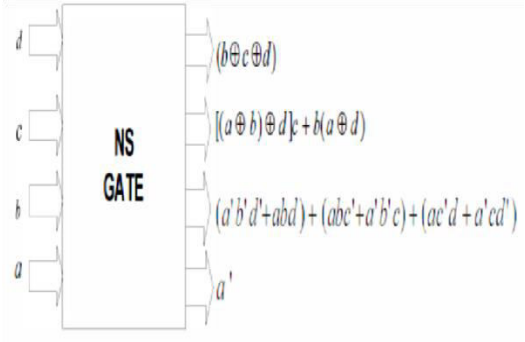

Fig 3.1 Reversible NS Gate

As mentioned above, MAC unit consist of multiplier, adder and register/accumulator. In this paper, we used 8 bit modified Reversible NS multiplier. The MAC inputs are obtained from the memory location and given to the multiplier block. This will be useful in 8 bit digital signal processor. The input which is being fed from the memory location is 8 bit.

Since the bits are huge and also ripple carryadder produces all the output values in parallel, PIPO register is used where the input bits are taken in parallel and output is taken in parallel. The output of the accumulator register is taken out or fed back as one of the input to the ripple carry adder. The above figure 2.1 shows [8] the basic architecture of MAC unit. The figures 3.2 shows the 8X8 NS multiplier.

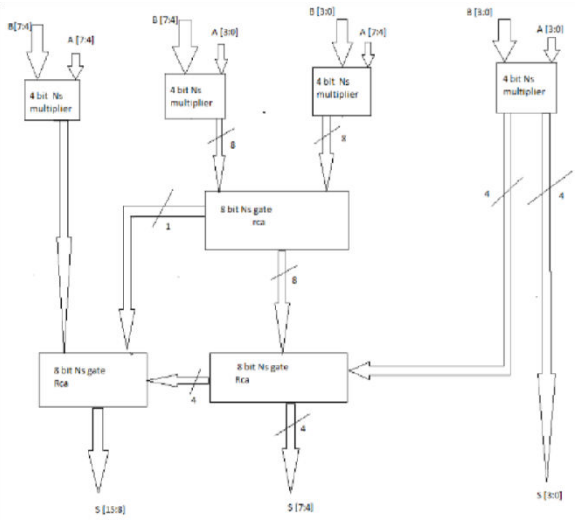

Fig 3.2 Multiplier architecture

IV. Results

The Reversible MAC unit simulated and synthesized using the Xilinx Design Suit14.7 with device family as spartan3E and device Xc3s100e5vq100. The simulation Results are verified by using ISIM simulator i.e. given the input values are multiplier of a = 00110011 (51) and b = 00011110 (30) and get the final output is final_out = 0000101111110100 (3060). The Figure 4.1 shows the model graph of Reversible MAC unit and Table I shows the comparison of conventional and Reversible MAC units. In the below table-I observe the number of (Look Up Tables) LUT's used in the

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general MAC unit is 214 which is higher than that of Reversible MAC unit. Here area occupied by the General MAC unit is higher than that of Reversible MAC unit. In reversible Mac unit, the multiplier we used was designed by using only one reversible gate called as NS gate. So area occupied by reversible multiplier is low when comparing with normal multiplier used in general MAC unit. And also the delay produced by general Mac unit is very high when comparing with Reversible MAC unit.

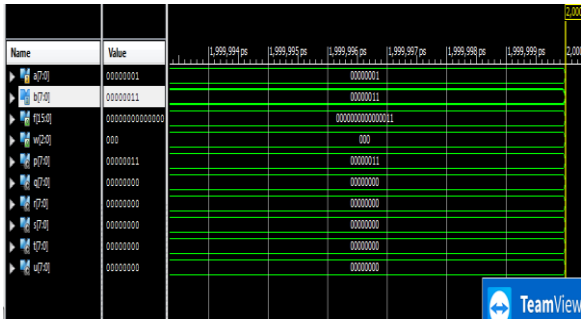

Fig 4.1 Simulation Results of Reversible MAC unit

Architecture	LUT's	Area (%)	Delay (ns)
General Mac Unit (8 – bit)	714	41	46.286
Reversible Mac Unit (8 – bit)	155	29	22.607

Table I Comparison of Delay and area for Conventional and Reversible MAC units

V. CONCLUSION

Reversible multiplier can be designed with the different logical designs purposed in conventional combinational and sequential logic with the aim to improve the performance of computational units. To improve the performance, the main measures in designing an efficient reversible logic multiplier are: Number of gates, Number of garbage outputs, Number of ancillary inputs. Finally reversible logic gates are occupied less area and delay because it has a many to many input and output relations. so by using of these gates we can design any large circuits with less components and it is the main advantage of reversible logic gates.

Future scope: we may extend this to 16*16 multiplier using 4*4 NS gate. It can be implementing by using other reversible gates for D.S.P applications.

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