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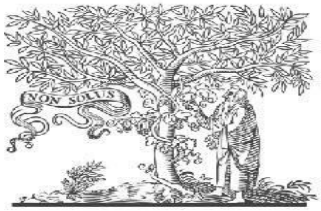

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D-Latch-Based Modified Low-Power and Area-Efficient Carry Select Adder

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Abstract— The Carry Select Adder (CSLA) is one of the quick adders used in many computer systems for quickly performing mathematical calculations. The employment of mathematical units that are not just quicker but smaller and lower power is required by the quickly growing mobile sector. When creating the enhanced CSLA architecture, the Converter from Binary to Excess-1 (BEC) was utilised. In place of the BEC, this study proposes a useful method that makes use of a D latch. In terms of power, latency and area, experimental study shows that the suggested architecture offers triple benefits.

Keywords— Low Power, Area Efficient, CSLA, and BEC

I. Introduction

Building high-speed data route logic systems[1] that are both power and area efficient is one of the most crucial study areas in VLSI system design. The time it takes a carry to go through an adder limits the pace of addition in digital adders. In an elementary adder, each bit location's Only when the sum and a carry have been transferred into the following bit position from the previous bit position is sum created sequentially. In multiple computational systems, the CSLA is used to independently generate several carries before choosing one of them to produce the sum. A compromise between the ripple carry adder's (RCA) smaller area and longer delay and the carry look-ahead adder's larger area and shorter delay is provided by the[2] carry-select adder (CSLA). The carry inputs Cin=0 and Cin=1 are taken into consideration when using several pairs of ripple carry adders (RCA) to construct partial sum and carry in the CSLA algorithm. The final total is then selected and carried by multiplexers. The redesigned CSLA using BEC has a minor increase in delay with a reduction in area and power consumption. The suggested architecture's fundamental concept is to replace the BEC with a D latch and an enable signal. The area, latency, and power are reduced by the suggested architecture. Following is the organizational structure of this work; section III details the structure and operation of the binary to excess-1 converter logic. Sections IV and V,[3] respectively, provide explanations of the standard and modified CSLAs. Section VI discusses the intended architecture. The report's seventh section analyses the findings. Section

II. Literature Survey

Low-power and space-efficient carry-select adder, IEEE Trans. Very Large Scale Integrated (VLSI) Syst., vol. 20, no. 2, February 2012, pp. 371-375. Ramkumar, B., and Kittur, H. M. They proposed a layout where a BEC-1 block known as the binary to recess one converter would substitute for the ripple carry block in a conventional CSLA layout. The basic idea behind this effort is to use BEC rather than RCA because BEC-1 takes up less room and uses less power than a traditional CSLA. Utilizing a binary to excess one converter is the intended alternative to using RCA with carry equal to one. There is a flaw in this project that will make it take longer than current procedures.

[2] Yajun. He, C. H. Chang, and J. Gu's article, "An area-efficient 64-bit square root carry select adder for low power application," was published in Proc. IEEE Int. Symp. Circuits Syst. in 2005. They gave information on a brand-new, space-effective square root CSL technique based on the first zero detection logic. The adder is divided into several groups using a carry-select adder, and each group does two additions simultaneously. As a result, the carry assessment blocks in each chosen step are two ripple-carry adders. When analyzing the carry chain, the block carry-in is assumed to be zero in one copy and one in the other copy.

[3] Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng published An Area- In the Proceedings of the International Multi Conference of Engineers, Efficient Carry Select Adder Design by Sharing the Common Boolean Logic Term and

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Computer Scientists 2012 Vol II, IMECS 2012, March 14–16, 2012, Hong Kong. They proposed an area-efficient carry select adder by using a common boolean logic term. In the conventional carry select adder after boolean simplification, they can get rid of the redundant adder cells. The carry-out and sum signals are instead repeated in each cell of the single-bit adder.

III. BEC

To decrease the size and power consumption of traditional CSLA, BEC is utilized in place of the RCA with Cin=1. The n-bit RCA is replaced with an n+1 bit BEC. Figure 1 and Table 1 each display the function table for a 4-b BEC. BEC logic allows us to greatly reduce the silicon area reduction in the VLSI design. The 3-bit BEC's corresponding Boolean equations are listed below.

S0=B0, B1=B0, B1, and S2=B2 are equal to B0 and B1, respectively.

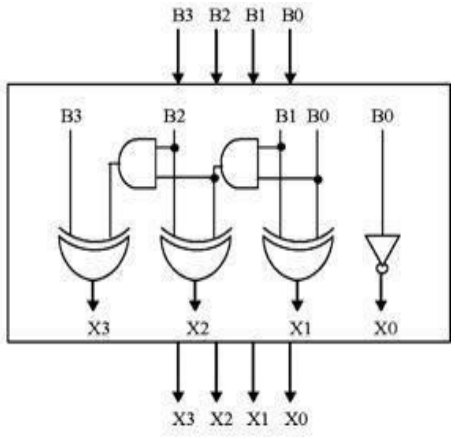

Fig. 1 4-Bit BEC

TABLE. FUNCTION TABLE OF 4-BIT BEC

B[3:0]	X{3:0}
1111	0000
1110 - - -	1111 - - -
0001	0010
0000	0001

IV. SQRT REGULAR CSLA

Figure 5 depicts the 16-b standard SQRT CSLA's structure. It includes five RCA groups of various sizes. Fig. 2 displays the delay and area evaluation for each group, with the delay values denoted by the numbers within []. The actual determined values of the output carry and total are chosen using the carry out calculated from the final step, or least significant bit stage. A multiplexer is employed in the selection process. Fig. 3 depicts the internal organization of group 2 of the standard 16-bit CSLA. By hand counting, there are 57 gates (full adder, half adder, and multiplexer) utilized in group 2. The mux receives two RCA inputs, one with Cin=0 and the other with Cin=1. Two sets of 2-b RCA are present in group 2. Selection input c1 arrives at 6:3 mux at the time (t) = 7, which is before s3 (t = 8) and after s2 (t = 6) respectively. As a result, Summation of c1 and mux is sum2 [t = 10], while sum3 [t = 11] is the summation of s3 and mux [t = 3].

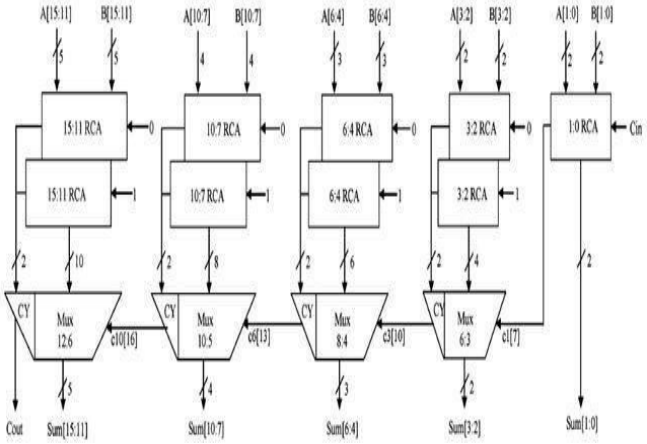

Fig.2 Regular 16-bit SQRT CSLA

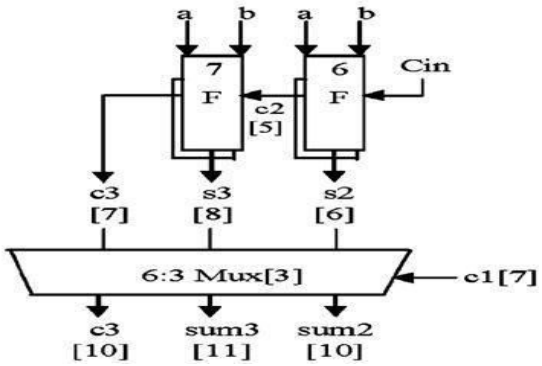

Fig.3 Group 2

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V.MODIFIED CSLA USING BEC

Fig. 4 depicts the topology of the 16-b SQRT CSLA that has been suggested, employing BEC for RCA with Cin=1 to maximize space and power. We divided the structure into five groups once more. Fig. 5 displays the delay and area estimation for each group 2 participant. The RCA with Cin=0 provides one input to the mux, and the BEC provides the other. It is evident from a comparison of group 2 of both standard and modified CSLA that the BEC structure reduces area and power. However, the BEC technique has the drawback of having a longer delay than the standard CSLA.

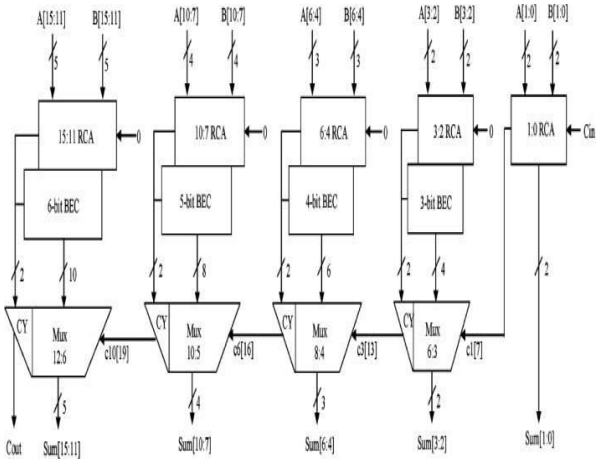

Fig 4:CSLA using BEC

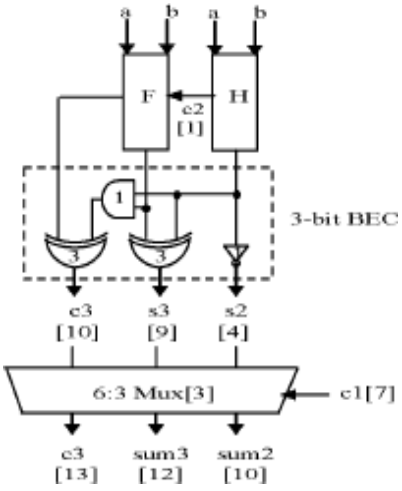

Fig. 5 Group II

VI.MODIFIED 16-BIT CSLA USING D-LATCH

With this technique, a D-latch and an enable signal replace the BEC and add one circuit. One piece of data is stored via latches. Their outputs are continuously influenced by their inputs as long as the enable signal is asserted. In other words, when they're activated, their content instantly adapts to user input. The D-latch and its waveforms are seen in Figures 6 and 7.

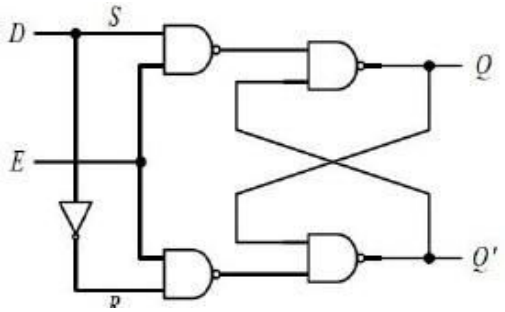

Fig6: Gates

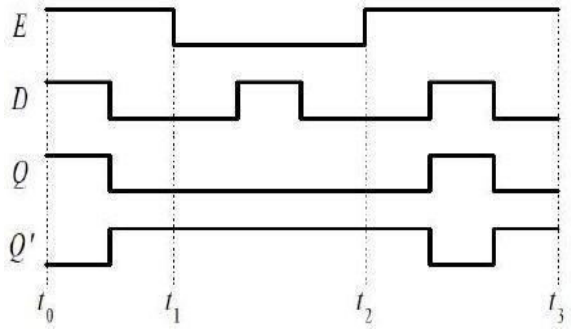

Fig 7: Input and output Waveforms

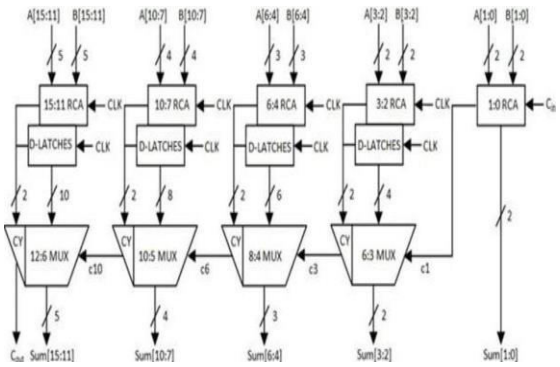

Fig8: Modified CLSA Using D-LATCH

It displays the group 2 internal structure of the suggested 16-bit CSLA. The two-bit addition was carried out by group 2 using the pairs a2 and b2, a3, and b3. This is done by the two full adders (FA), FA2 and FA3, in turn.

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The carry output from FA2 serves as the third input to the full adder FA2, and the clock serves as the third input to the full adder FA3. Five D-Latches make up the group 2 structure, four of which is used to store carry, while the fifth is used to store the sum2 and sum3 from FA2 and FA3, respectively. The real total and carry are chosen using a multiplexer based on the carry from the previous stage. The 2:1 multiplexer and the 6:3 multiplexer are combined a2 and b2 are added with a carry of 0, when the clock is low. Due to the low clock, the initial D-Latch is not enabled. Using an inverted clock enable, the second D-Latch stores the sum when cosine equals 0. The addition is performed with a carry of 1 when the clock is ticking quickly. The total of the other enabled D-Latches that the store carry for carry is one. Whether c1 had a value of 0 or 1 determined the real sum and carry the multiplexer would use.

VII.SIMULATION RESULTS

A. Waveforms

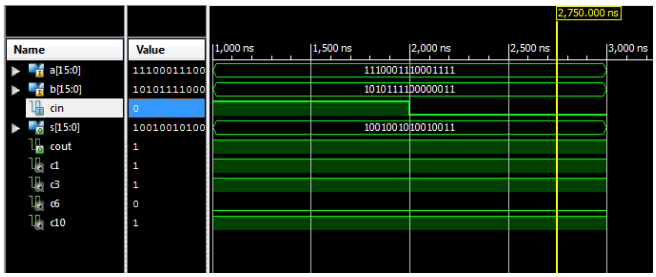

Fig.9 Regular SQRT CSLA Simulation

Fig.10 D-Latch-enhanced modified CSLA

B. Power Report

2.3. Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Quiescent
Supply Power (mW)	1710.63	1654.98	55.65

Power Supply Currents

Supply Source	Supply Voltage	Total Current (mA)	Dynamic Current (mA)	Quiescent Current (mA)
Vccint	1.200	37.60	15.18	22.42
Vccaux	2.500	43.90	33.90	10.00
Vcco25	2.500	622.30	620.80	1.50

Fig .11 Power report of Regular SQRT CSLA

2.3. Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Quiescent
Supply Power (mW)	874.37	827.49	46.88

Power Supply Currents

Supply Source	Supply Voltage	Total Current (mA)	Dynamic Current (mA)	Quiescent Current (mA)
Vccint	1.200	22.70	7.59	15.11
Vccaux	2.500	26.95	16.95	10.00
Vcco25	2.500	311.90	310.40	1.50

Figure.12, Regular SQRT CSLA Power Report

2.3. Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Quiescent
Supply Power (mW)	324.21	281.48	42.73

Power Supply Currents

Supply Source	Supply Voltage	Total Current (mA)	Dynamic Current (mA)	Quiescent Current (mA)
Vccint	1.200	246.22	234.57	11.65
Vccaux	2.500	10.00	0.00	10.00
Vcco25	2.500	1.50	0.00	1.50

Fig. 13. Modified CSLA power report utilizing D-Latch

TABLE III

COMPARISON

(16-bit) Adder	Delay(ns)	Power(mW)	PDP(x10^-12)
SQRT Regular CSLA	21.07	1715.42	34411.2
CSLA using BEC	21.678	882.37	18684.64
Modified CSLA using D-Latch	17.09	324.21	5783.90

VII.CONCLUSION

This study suggests a straightforward method for reducing the size and power of SQRT CSLA architecture. This work's fewer gates have a significant benefit in terms of reduced area and overall power (Table II). By using a Binary to Excess-1 converter, In comparison to a standard CSLA, the modified CSLA reduces area and power while increasing latency. By utilizing D-latches, the technique proposed in this research reduces delay, area, and power compared to normal and modified CSLA.

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