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TERNARY SRAM EFFICIENCY AND HIGH PERFORMANCE

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Abstract In every application static random access memory is used for high speed register , cache and relatively small memory banks such as a frame buffer in the increased demand of SRAM with large use in system on-chip . It stores information in the form of binary values due to this reason it require more number of cells. Nowadays, ternary logic is popularly used and It is the best substitute for traditional binary logic because of its storage capacity and delay that results from reduced degree of complexity in interconnects and chip area. This project proposes the design of standard ternary inverter , by arranging ternary standard inverters back to back a Trit storage element is implemented as a ternary SRAM cell and continuous read operation is obtained by Transmission gate technology . We measure the performance by considering the parameters area , delay and power . Tanner T- spice based circuit simulation of the proposed designs were carried out , Simulation result demonstrates an increased performance of area and delay for the Proposed design as compared to the existing design.

Keywords Ternary logic , STI , SRAM , Transmission gate technology.

1. Introduction :

Multi valued logic circuit's have a great deal of effectiveness for upgrading today's Very large scale integration circuit design [1]. Those systems can hold information more than binary systems.Ternary memory cell offers a superior than binary memory in terms of storage capacity, which provides advantages such as lower costs and faster access.

Static random access memory architecture is a major Challenge for wireless applications and implantable devices [1], [2], with working the frequencies that vary from a several hundreds of KHZ to tens of megahertz [3]. This is due to SRAM's substantial contribution towards the System-on-Chip (SoC) , using around 70 percent of the total area , which might be expanded in the coming years [4].

Because of loss in write ability / read stability, the standard 6T cell ceases to operate in the near and sub-threshold area [6]. For a successful write - operation, It preferred to utilise a Wide-access transistor , this may have an impact on stability of read operation. In terms of data stability during write and read operations, this is a trade-off. Researcher's exhibited a variety of cells that avoid the read-write integrity trade off . The aforementioned concept , such [7-17] cells , Focus on segregating read and write ports by dividing the Routes for reading and writing, allowing operation to be improved individually. However , they can be sensitive to current leakage , require a huge area and use a Single ended read technique, which reduces Sensitivity to reading . To overcome the intricacy of the Single ended read method, several strategies [5]

increasing port for differential reading by incorporating more number of transistors but at the expense of extra area were adopted.

2 Literature Survey

N.Maroof et al .[4] : A unique Static random access memory of 10 transistors per a cell containing Decoupled Single ended read bitline (RBL) and a 4-T readport was proposed for leakage reduction and Efficient power behaviour . The read bitline is Precharged at 50% the supply voltage of the cell and is permitted to charge as well as discharge in accordance with the stored data bit. During the read operation, inverter powered through the additional data node (QB) links the RBL through a transmission gate to the virtual power lines. For a read 1, Read bitline rises towards the VDD and falls towards the Ground for a read 0. During write as well as hold modes the value of virtual power lines is the same. as the Read bitline pre-charging level and In the read operation they are linked to proper levels of supply. Read bitline leakage is greatly reduced when virtual rails are managed dynamically. In a realistic 65 nm technology, the suggested 10T cell is 2.47 times size of the 6T with β is 2 , provides Read static noise margin of 2.3 , and reduces 50% of read power consumption . As in comparison to 6T BL leakage, Read bitline leakage is less than three orders of Magnitude smaller, and (ION / IOFF) is significantly upgraded . 6T and 10T have similar total leakage characteristics, resulting in competitive performance.

T.-H.Kim et al.[7] : A Voltage scalable the value of 0.26 Volt , 64 kilobyte SRAM of 8T having 512 cells / bit line has been demonstrated with 130nm CMOS Technology. The Reverse short channel effect is used in the design of an SRAM cell to improve Read performance and Write Margin of cell without the use of the External Peripheral circuit's. The Marginal Bit line Leakage Compensation (MBLC) system substitutes for leakage current of the bit line, which acts as equivalent at subthreshold supply voltages to a read current. The Marginal bitline leakage compensation lowers Vsub to 0.26 Volts and Precharged read bitlines are no longer required. Leakage power consumption is reduced by floating point read and write bitline approach. AStandby leakage power consumption lowers by deep sleep mode While continuing to Hold mode cell integrity . Ultimately, after a read operation is concluded, an automatic circuit for controlling the pulse width of a wordline analyses PVT transitions and switches off the bit line current leakage.

Jayashree H V et al .[8] **:** This study describes the Ternary CMOS-SRAM design and performance verification. Ternary Static RAM is manufactured in 180 nm, 90 nm, and 6 5nm technology processes. Ternary cells are made up of 2 cross coupled Ternary inverters. TSPICE is used to conduct read , write operations on the Ternary memory cell using Sense Amplifiers, Fast Decoders and Tritline Conditioning circuits . Because Fast Decoders employ less transistors than traditional Decoders, the suggested technology can be used for Low Power Applications. The 65 nm technology array module consumes power of 0.608 mW and has resulted in a data access time of about 9.88 ns.

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Punnam Nagaraju et al.[11] : This study describes the designs and modelling of CMOS ternary SRAM cells and ternary logic gates using Very Large Scale Integration (VLSI). The 180nm technology is used to create the Simple ternary inverter, Negative ternary inverter and Positive ternary inverter .Ternary NAND , NOR gates are constructed and simulated as well. Cross coupled ternary inverters make form a ternary SRAM. SPICE simulations confirmed that the READ and WRITE functionalities work correctly.

3 Existing Design

Static Random Access Memory is the form of semi conductor memory stores each bit using bistable latching circuitry. The notion of Static RAM distinguishes from the Dynamic memory, which must be renewed on a periodic schedule . Although static RAM may store data, it is nevertheless in the volatile conceptual perception that data is lost , when the memory switch is flipped off.

In numerous applications, the area is critical. The presently available SRAM cell [12] enhances stability at the price of larger area owing to the higher number of transistors.

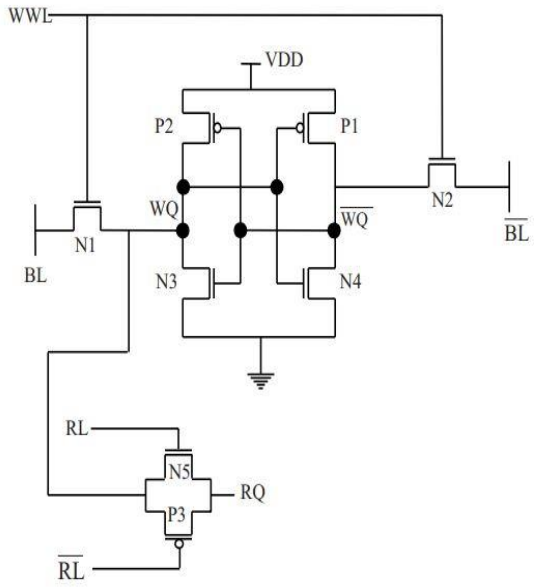

Fig 1 : Existing SRAM cell

4 Proposed design

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Multi valued circuits has high potential for improving the storage capacity than binary memory.Ternary circuits were implemented by Standard ternary inverter (STI) , Negative ternary inverter (NTI) ,Positive ternary inverter (PTI) .

In the developed Ternary memory component , standard ternary inverter used as basic functional building block.

TABLE 1 : Ternary Logic Symbols

Voltage-levels	Logic-values
0	0
0.5 * vdd	1
vdd	2

There are 3 levels in ternary logic 0,1,2.

4.1 standard ternary inverter

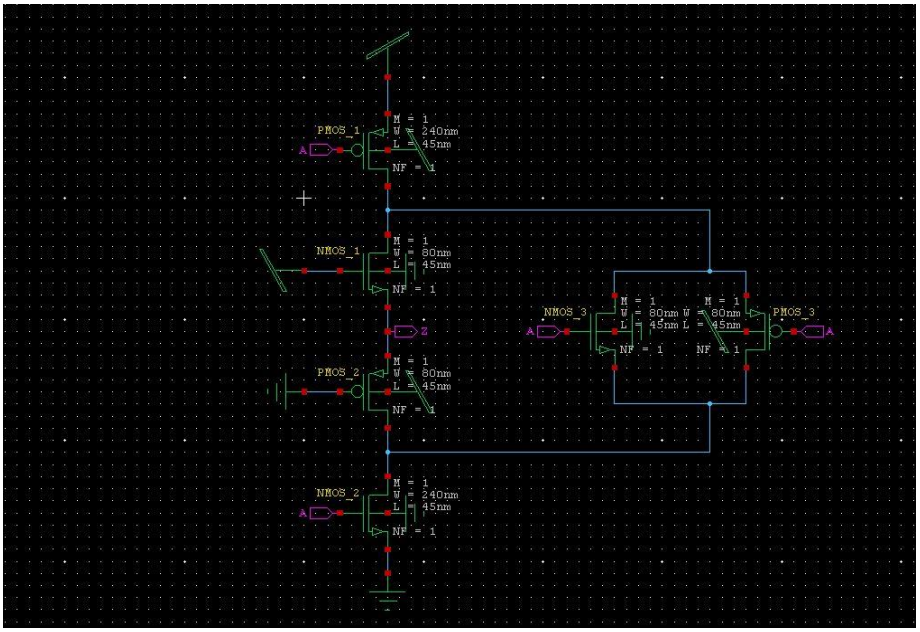

Fig 2a : standard Ternary inverter

Table 2 : Truthtable of STI

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Input A	Z (STI output)
0	2
1	1
2	0

The standard Ternary inverter is the primary form of ternary inverter. It produces the output 2, 1, 0 for the inputs 0 , 1, 2. STI is utilised to be the significant component for the Proposed Static RAM cell as a result of its capability to produce 1 at the output. We get ternary storage element by incorporating the STI back to back.

4.2 Ternary SRAM Cell

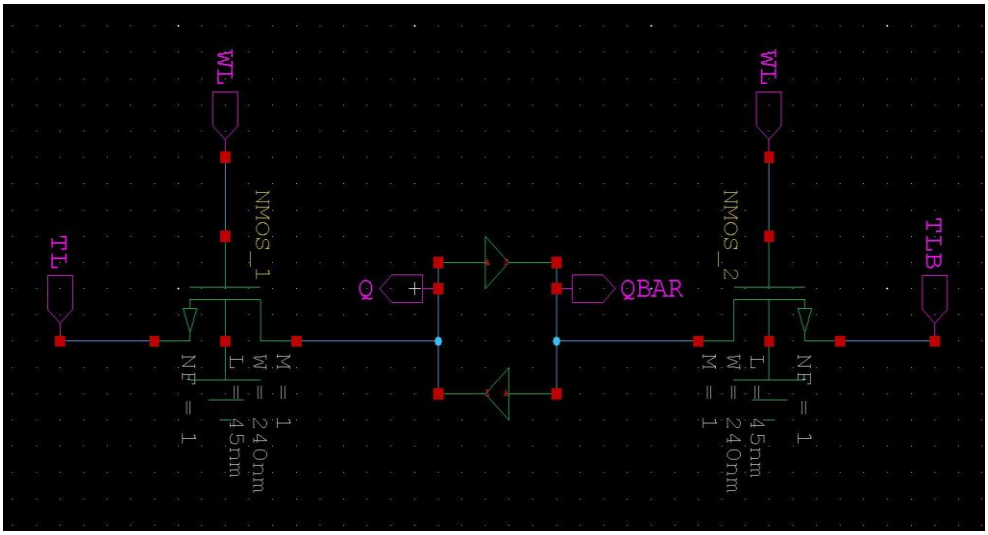

Fig 2b : Ternary SRAM Cell

Table 3 Truth Table of SRAM Cell

OPERATIONS	WL	TL	TLB	Q	QB
Write	2	0/1/2	2/1/0	0/1/2	2/1/0
Read	2	2	2	0/1/2	2/1/0
Hold	0	X	X	NC	NC

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This cell is read/write through the tritline and is triggered by lifting the wordline. The wordline indicates that it is able to read or write to the cell. The Ternary SRAM behaviour has been split into two phases: READ and WRITE.

In the Write operation : The tritline TL corresponds to the data to be saved. The wordline is then activated, storing the data in the cell. When the WL is set to high, the data at the TL is passed to Q by means of access transistors.

In the read operation : Initially TL and TLB both are kept at high , based on the logic values present at Q and QB the charging and discharging takes place . This will observe on TL and TLB.

For high read stability and continous read operation a transmission gate technology is used for the ternary memory cell.

4.3 Ternary SRAM With Transmission Gate

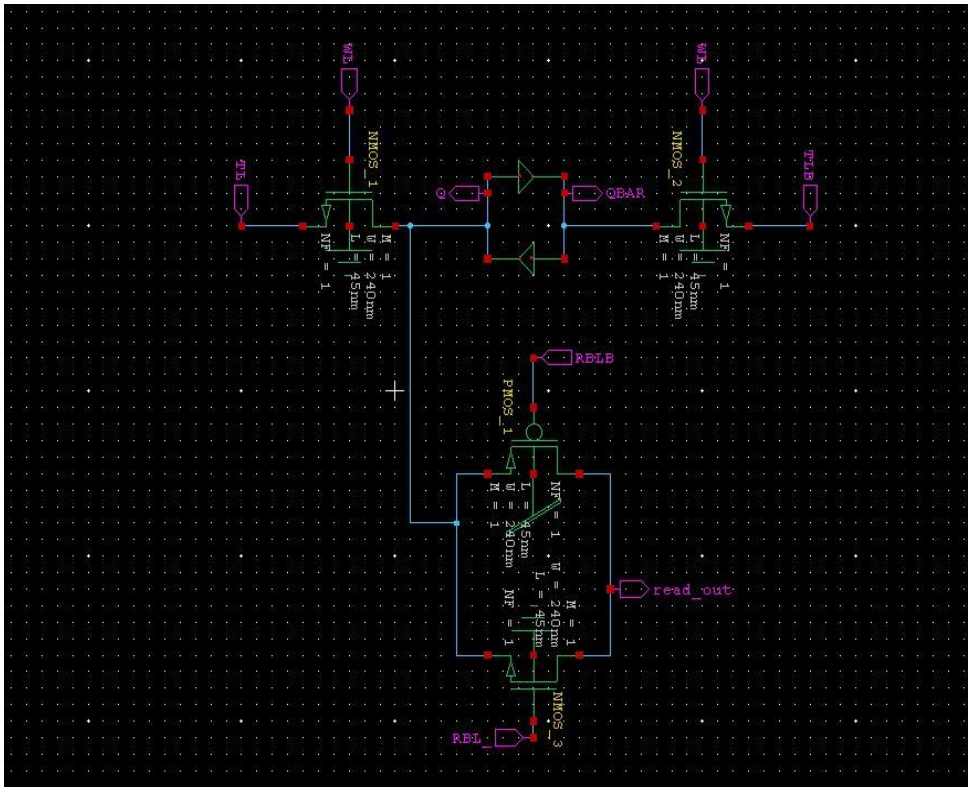

Fig 2c : Ternary SRAM by Transmission gate Technology

Table 4 Truth Table of Ternary SRAM for continous read operation

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OPERATION	WL	TL	TLB	RBL	Q	QB
Write	2	0/1/2	2/1/0	X	0/1/2	2/1/0
Read	X	X	X	2	0/1/2 (readout)	2/1/0
Hold	0	X	X	X	NC	NC

By including the transmittion gate with the design of ternary SRAM , can make the read operation possible irrespective of the logic value at WL,TL and TLB.

5 Simulation Results

Tanner t-spice is used to validate the functioning of stated designs; the simulation results are shown below.

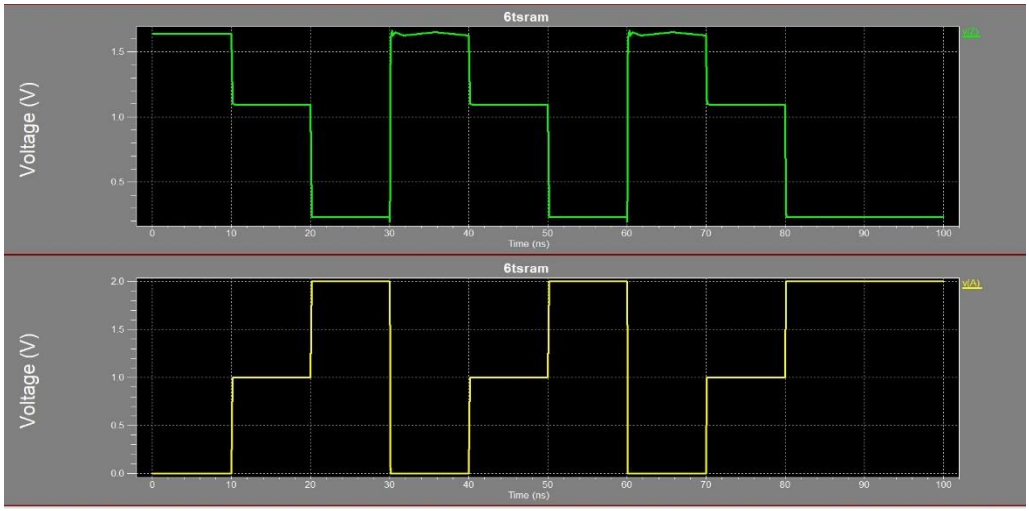

Fig 3a : Characteristics of STI

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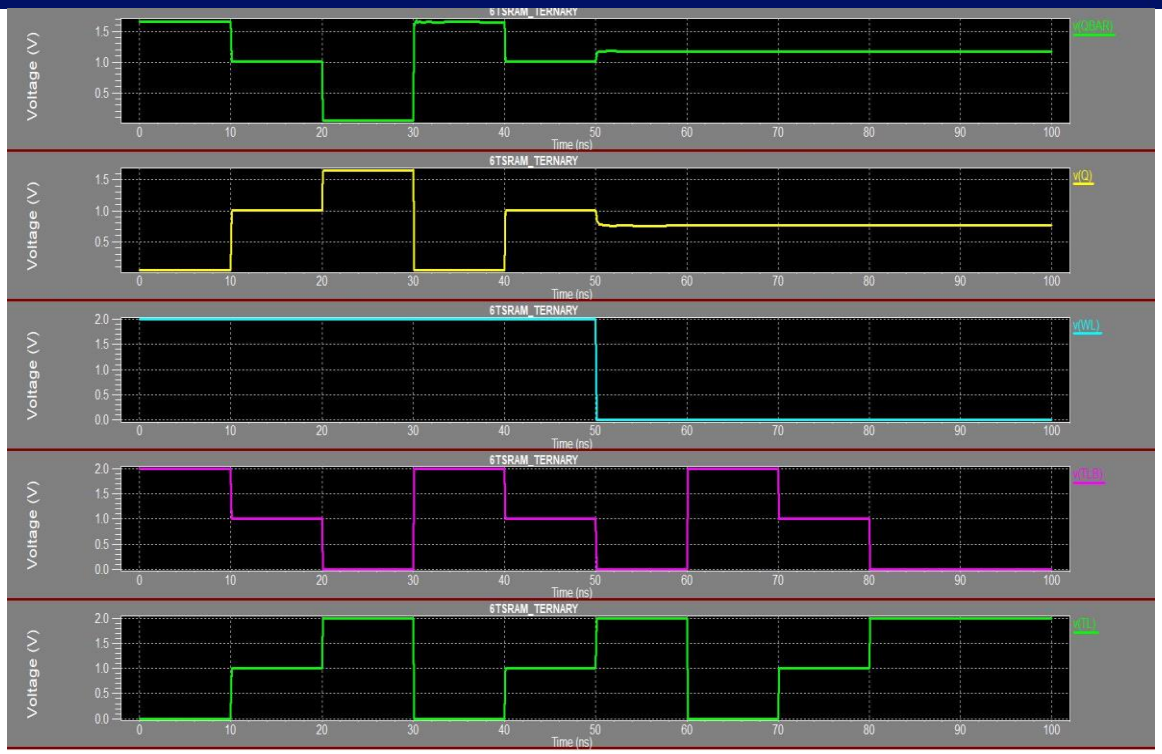

Fig 3b Characteristics of Ternary SRAM

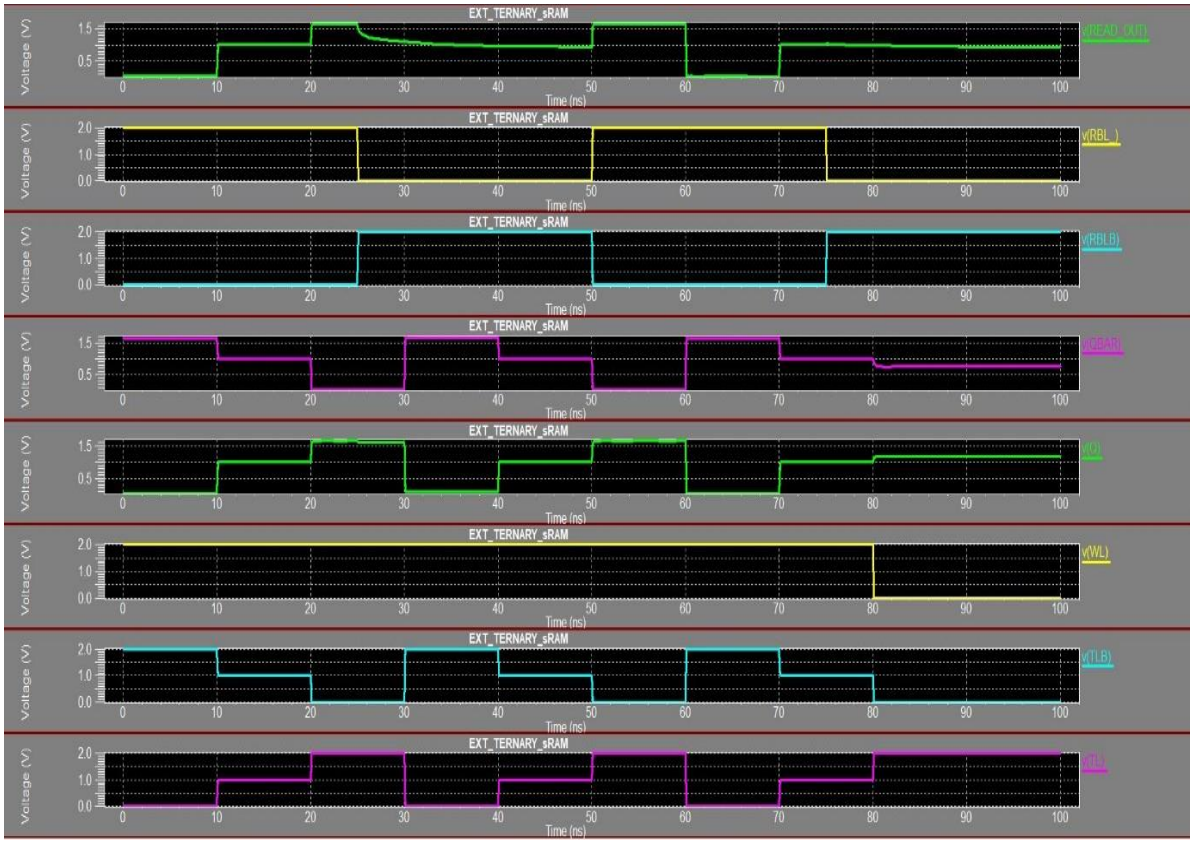

Fig 3c Characteristics of Ternary SRAM with Transmission Gate

Table 5 Design metrics of proposed designs from simulation

Design	No.of mosfets	Delay(ps)	Power (µw)
Ternary Inverter	6	0.2607	0.1767
Ternary SRAM	14	0.3637	531.94
Ternary SRAM by TG	16	2.2216	479.96

Table 6 Comparision of Design metrics with Existing design

Design	Memory capacity	Delay(ns)	Read Power(nw)
Existing Design	(0 or 1) / single cell	5.5	0.036
Proposed Design	(0 or 1 or 2) / single cell	0.0022	64.95

6 . Conclusion :

This paper discusses about proposes ternary Static RAM **.** The ternary SRAM is implemented for Memory Application to accomplish all three operations of write/hold/read , as a model provides progressive improvement in delay, ternary logic operation and stability . In future it requires more concentrated work on power consumption.

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