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Paper Authors

M.GANGA MAHESH1, HABEEMUNEESA 2

Electronics and Communication Engineering, SIR C.V. RAMAN Institute of Technology & Science, AP, India

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IMPLEMENTATION OF PRPG WITH LOW TRANSITION TEST COMPRESSION TECHNIQUE

M.GANGA MAHESH[1], HABEEMUNEESA [2]

1PG Scholar, Electronics and Communication Engineering, SIR C.V. RAMAN Institute of Technology & Science, AP, India

2 Assistant Professor, Electronics and Communication Engineering, SIR C.V. RAMAN Institute of Technology & Science, AP, India

ABSTRACT:

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation for VLSI circuits The novel test pattern generator which is more suitable for built in self test (BIST) structures used for testing of VLSI circuits. This paper describes a low-power (LP) programmable generator capable of producing pseudorandom test patterns with desired toggling levels and enhanced fault coverage gradient compared with the best-to-date built-in self-test (BIST)-based pseudorandom test pattern generators. It is comprised of a linear finite state machine (a linear feedback shift register or a ring generator) driving an appropriate phase shifter, and it comes with a number of features allowing this device to produce binary sequences with preselected toggling (PRESTO) activity. We introduce a method to automatically select several controls of the generator offering easy and precise tuning. The same technique is subsequently employed to deterministically guide the generator toward test sequences with improved fault-coverage-topattern- count ratios. Furthermore, this paper proposes an LP test compression method that allows shaping the test power envelope in a fully predictable, accurate, and flexible fashion by adapting the PRESTO-based logic BIST (LBIST) infrastructure.

1. INTRODUCTION

The test pattern generator produces test vectors that are applied to the tested circuit during pseudo-random testing of combinational circuits. The nature of the generator thus directly influences the fault coverage achieved. The influence of the type of pseudo-random pattern generator on stuck-at fault coverage. Linear feedback shift registers (LFSRs) are mostly used as test pattern generators, and the generating polynomial is primitive to ensure the maximum period. We have shown that it is not necessary to use primitive polynomials, and moreover that their using is even undesirable in most cases. This fact is documented by statistical graphs. The necessity of the proper choice of a generating polynomial and an LFSR seed is shown here, by designing a mixed-mode BIST for the ISCAS benchmarks As the complexity of VLSI circuits constantly increases, there is a need of a built-in self-test (BIST) to be used. Built-in self-test enables the chip to test itself and to evaluate the circuit's response. Thus, the very complex and expensive external ATE (Automatic Test Equipment) may be

completely omitted, or its complexity significantly reduced. Moreover, BIST enables an easy access to internal structures of the tested circuit, which are extremely hard to reach from outside. There have been proposed many BIST equipment design methods. In most of the state-of-the-art methods some kind of a pseudorandom pattern generator (PRPG) is used to produce vectors to test the circuit. These vectors are applied to the circuit either as they are, or the vectors are modified by some additional circuitry in order to obtain better fault coverage. Then the circuit's response to these vectors is evaluated in a response analyzer. Usually, linear feedback shift registers (LFSRs) or cellular automata (CA) are used as PRPGs, for their simplicity. Patterns generated by simple LFSRs or CA often do not provide a satisfactory fault coverage. Thus, these patterns have to be modified somehow. One of the most known approaches is the weighted random pattern testing . Here the LFSR code words are modified by a weighting logic to produce a test with given probabilities of occurrence of 0's and 1's at the particular circuit under test (CUT) inputs. Many papers dealing with the computation of the weights and the design of the weighting logic have been published .

2.LITERATURE SURVEY:

Built-in self test is a design technique in which parts of a circuit are used to test the circuit itself. Built in self test is the capability of the circuit (chip board or system) to test itself. BIST represents a merger of concept of built in test and self test and hence come to be synonymous with terms. BIST technique can be classified into two categories, namely online BIST which includes concurrent and non concurrent techniques, and offline BIST which includes functional and structural approaches. In ONLINE BIST, testing occurs during normal function operating condition; i.e the circuit under test(CUT) is not placed into a test mode where normal functional operation is locked out. Concurrent-on-line BIST is a form of testing that occurs simultaneously with normal function operation. This form of testing is usually accomplished using coding techniques or duplication and comparison. In non-concurrent on-line BIST, testing is carried out while a system is in an idle state. This often accomplished by executing diagnostic software routine or diagnostic firm where routines. The test process can be interrupted any time so that normal operation can be resuming.

OFFLINE BIST deals with testing a system when it is not carrying out its normal functions. Systems, boots and chips can be tested in this mode. This form of testing is also applicable at the manufacturing field, depot and operational levels. Often off-line testing is carried out using on chip or on board test pattern generator(TPGS) and output response analyser (ORAS) or micro diagnostic routine. Offline testing does not detect errors in real time that is when they first occur, as it possible with many online concurrent BIST techniques. Functional offline BIST deals with execution of a test based on a functional description of CUT and often employs a functional or high level, fault level. Normally such a tests is implemented as diagnostic software or firmware. Structural offline BIST deals with the execution of a test base on the structure of the CUT. An explicit structural fault model may be use fault coverage is based on detecting structure faults. Usually

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tests are generated and responses are compresses using some form of an LFSR.

3. PRESTO (PRESELECTED TOGGLING) GENERATOR:

A n-bit PRPG is connected with a phase shifter feeding scan chains producing pseudo random test patterns.A linear feedback shift register(LFSR) or a ring generator can implement a PRPG(PseudoRandom Pattern Generator).In between PRPG and phase shifter n hold latches are connected and it is controlled by n-bit toggle control register.When the enable input is given, the latch becomes transparent otherwise latch is disabled and captures and saves for a period of clock cycles with constant value feeding phase shifter.

The toggle control registers supervises hold latches which consists of 0s and 1s where 1s indicate toggle mode thus latch is transparent for data moving from PRPG. The toggle control register are loaded once per pattern count with additional shift register content and the enable signals for the shift register are produced in probalisitic manner by using original PRPG with programmable set of weights.The weights are determined by four AND gates producing 1s with probability 0.5,0.25,0.125,0.0625 respectively. The OR gate allows choosing probabilities beyond powers of 2.

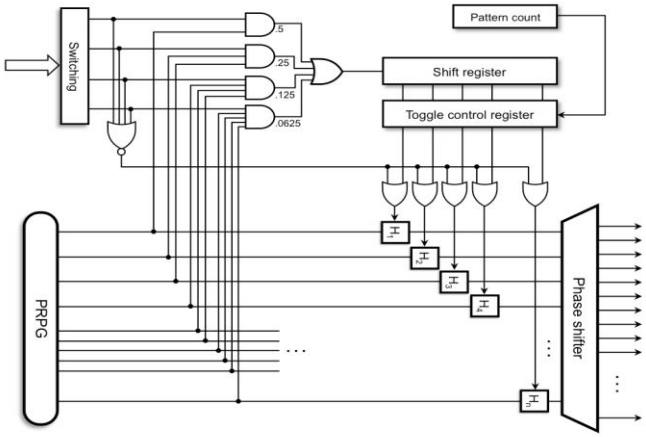

Fig 1 Basic architecture of PRESTO generator

An additional 4-input NOR gate detects the switching code0000, which is used to switch the LP functionality off.So,while working in weighted random mode,the switching selector ensures stastically stable content of the control register interms of amount of 1s it carries.Much higher flexibility in forming low-toggling test patterns can be achieved using this architecture.This approach splits up a shifting period of every test pattern into sequence of alternate toggle and hold intervals.To move to and forth between toggle and hold states,we use a T-flip flop that switches wheneverthere is at 1 on its data input.If it is set to 0,the generator enters in hold mode with temporarily disabling latches regardless of the toggle control register.If it is set to 1,it enables the latches and enters into togglemode which moves data from PRPG to scan chains.

Two additional parameters kept in toggle and hold register determine how long the entire generator remains either in toggle or hold mode.To terminate either mode,a 1must occur on T-flip flop similar to that of a weighted logic used to feed the shift register.The T-flip flop controls four 2-input multiplexers routing data from toggle and

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control registers.It allows selecting a source of control data that will be used in the next cycle to change the operational mode of the generator testpatterns.When using the PRESTO generator with existing DFT flow,all LP registers are either loaded once per test data registers or parts of an IJTAG network,and are initialized by the test setup procedure.Clearly,it suits LBIST applications where shift speeds are quite high.

4 FULLY OPERATIONAL PRESTO GENERATOR

As shown in operational version of PRESTO generator depend on mainly three factors in BIST mode they are:1)1the switching code(kept in switching register 2)the hold duty cycle(HC) 3)the toggle duty cycle.Given the size of PRPG,the number of the scan chains and the corresponding phase shifter, the switching code as well as HC and TC values can be selected automatically in such a way that the entire generator will produce pseudorandom test patterns having a desired level of togglingT provided the scan chains are balanced.The procedure for selecting these parameters consists of many steps and values of switching hold and toggle codes yields a ratio r with smallest deviation from theoretical values using equation A=(T * S)/50 where S is the total number of scan chains and T is the toggling level (%) and A is the number of active scan chains.

Ring generators are high performance LFSR which produces pseudo random test patterns which produces binary sequences.Two adjacent flipflop contain atmost one 2-input XOR gate and each flip-flop output drives atmost 2 fanoutnodes.The circuit is constructed in ring structure so there is no long feedback path connecting the right most flipflop to the left-most flip flop.It is a ring shape structure and produces two layer feedback so power consumption will be more.

The principle of the decompressor is to disable both weighted logic blocks(V and H) and to deploy control data instead. The content of toggle control register can be selected in deterministic manner due to multiplexer placed in front of shift register.Further, the toggle and hold registers alternately preset a 4-bit down counter, thus determine the durations of hold and toggle phases.When circuit reaches a value of zero, it causes a dedicated signal to go high in order to toggle the T-flip flop.The same signal allows the counter to have the input data kept in toggle or hold register entered as the next state.

Both the down counter and the T-flip flop needed to be initialized for every test pattern.The initial value to the T- flip flop decides whether the decompressor will begin to operate either in toggle or in the hold mode, while the initial value to the counter is reffered to as an offset, determines mode's duration.The functionality of the T-flip flop remains same as that of LP PRPG.Here, it occurs in two cases: First of all, the encoding procedure can completely disable the hold phase by loading the Hold register with appropriate code.If detected (No Hold) it overrides the output of the T-flip flop by using an additional OR gate.As a result, the entire test pattern is going to be encoded within toggle mode exclusively.In addition ,all the hold latches have to be properly initialized.Hence a control signal First cycle produced at the end of ring generator initialization phase reloads all latches with current content of this part of the

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decompressor.

In order to facilitate test data decompression while preserving its original functionality the circuit is rearchitected.This architecture consists of an additional block transition controller and ring generator is replaced by LFSR.LFSR produces pseudorandom test patterns and consumes less power compared to ring generator.Transition controller produces less controlled transitions on phase shifter outputs.

In the proposed system, Linear feedback shift registers(LFSRs) produce extremely good pseudorandom test patterns.Gated clock signal present in design approach for LFSR lead to power reduction.Power reduction hardly depends on technological characteristic of gates employed.LFSR is a shift register whose input is result of XOR of some of its inputs.The outputs of flip-flops are loaded with seed value(anything except 0s which cause LFSR to produce all 0 patterns)and when LFSR is clocked,it will generate PRPG of 1s and 0s.Here,the signal necessary to generate test patterns is clock.Maximum length of LFSR is 2^n-1.

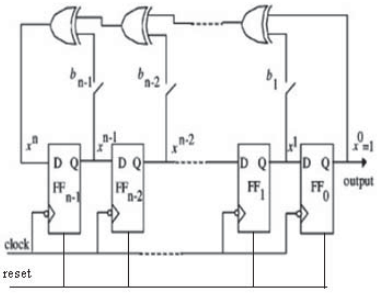

Fig.2 Simplified circuit of a generic LFSR circuit

Low Power PRPG architecture with transition controller:

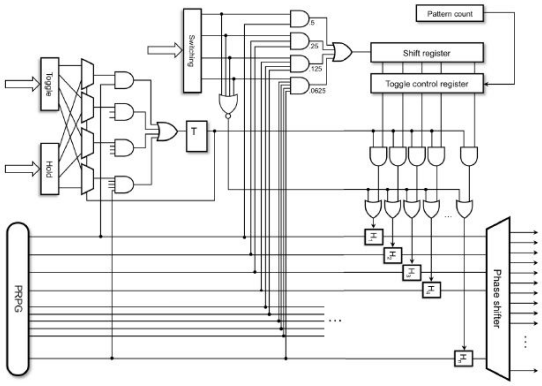

Fig 3 Fully operational version of PRESTO

An adaptive technique is applied to reduce the shift power to improve the shift power reduction in logicBIST.To get the required power reduction, we implement an additional module called transition controller.During shift mode the previous test responses in scan flip-flops are given as feedback to transition controller which is used to generate test patterns so that switching is reduced.

The transition controller consists of a multiplexer,a XNOR gate and D-flip flop.The inputs of XNOR gate is driven by the outputs of last two scan cells in the same chain SCk-1 and SCk.The output of XNOR gate connects to multiplexer selects input and here,we assume that there is no inversion between SCk-1 and SCk.When SCk-1 and SCk have different values ,the value at XNOR gate output is 0 and it causes the D-flip flop hold its previous value.Otherwise the D-FF will be updated by phase-shifteroutput.

IV. LP DECOMPRESSOR

In order to facilitate take a look at information decompression whereas protective its original

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practicality, the electronic equipment of Fig. two should be rearch itected. this is often shown in Fig. 3.

The core principle of the decompressor is to disable each weighted logic blocks (V and H) and to deploy settled management information instead. particularly, the content of the toggle management register will currently be elect in an exceedingly settled manner attributable to a electronic device placed before of the register. what is more, the Toggle and Hold registers area unit utilized to alternately predetermined a 4-bit binary down counter, and so to work out durations of the hold and toggle phases. once this circuit reaches the worth of zero, it causes a passionate signal to travel high so as to toggle the T flip-flop. constant signal permits the counter to own the input file unbroken within the Toggle or Hold register entered because the next state. Both the down counter and also the T flip-flop have to be compelled to be initialized each take a look at pattern. The initial

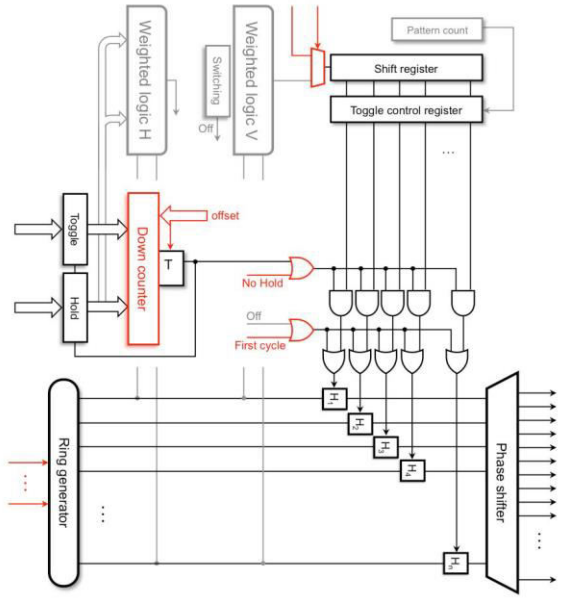

Fig.4. LP decompressor—modules in gray are disabled. The red items have been added.

worth of the T flipflop decides whether or not the decompressor can begin to work either within the toggle or within the hold mode, whereas the initial worth of the counter, any stated as associate degree offset, determines that mode's period. As will be seen, practicality of the T flip-flops remains constant as that of the disc PRPG however 2 cases. 1st of all, the cryptography procedure might utterly disable the hold part (when all hold latches area unit blocked) by loading the Hold register with associate degree applicable code, as an example, 0000. If detected (No

Hold signal within the figure), it overrides the output of the T flip-flop by exploitation an extra logic gate, as shown in Fig. 4. As a result, the whole take a look at pattern goes to be encoded among the toggle mode solely. additionally, all hold latches got to be properly initialized. Hence, an impression signal 1st cycle made at the tip of the ring generator data format part reloads all latches with the present content of this a part of the decompressor. Finally, external Ate channels (feeding the initial PRPG) permit one to implement a continual flow take a look at information decompression paradigm like the dynamic LFSR reseeding. Given the scale of PRPG, the amount of scan chains and also the corresponding part shifter, the shift code, the offset, furthermore because the values unbroken within the Toggle and Hold registers, the whole decompressor can manufacture settled (decompressed) take a look at patterns having a desired level of toggling provided the scan chains area unit balanced.

5.RESULTS AND DISCUSSION

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5.1 BLOCK DIAGRAM

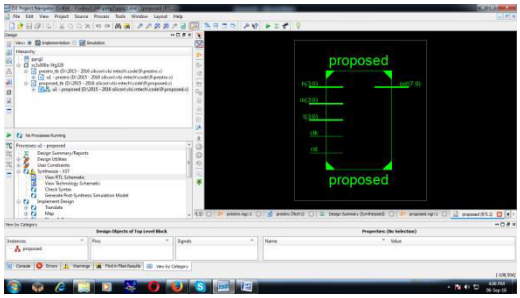

Fig 4 Block diagram of proposed system

5.2 SIMULATION RESULTS FOR PROPOSED SYSTEM

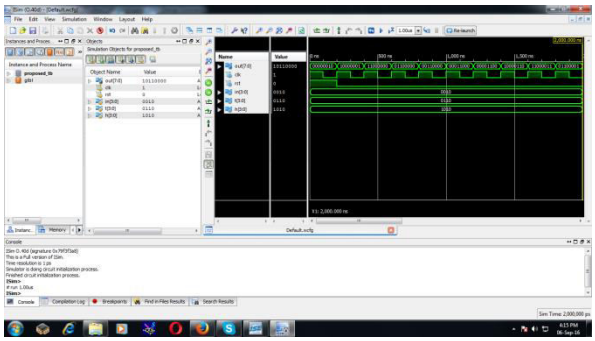

Fig 5 patterns generated in proposed system

Above fig 7.10 gives simulation result of proposed system which consist of 3-bit input data, toggle data, hold data which decides how much switching activity occurring in circuit and it generates the 8-bit different patterns which were required for our circuit implementation.

6 RESULT COMPARISION OF EXISTING SYSTEM(S.K.GUPTA[8]) WITH PROPOSED SYSTEM

Serial No	Parameter	Existing system	Proposed System
1	Power consumption(W)	0.089	0.088
2	Path Delay(ns)	7.061	7.183
3	No of Slices(CLB)	10	14
4	Frequency(MHz)	141.6	139.2

	PRESTO.	Proposed PRESTO.	LP decompressor
power	89 mw	88 mw	87 mw

7.CONCLUSION & FUTURE SCOPE

CONCLUSION:

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The seed generated from (LP-LFSR) is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities among the test patterns. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator. From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.

FUTURE SCOPE:

We can implement LP TPG (Low Power Test Pattern Generator) by using gray code convertor and LFSR which can reduce power consumption more compared to our proposed system.

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