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# VLSI ARCHITECTURE OF FM0/MANCHESTER ENCODING USING SOLS TECHNIQUE FOR WIRELESS SENSOR NETWORK

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## ABSTRACT:

In this paper we studied the implementation of Manchester coding is being described.Manchestercoding technique is a digital coding technique in which all the bits of the binary data are arranged in a particular sequence. These sections operate completely independent of each other, except for the Master Reset functions. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.The encoding can also be used in many party line digital data communications application such as an environmental control system driven from single twisted pair cable of fiber optic cable throughout the building. This circuitry can run very fast since it does not require a high-frequency clock. The frame format used is similar to that of a UART. The Manchester decoder limits the maximum frequency of operation of the MED, since it uses a high-frequency clock. The receiver circuitry is more complex, since clock recovery and center sampling is done. Additional receiver functions are frame detection, decoding of Manchester to NRZ, serial to parallel conversion, and a microprocessor interface.

**Keywords:** Manchester coding, Encoder, Decoder, NRZ, Moore's law, UART, clock frequency.

## I. INTRODUCTION

Manchester coding technique is a digital coding technique in which all the bits of the binary data are arranged in a particular sequence.Here a bit '1'is represented by transmitting a high voltage for half duration the input signal and for the next halftime Period an inverted signal will be send. When transmitting 0'in Manchester format, for the first half cycle a low voltage will send, and for the next half cycle a high voltage is send. The advantage of Manchester coding is that, when sending a data having continuous High signals or continuous low signal (e.g.: 11110000) , it is difficult to calculate the number of 1 S and Os in the data. Because there is no transition from low to high or high to low for a particular time period (Here it is 4 x T, T is the time duration for a single pulse).The detection is possible only by calculating the time duration of the signal. But when we code this signal in Manchester format there will always be a transition from high to low or low to high for each bit.Thus for a receiver it is easier to detect the data in Manchester format and also the probability for occurrence of an error is very low in Manchester format and it is a universally accepted digital encoding technique. The dedicated short range communication is a protocol for one or two way medium range communication. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to road side.In automobile-to-automobile, the DSRCenables the messages ending and broad casting among automobile.The automobile to-roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC). The DSRC architecture having the transceiver. The transceiver having the base band processing, RF front end and microprocessor.

The microprocessor is used to transfer the instruction to the baseband processing and RF front end. The RF front end is used to transmit and receive the wireless signals using the antenna .

The base band processing is responsible for modulation, error correction, encoding and synchronization. The transmitted signal consists of the arbitrary binarysequence, it is very difficult to obtain the dc balance.The fm0 and Manchester are providing the transmittedsignal and then the dc-balance. both FM0 andManchester codes are widely adopted in encoding fordownlink. The (SOLS) similarity oriented logic simplificationhaving the two methods:

A. area compact retiming and
B. balance logic operation sharing.

The area compact retiming used to reduce thetransistor counts, the balance logic operation sharing isused to combine the fm0 and Manchester encoding.

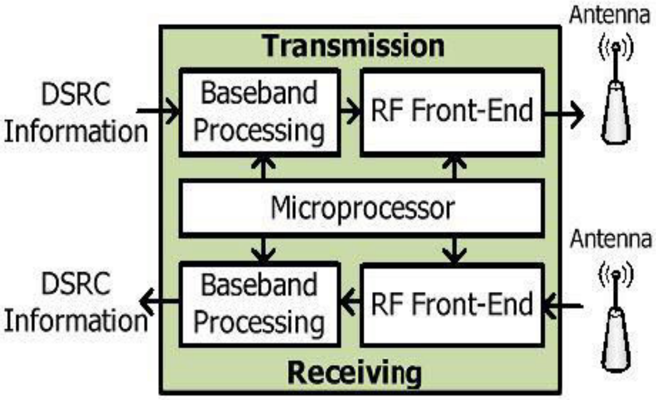


Fig: 1.System architecture of DSRC transceiver.

The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts arededicated for transmission and receiving, respectively. This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF frontend. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna. The DSRC standards have been established by several organizations in different countries. TheseDSRC standards of America, Europe, and Japan are shown in Table I. The data rate individually targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz. The modulation methods incorporate amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zero mean for robustness issue, and this is also referred to as dc-balance.

## II.LITERATURE SURVEY

The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance. The purposes of FM0 and Manchester codes can provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink. The VLSI architectures of FM0 and Manchester encoders are reviewed as follows

A. Review of VLSI Architectures for FM0 Encoder and Manchester Encoder The literature [4] proposes VLSI architecture of Manchester encoder for optical communications. This design adopts the CMOS inverter and the gated inverter as the switch to construct Manchester encoder. It is implemented by 0.35-µm CMOS technology and its operation frequency is 1 GHz. The literature [5] further replaces the architecture of switch in [4] by the nMOS device. It is realized in 90-nm CMOS technology, and the maximum operation frequency is as high as 5 GHz. The literature [6] develops a highspeed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. This design is realized in 0.35-µm CMOS technology and the maximum operation frequency is 200 MHz. The literature [7] also proposes Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is conducted from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA) prototyping system. The maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator [8]. Its maximum operation frequency is about 192 MHz. Furthermore,[9] combines frequency shift keying (FSK) modulation and demodulation with Manchester codec in hardware realization.

## III. CODING PRINCIPLES OF FM0 CODE ANDMANCHESTERCODE:

In the following discussion, the clock signal and the input data are abbreviated as CLK, and X, respectively. With the above parameters, the coding principles of FM0 and Manchester codes are discussed as follows.

A. FM0 Encoding for each X, the FM0 code consists of two parts: one for former-half cycle of CLK, A, and the other one for later-half cycle of CLK,B. The coding principle of FM0 is listed as the following three rules.

1) If X is the logic-0, the FM0 code must exhibit a transition between A and B.

2) If X is the logic-1, no transition is allowed between A and B.

3) The transition is allocated among each FM0 code no matter what the X is.

Fig: 2.

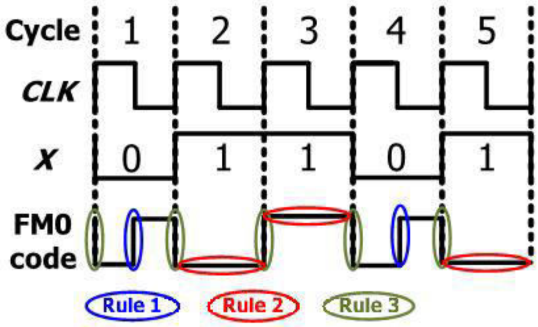


Fig: 2.Illustration of FM0 coding example.

A FM0 coding example is shown in Fig. 2. At cycle 1, the X is logic-0; therefore, a transition occurs on its FM0 code, according to rule 1. For simplicity, this transition is initially set from logic-0 to -1. According to rule 3, a transition is allocated among each FM0 code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2.

Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the X of logic-1. Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

B. The Manchester coding example is shown in Fig.3.

The Manchester code is derived from

$$X \oplus CLK.$$

The Manchester encoding is realized with a XORoperation for CLK and *X*. The clock always has atransition within one cycle, and so does theManchester code no matter what the *X* is.

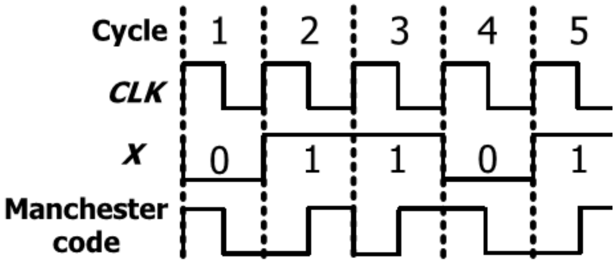


Fig: 3.Illustration of Manchester coding example.

## Hardware Architecture Of Fm0/Manchester Code:

This is the hardware architecture of the fm0/Manchestercode shown in Fig.4. the top part is denoted the fm0 code and then the bottom part is denoted as the Manchester code. In fm0 code the DFFA and DFFB are used to store the state code of the fm0 code and also mux_1 and not gate is used in the fm0 code. When the mode=0 is for the fm0 code. The Manchester code is developed only using the XOR gate and when the mode=1 is for the Manchester code. The hardware utilization rate is defined as the following:

$$HUR = \frac{Active\ components}{total\ components} \times 100$$

The component is defined as the hardware to perform a specific logic function, such as AND, OR, NOT, and flip-flop.The active components mean the components that work for FM0 or Manchester encoding. The total components are the number of components in the entire hardware architecture no matter what encoding method is adopted.

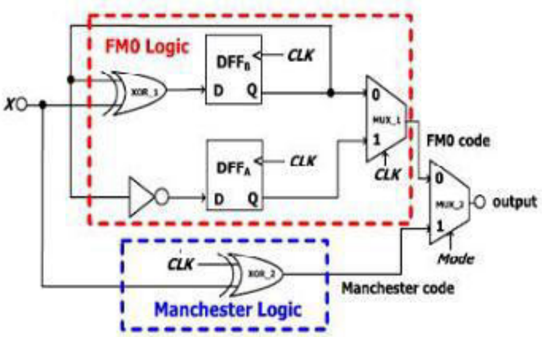
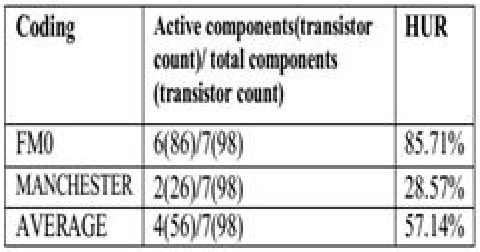


Fig: 4.Hardware architecture

The active components means the components are work in the both fm0 and Manchester code. The total components means the number of the components are present in the hole circuit. The HUR rate is given below the following Table 1.

TABLE I

HUR rate of FM0 And Manchester Encoding



| Coding | Active components(transistor count)/ total components (transistor count) | HUR |
|---|---|---|
| FM0 | 6(86)/7(98) | 85.71% |
| MANCHESTER | 2(26)/7(98) | 28.57% |
| AVERAGE | 4(56)/7(98) | 57.14% |

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For both the encoding methods the total components is 7.for the fm0 code the total component is 7 and then the active component is 6.in Manchester code the total component is 7 the active component is 2.in both coding having 98 transistors are used without SOLS. The fm0 was having 86 transistors, and then the Manchester having the 26 transistor.

The average for both coding is 56 transistors .In proposed work reduces the total components from 7 to 6 and reduce the transistor counts. In this paper two multiplexer is used in proposed work reduce two multiplexer from one multiplexer, when reduce the multiplexer the total components are reduced the area and then the power Consumption also reduced.

## IV. FMO and Manchester Encoder Using SOL’sTechnique:

The SOLS technique is classified into two parts area compact retiming and balance logic operation sharing.

### A. Area Compact Retiming

Fig.5. shows fm0 state code of the each state is stored into DFFA and DFFB .the transition of the state code is only depends on the previous state of B(t-1) instead of the both A(t-1) and B(t-1)

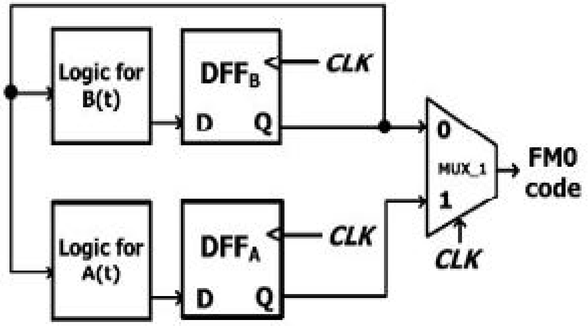


Fig: 5.Area compact retiming

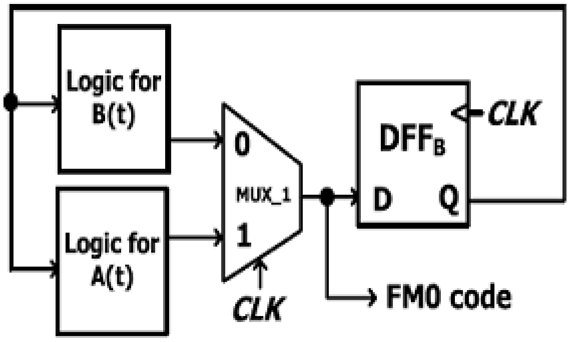


Fig: 6.FM0 encoding without area compact retiming

The previous state is denoted as the A(t-1) and then the B(t-1).and then the current state is denoted as the A(t) and then the B(t).

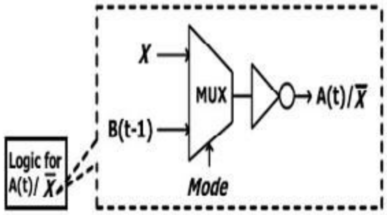


Fig: 7.FM0 encoding with area compact retiming.

Thus, in Fig.6. the FM0 encoding just requires a single 1-bitflip-flop to store the previous valuemB(t−1).If the DFFA is directly removed, a non synchronization between A(t) and B(t)causes the logic fault of FM0 code. To avoid this logic-fault, the DFFB is relocated right after the MUX−1, where the DFFB is assumed be positive-edge triggered flip flop.

At each cycle, the FM0 code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FM0 code is alternatively switched between A(t) and B(t) through the MUX−1 by the control signal of the CLK. In the Q of DFFB is directly updated from the logic of B(t) with 1-cycle latency. When the CLK is logic-0, the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB.

TABLE II
Transistor Count Of Fm0 Encoding Architecture With Area Compact Retiming

| | Without area-compact retiming | With area-compact retiming |
|---|---|---|
| PMOS | 36 | 25 |
| NMOS | 36 | 25 |
| Total | 72 | 50 |

The timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. The B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not.

The transistor count of the FM0 encoding architecture without area-compact retiming is 72, and that with area-compact retiming is 50. The areacompactretiming technique reduces 22 transistors.

### B. Balance logic operation sharing

The Manchester encoding is derived using the XORoperation. The equation of the XOR gate is givenbelow.

$$X \oplus CLK = X\ CLK + \sim X\ CLK \quad (3)$$

The concept of balance logic-operation sharing is tointegrate the X into A(t) and X into B(t).The fm0 andManchester logics have a common point of themultiplexer like logic with the selection of the CLK.the diagram for the balance logic operation sharinggiven the following.

In Fig.7. The A(t) can be derived from an inverterof B(t−1),and X is obtained by an inverter of X. Thelogic for A(t)/X can share the same inverter, and thenba multiplexer is placed before the inverter to switch heoperands of B(t − 1) and X. The Mode indicateseitherFM0 or Manchester encoding is adopted. Thesimilar concept can be also applied to the logic forB(t)/X shown in Fig.8.

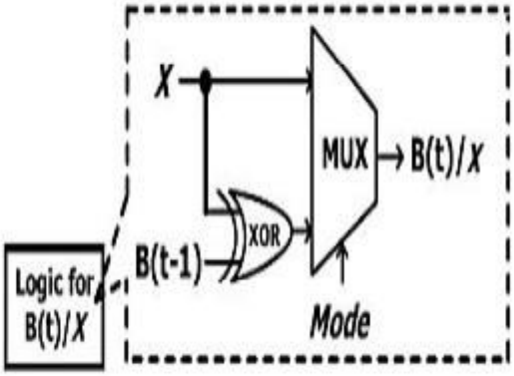
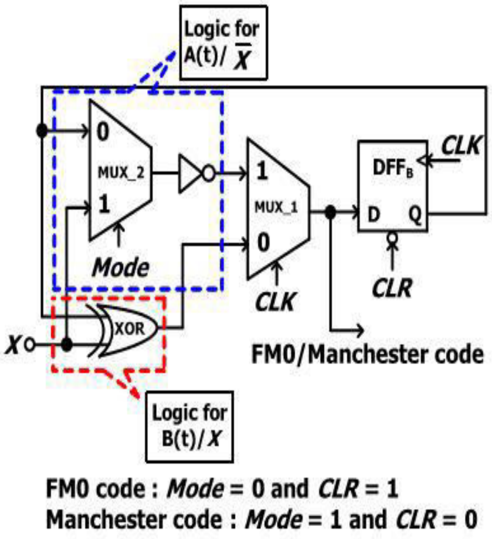


Fig: 8.Balance logic operation sharing

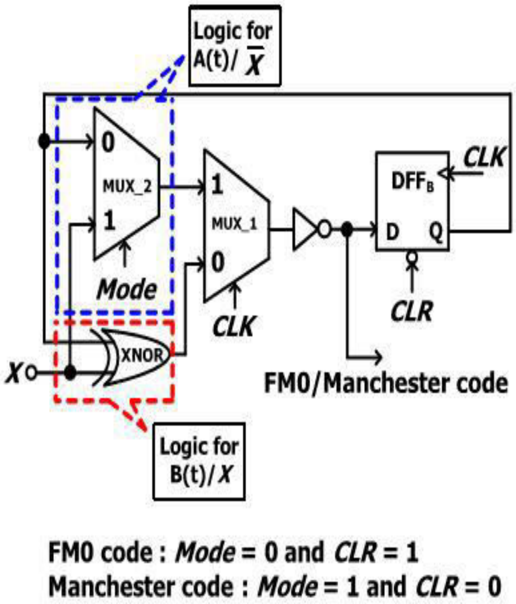
Never the less, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and is not shared with Manchester encoding. Therefore, Fig.9.shows the HUR of thisarchitecture is certainly limited. The X can be also interpreted as the X 0, and thereby the XOR operation can be shared with Manchester and FM0 encodings, where the multiplexer irresponsible to switch the operands of B(t−1) and logic-0. This architecture shares the XOR for both B(t) and X, and there by increases the HUR. When the FM0 code is adopted, the CLR is disabled, and the B(t −1) can be derived from DFFB.

Hence, the multiplexer can be totally saved, and its function can be completely integrated into the relocated DFF. The logic for A(t)/X includes the MUX−2 and an inverter. Instead ,the logic for B(t)/X just incorporates a XOR gate. In the logic for A(t)/X, the computation time of MUX−2is almost identical to that of XOR in the logic for B(t)/X. However, the logic for A(t)/X further incorporates an inverter in the series of MUX−2. This unbalance computation time between A(t)/X and B(t)/X results in the glitch to MUX−1,possibly causing the logic fault on coding. To alleviate this unbalance computation time, the architecture of the balance computation time between A(t)/X and B(t)/XThe XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for A(t)/X.

This shared inverter is relocated backward to the output of MUX−1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other. The adoption of FM0 or Manchester code depends on Mode and CLR. In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller.



(a)



(b)

Fig: 9.VLSI architecture of FM0 and Manchesterencodings using SOL’s technique. (a) Unbalancecomputation time between A(t)/X and B(t)/X. (b)Balance computation time between A(t)/X and B(t)/X.

Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved.

## V. SIMULATION RESULTS

### FM0 Module:

Fig: 10.FM0 graph

### RTL Schematic

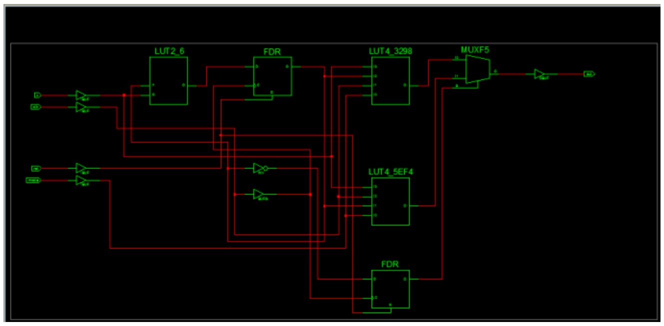


Fig: 11. RTL Schematic of FM0/Manchester Encodingusing SOL's Technique.

### Technology Schematic:

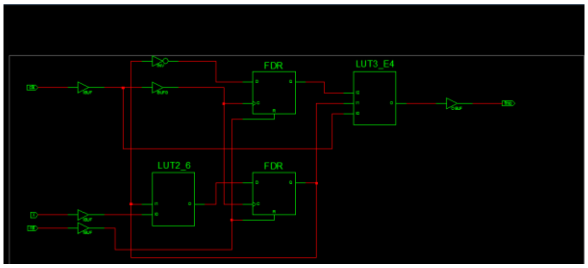


Fig:12.Technology schematic of FM0/ManchesterEncoding using SOL's Technique.

## VI. CONCLUSION

The coding-diversity between FM0 and Manchesterencodings causes the limitation on hardware utilizationof VLSI architecture design. A limitation analysis onhardware utilization of FM0 and Manchesterencodings is discussed in detail. In this paper, the fullyreused VLSI architecture using SOLS techniquefor both FM0 and Manchester encodings isproposed.

The SOL's technique eliminates thelimitation on hardware utilization by two coretechniques: area compact retiming and balance logicoperationsharing. The area compact retiming relocatesthe hardware resource to reduce the transistors. Thebalance logic-operation sharing efficiently combinesFM0 and Manchester encodings with the identicallogic components. This paper is realized in180nmtechnology with outstanding device efficiency. Thepower consumption is 29392.843nW for Manchesterencoding and FM0 encoding.

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