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LOW COST LOW POWER ALL DIGITAL SPREAD SPECTRUM CLOCK GENERATOR

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ABSTRACT

This paper gives the brief description of digital communication system. Digital communication is more reliable, secure and efficient than that of analog communication. In Digital communication, BPSK is most important and efficient technique in terms of signal power. In this brief, a low-cost low-power all-digital spreads spectrum clock generator for BPSK is presented. In this paper BPSK modulator is purely design by using hardware description language (VHDL).

I. INTRODUCTION

In recent years, there has been a significant amount of research Performed in both industry and academia into the development Of CDMA systems. DS-CDMA is a type of spread-spectrum communication system in which multiple signal channelsoccupy the same frequency band, being distinguished by the use of different spreading codes. CDMA communication is employed in,for example, digital cellular telephone systems and personal communication services. In these systems, a base station communicates with a plurality of mobile stations, one frequency band being used for all of the up-links from the mobile stations to the base station, and another frequency band being used for all of the downlinks from the base station to the mobile stations.This paper describes the design and a circuit for pseudo random PN coding and synchronization of a wireless transmitter for DS-CDMA using VHDL software. The circuit for the transmitter is comprised of basic digital components, such as flip-flops, oscillators, shifts registers, PN coder and a BPSK modulator.FPGA was selected to implement this circuit. The research involved two phases -simulation and synthesis of the VHDL codes using the Synopsys package and converting the integrated circuit of the transmitter in the FPGA compiler for downloading on the Xilinx FPGA board.A VHDL design begins with an ENTITY block that describes the interface for the design. The interface defines the input and output logic signals of the circuit. The ARCHITECTURE block describes the internal operation of the design. Within these blocks, there are numerous other functional blocks used to build the design elements of the logic circuit created. The source code written using the normal TEXT editor, thensaved as a VHDL file with '.vhd' extension and transferred to any of the VHDL design compilers (DC). If the compilation shows no error(s), the file can be simulated, synthesized and implemented with FPGA.The transmitter components were designed individually using the bottom-up approach. The designs

were then combined and defined by a component declaration and port mapping. Generally, this is an easy method although it could have had Complications.The basic transmitter circuit used was adopted from the following digital components; flip-flops, shift registers, PN coder nd a BPSK modulator with 40 MHz DIP oscillators providing the reference frequency. This paper concentrates on the application of VHDL simulation tool and FPGA compiler to wireless data components. Networks operating over unlicensed bands have recently received increased attention with the prominence of such standards as IEEE 802.11 and Blue tooth. In 3G, the information transferred is not limited to having voices, images and digital data separately. Users will have full coverage and mobility for 144 kbps (preferably 348 kbps) and eventually up to 2 Mbps. With this wide bandwidth, users are able to access the information in full multimedia form, wirelessly and with better quality.

II. BPSK MODULATION

Binary Phase Shift Keying (BPSK) is an one modulation method using for base band digital data transmission. We are representing digital data as group of ones or zeros. For transmitting the digital data from source to destination which will be very long distance ,we cannot transmit digital data directly ,because analog signal only can be transmittable for a distance , So for transmitting the digital base band signal ,we need modulation ie one analog signal should modulated in correspondence to digital data, for traveling long distance ,the analog signal should have very high frequency in terms of Mhz ,this high frequency signal called as carrier.

III. TRANSMITTER BLOCK DIAGRAM

It contains 7 blocks, namely, PN code generator, control block, multiplexer, 16-bit shift register, parity bit, 1-bit shift register and PBSK modulator. The PN generator generates a DSCDMA code, which is multiplied by the data entering the PN generator. The Shiften port is controlled by the PN code generator. Here, the Control Block controls all the operations of the transmitter and the timing for the transmitted bits, enabling the multiplexer and the 16-bit shift register. The multiplexer fed coded data from the PN code generator and parity bit. The 16-bit shift register is used to shift the coded data parallel and serial to the parity and to the BPSK modulator simultaneously. The 16-bit coded data is shifted first to the parallel XORed with parity calculation and fed back to the multiplexer after storage in the 1-bit shift register. The parity bit is added to the 16-bit waiting for transmission in the 16-bit shift register. It is added at the end of the 16-bit coded data.

The operation is as follows:

- The coded data from the PN generator is multiplexed immediately when it appears at the PN output.
- The coded data is delayed for 2-clock cycle at the PN generator after each 16 clock cycle (state at previous flow chart).
- The multiplexed data is shifted and stored at 16-bit shift register.
- For 16 clock cycles the multiplexer multiplex the output of the PN generator.

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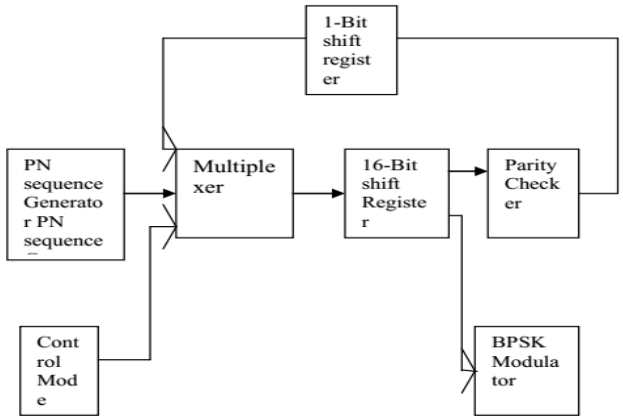
- For 2 clock cycles after each 16-clock cycle the multiplexer waits to multiplex one bit from the parity output. For the initial time of simulation the data appears at the PN output after 32-clockcycle.
- The 16-bit shift register shifted the coded data in parallel to parity to perform 1- bit parity and stored in 1-bit shift register.
- The data stored at the 16-bit shift register waited for 2-clock cycle to start transmission through the BPSK modulator in serial.
- The transmitted data frame contains 16-bit data with 1-bitparity.

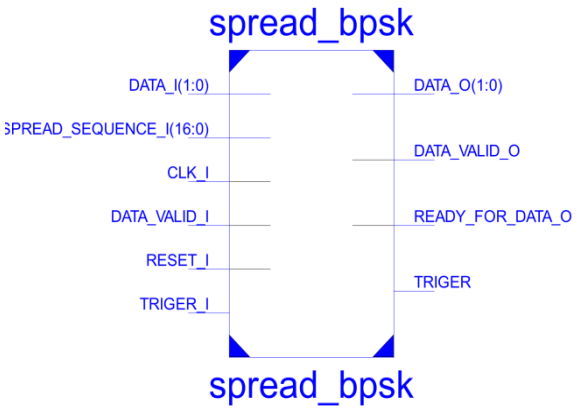


The block diagram of the DS-CDMA transmitter.

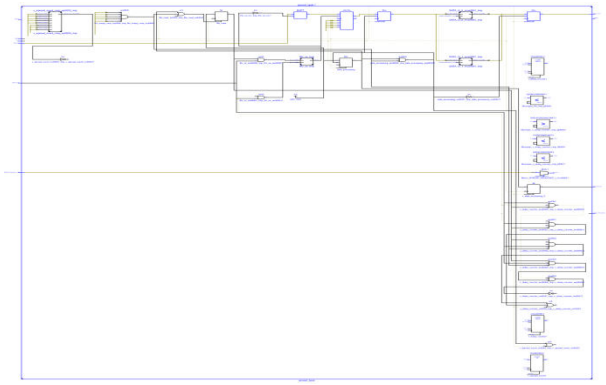
IV. RESULT ANALYSIS AND PERFORMANCE

The VHDL source code files were created and saved with the extension '.vhd'. These files were for the PN code generator, parity check (including control block, multiplexer, 16-bit shift register, parity bit and 1-bit shift register), oscillator and BPSK modulator. A toplevel design was created for the parity check files for the whole design. Then the design was simulated and synthesized to check its logical operation.

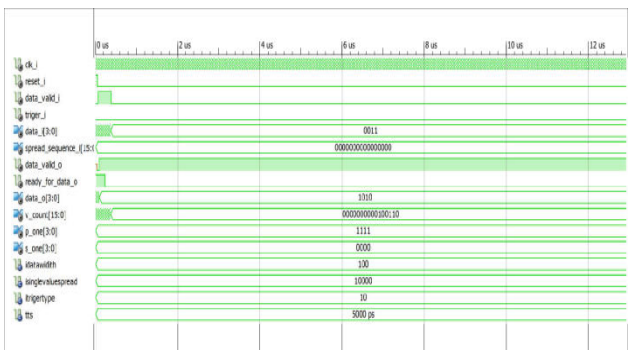
The individual elements were simulated using vhdlan and vhdlsim in the DOS command for Windows NT. The FPGA Compiler 11 was used for compiling and synthesizing the VHDL source code. The synthesis allowed the timing factors and the other influences of the actual FPGA devices to affect the simulation, thereby resulting in a more thorough check.



BPSK Block Diagram



RTL Schematic for BPSK



Simulation Results of BPSK

V. CONCLUSIONS

VHDL behavioral modeling is useful in digital systems design because the designer can model the circuit in a program that simulates the circuit operation rather than spend time on complex finite state machines or truth tables. This greatly facilities and reduces the design time for a large digital system. The simulation waveforms presented in this paper have proven the reliability of the VHDL implementation to describe the characteristics and the architecture of the digital transmitter. The simulated waveforms also have shown the observer how long the test result can be achieved by using test-bench file. From the waveforms the digital transmitter transmitted at Shigh data rates of up to 2 Mbps with the BPSK modulator holding the data during transmission. The transmitted data included a 1-bit parity that acted as error detection. From the optimized FPGA circuit for top-level design, the circuit of the transmitter was reduced sufficiently for downloading.

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