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DESIGN AND IMPLEMENTATION OF DIGITAL CIRCUITS USING NOVEL REVERSIBLE GATES

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ABSTRACT:

Reversible structures are very prominent designs in recent trends. Because it gives less power consumption and area. As R launderer said if it uses reversible circuits, then KTln2 power does not dissipate from the circuit in the form of heat. If there is no heat dissipation, energy will not be lost from the circuit. And another advantage of reversibility is, any input or output signal can be obtained at any stage. In this paper, some sequential circuits are designed using reversible logic. In reversible logic, the main problem is garbage outputs. By these garbage outputs, the delay constrains are increased. So, in this paper, circuits are designed with fewer garbage outputs i.e., having less delay. Here in this paper, Decoders, latches, comparators, adders and subtractors are designed using reversible logic with fewer garbage outputs. The designs are constructed using Verilog HDL in RTL style. The results are simulated using Quartus II software.

1.INTRODUCTION

1.1 DIGITAL CIRCUITS:

A digital logic circuit is defined as the one in which voltages are assumed to be having a finite number of distinct values. Types of digital logic circuits are combinational logic circuits and sequential logic circuits. These are the basic circuits used in most of the digital electronic devices like computers, calculators, mobile phones.

Digital circuits are of two types:

1. Combinational Logic Circuits.
2. Sequential Logic Circuits.

1.1.1 COMBINATIONAL LOGIC CIRCUITS

The combinational logic circuits are made up

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of logic gates whose output is determined by the present input only. The output does not depend on the previous outputs of the circuit. This type of circuit is widely used in the electronic industries for various purposes. The circuits are designed by combining the different logic gates. Two types of combinatorial circuits are encoder and decoder. Other examples include half adder, full adder, and multiplexer.

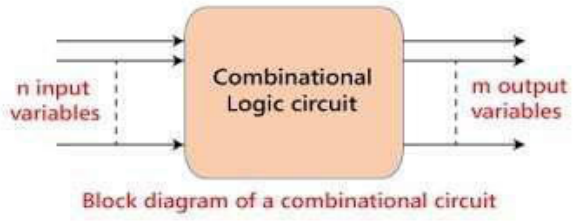

FIG 1.1: COMBINATIONAL CIRCUIT

1.1.2 SEQUENTIAL LOGIC CIRCUITS:

The sequential logic circuit is one such circuit in which the output of the circuit not only depends on the present input but it also depends on the past outputs Sequential circuits have the ability to store the past output in various memory devices. They are designed using finite state machines. Different kinds of sequential logic circuits are counters and flip flops. Sequential circuits are again of three types: clock-driven circuits, event-driven circuits, and pulse-driven circuits.

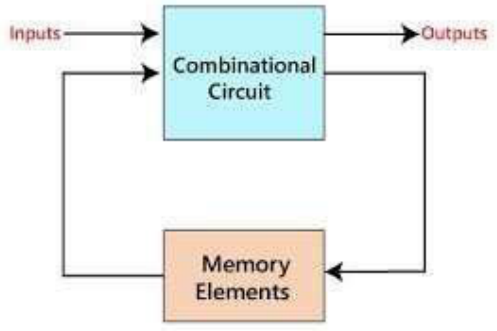

FIG 1.2: SEQUENTIAL CIRCUIT

Generally, a flip flop is a circuit that can be used to store the data in the form of bits i.e., in binary form. Here in this paper, flip-flops like T Flip-flop, D Flipflop, and JK Flip-flop are designed using reversible gates. Here T Flip-flop is designed with SGG gate and JK flip-flop is designed with NMG gates and Feynman gates as shown in fig. By using these flipflop designs will help to construct counters and LFSR. A counter is a device that can be used to count the number of pulses. These counters can be two types that are Synchronous counter and Asynchronous counter. For synchronous counters Only clock one clock is connected to all flip-flops. If you observe the asynchronous counter, the output of the flip-flop is a clock signal from the previous one. Here in this paper, a 4 bit Up-Down asynchronous counter is developed using T-flip-flops. The block diagram is shown in fig. Linear Feedback Shift Registers are extensively useful in test vectors generation for built-in self-test (BIST). Generally, LFSR is a very efficient pseudo- random test pattern generator. The basic building blocks for constructing LFSR are flipflops. In irreversible LFSR designs, the power consumed during testing is high. To eliminate this problem, LFSR can be designed with reversible logic gates. According to Lindauer if all operations required in computation could be performed reversibly, thus it cannot dissipate heat! The first condition is that for any device that to be reversible means that their response and input can be retrievable uniquely from each other - - then it is called logical reversibility. The second condition is that a device can operate backward, and then it is called physical reversibility. And the second law of thermodynamics guarantees that it cannot dissipate heat. By this, the power consumption is somehow decreased.

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1.2 REVERSIBLE GATES:

1.2.1. QUANTUM COST:

The quantum cost of a 1*1 Gate is Zero and the any 2*2 Gate is one. The Quantum cost of Reversible can be calculated by counting the numbers of NOT, Controlled V and CNOT Gates Required in its implementation. The quantum cost of a 2*2 Feynman gate is 1 while the quantum cost of 3*3 Fredkin and Peres gate is 5 and 4 respectively.

1.3. GARBAGE OUTPUTS:

Garbage output is the unwanted or unread outputs which are needed to maintain the reversibility of the reversible gate (circuits). Number of garbage outputs for a particular reversible gate is not fixed, but any output that is not used in a circuit in which the gate is used is labelled garbage outputs.

1.4 APPLICATIONS:

Reversible logic has various applications in various fields like in Nano-technology, quantum computing, Low power CMOS, Optical computing and DNA computing, etc. Quantum computation is One of the most important applications of the reversible logic. Basically, reversible circuits do not lose information & reversible computation is performed only when system comprises of reversible gates. The reversible logic is design, main purposes are - decrease quantum cost, depth of the circuits & the number of garbage output.

2. LITERATURE SURVEY

2.1 REVERSIBLE UNIVERSAL SHIFT REGISTER (RUSR) USING NOVELREVERSIBLE GATES:

In 2017, maity has proposed the design of a 4-bit reversible universal shift register (RUSR) using novel reversible gates. The proposed design has its application in quantum computing by its lesser quantum cost (QC); less no. of the reversible logic gate and low garbage outputs (GO). They obtained QC as 68 and GO as 16. In previous designs, these are high that are 94 and 19 respectively.

The universal shift registers store binary data and its data can be shifted left or right when a clock signal is applied. All modes of operation such as SISO (serial-in-serial output), SIPO (serial-in-parallel output), PISO (parallel-in-serial output) and PIPO (parallel-in-parallel output) can also be performed upon the occurrence of clock. Thus, serial data (SIR during right shift and SIL during left shift) or parallel data can be loaded into shift register. The values of the select lines determine the operation to be performed as given in table 1. The existing design of Reversible Universal Shift Register in reference is basically built from basic cells comprising of DFF, Feynman gate (FG) and Fredkin gates. In the existing design fanout circuits are not used for any of the signals.

S1	S0	*Operation*
0	0	*No Change*
0	1	*Right Shift*
1	0	*Left Shift*
1	1	*Parallel Load*

TABLE 2.1: Operation of universal shift register

2.2 ARRAY MULTIPLIER USING REVERSIBLE LOGIC GATES:

In 2018, K. Yugandhar presented a design of a high-performance array multiplier using half adder and a full adder that is designed

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by using reversible logic gates. They designed a full adder using reversible multiplexers. This reversible multiplexer is designed by using the COG reversible gate. By the use of multiplexer-based design, the numbers of I/O buffers needed are reduced. So, they intend to decrease I/O buffer for reducing static power dissipation. They designed half adders using the Peres gate. By this design, the power consumption and delay are greatly reduced when compared to conventional logic. They greatly focused on reducing I/O buffers. In the future, they want to implement an 8-bit comparator using the same formula.

2.2.1FULL ADDER USING REVERSIBLE LOGIC:

The adder circuit play a major role in all arithmetic and logical operations in digital circuits .and also it placed a major Roll in processor memory organization by accessing the entire memory address with time multiplexed minimum address lines in early processors. The proposing adder called Reversible adder using multiplexers only some reversible multiplexers based full adder which we proposed shown in Fig 1 these full adders produce less power dissipation when compare to previous adder. First let's see what is multiplexer; A Multiplexer is a device which is used to selectively present output, based off the selection input provided. By cleverly manipulating the Input lines and the selection lines, we can simulate the logic behind many circuits using MUXes.

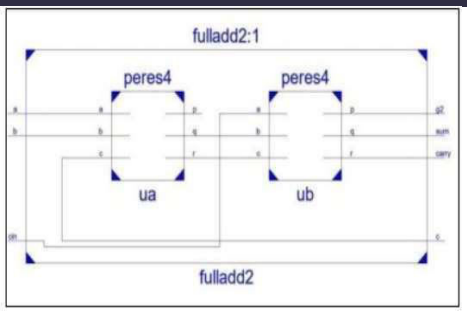

FIG 2.1: Full adder using reversible gates

2.2.2HALF ADDER USING REVERSIBLE LOGIC:

We proposed half adder using peres5 reversible gate. Here in peres5 reversible gate a, b and c are the inputs and P and Q are the outputs.
In which

P <= a,

Q<= a xor b,

R<= (a and b) xor c.

In the proposed half adder, A and B are inputs SUM and CARRY are outputs.

From the above reversible gate half adder function is justified.

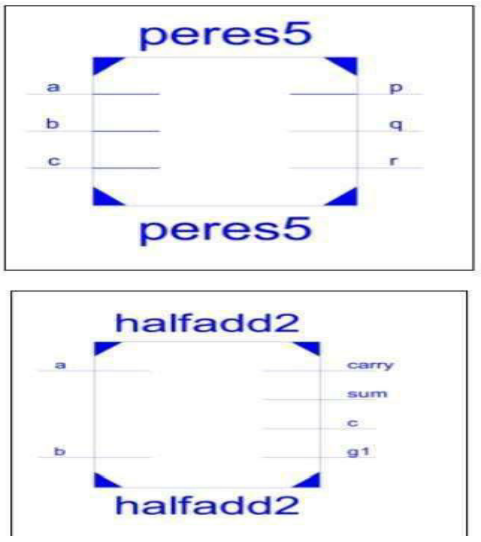

FIG 2.2: Half adder using reversible logic

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2.2.3ARRAY MULTIPLIER:

A multiplier is simply nothing but, it is a logic circuit which is doing multiplication of two or more numbers. If we talk about multiplier then we talk about multiplier from designer side but not from the user side. Here the multiplication operation is done on the numbers only logic 1 and logic 0 i.e., binary, because, the computer or logic circuit takes any number into binary form only. The logical multiplication is done on the basis of basic multiplication rules that are 0 x 0 = 0, 0 x 1 = 0, 1 x 0 = 0 and 1 x 1= 1. Suppose if we multiply two binary numbers 1011 and 1001 then from the above procedure result would be 01100011. It is an 8-bit number.

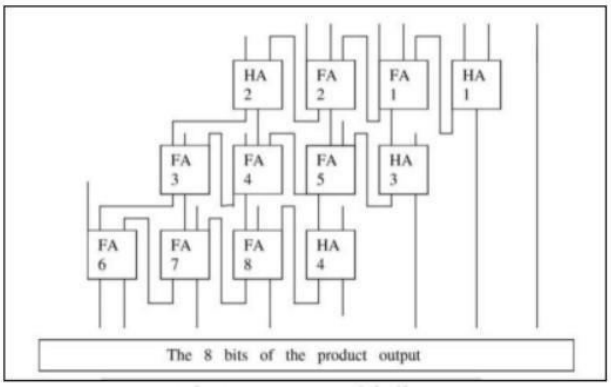

FIG 2.3: Array multiplier

2.3 ASYNCHRONOUS AND SYNCHRONOUS COUNTER USINGREVERSIBLE GATES:

In 2016, Rupali Singh has done their work in the field of reversible counters. They designed some modules like asynchronous counter and synchronous counter using reversible gates. From their design perspective, the counter has improved in terms of reversible gates count. And they showed their circuits would have less delay and reduced GO count and decreased circuit complexity. They obtained performance improvement of delay and GO as 44% and 31% respectively concerning previous designs.

2.4 D FLIP-FLOP, JK FLIP-FLOP, T-FLIP-FLOP BY THE USEOF NOVEL REVERSIBLE STRUCTURES:

In 2014, Mamataj has designed D flip-flop, JK flip-flop, T-flip-flop by the use of novel reversible structures. With these, they made two types of 4-bit decade counters called SCCDC and SGCCC. For SCCDC they obtained GC and GO as 25 and 36 respectively. For SGCCC they obtained GC and GO as 22 and 18

2.5 SIXTEEN-BIT BINARY SEQUENTIAL COUNTER USINGFEYNMAN AND FREDKIN GATES:

In 2014, Asima Jamal et.al [5] proposed the design of a sixteen-bit binary sequential counter using Feynman and Fredkin gates. In their design, it has one control input called UP/DOWN. It controls the operation of the up count or down count of the circuit. If you give control input as logic '1' to the UP/DOWN it acts as up counter. And if you give control input as logic '0' it acts as down counter operation. It is observed that in this paper is they compared their design perspectives with non-reversible circuits. And their circuits have less power consumption compared to others.

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2.6 DESIGN OF 4-BIT REVERSIBILITY SHIFT REGISTERS:

In 2011, Naga Pavani presented a paper that they were proposed a design of 4-bit reversibility shift registers which are compared with previous designs. They had presented the designs that are SISO, SIPO, PISO, and PIPO. These designs had the applications to compute S/P (serial to parallel) and P/S (parallel to Serial) conversion. For SISO, SIPO, PISO, PIPO they obtained GO as 5,5,10 and 9 respectively. They obtained huge improvement compared to previous designs.

Landauer stated that the amount of information is erased in the form of heat in irreversible circuits by KTln2. (K is Boltzmann constant and T is the room temperature). By this research only, the reversible circuits come out to this world.

3. PROPOSED SYSTEM

PROPOSED MODULES

PROPOSED REVERSIBLE GATES:

In the proposed system there are 8 different types of reversible gates. They are:

➢ FEYNMAN GATE

The Feynman gate has two inputs and two outputs i.e., 2X2 gate. The function of this gate is shown below. Here output P = A and Q= A (XOR) B. Feynman gate is also recognized as controlled- not gate (CNOT). This gate can be used to copy a signal. Since fan-out is not allowed in reversible logic circuits, the Feynman gate is used as the fan-out gate to copy a signal. Quantum cost of a Feynman gate is 1.

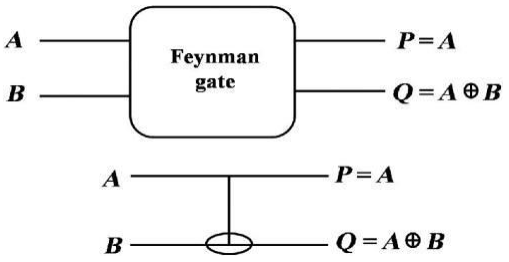

FIG: FEYNMAN GATE

➢ FREDKIN GATE

The Fredkin gate has three inputs and three outputs i.e., 3X3 gate. The function of this gate is shown below. Here outputs are P = A ,Q=A'B XOR AC and R=A'C XOR AB.

FIG : FREDKIN GATE

➢ PERES GATE

The peres gate has three inputs and three outputs i.e., 3X3 gate. The function of this gate is shown below. Here outputs are P = A ,Q=A XOR B and R=AB XOR C.

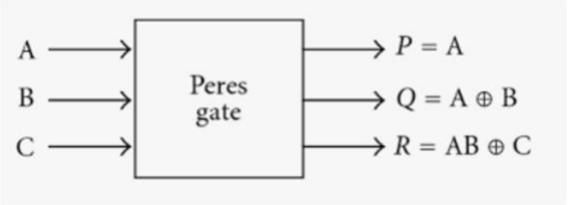

FIG: PERES GATE

➢ TG GATE

The TG gate has three inputs and three outputs i.e., 3X3 gate. The function of this gate is shown below. Here outputs are P = A, Q= B and R=AB XOR C.

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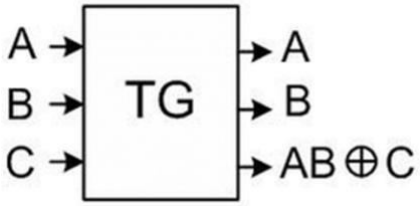

FIG : TG GATE

➢ **VGG GATE**

The proposed VGG gate has 4 inputs and 4 outputs i.e., 4X4 gate. Here the outputs P=A XOR BC, Q = B EXOR CD, R = C, AND S = D. The proposed gate is shown in the below diagram.

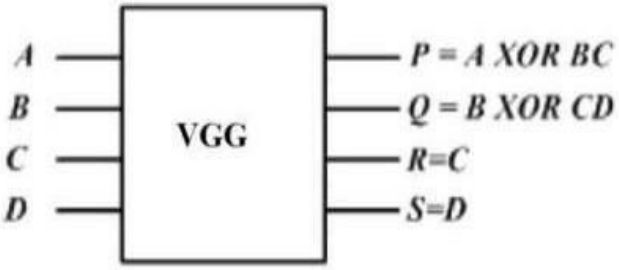

FIG: VGG GATE

➢ **GAN GATE**

The proposed GAN gate has 3 inputs and 3 outputs i.e., 3X3 gate. The function of this gate is shown below. Here P =! A, Q =! AB XOR A! C AND R =! AC XOR AB.

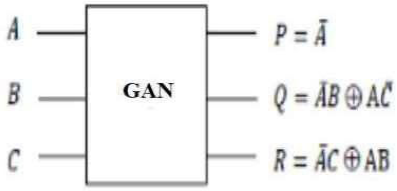

FIG 4.25: GAN GATE

➢ **MF GATE**

The proposed MF gate has 3 inputs and 3 outputs i.e., 3X3 gate. The function of this gate is shown below. Here P =A, Q= A'B XOR AC' AND R = A'C XOR AB.

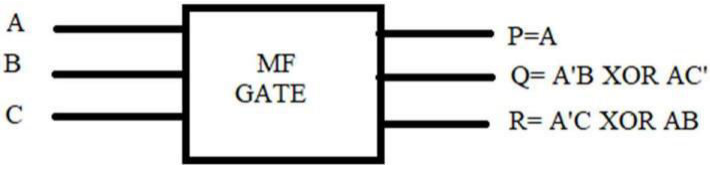

FIG: MF GATE

➢ TFG GATE

The proposed TFG gate has 4 inputs and 4 outputs i.e., 4X4 gate. The function of this gate is shown below. Here P =A, Q= B XOR A, R = AB XOR C and S= (AB XOR C) XOR D.

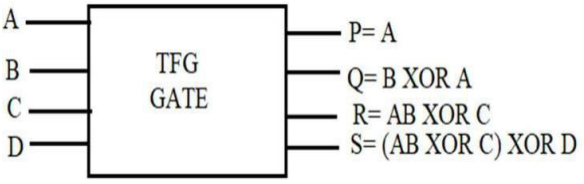

FIG: TFG GATE

2PROPOSED CIRCUITS:

2:4 DECODER:

The 2:4 Decoder is designed by using the three Fredkin gates. The 2:4 decoder is shown in the below figure

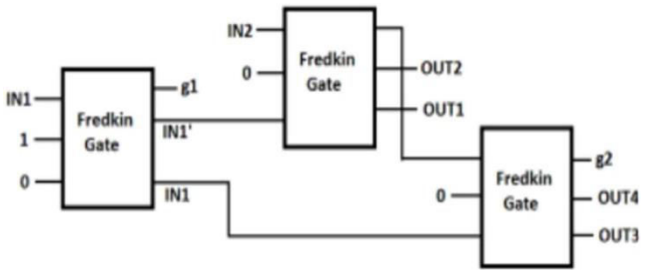

FIG 4.31: 2:4 DECODER

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3:8 DECODER USING 2:4 DECODER:

The 3:8 Decoder is designed by using the 2:4 decoder andfour Fredkin gates. The 3:8 decoder is shown in the below figure.

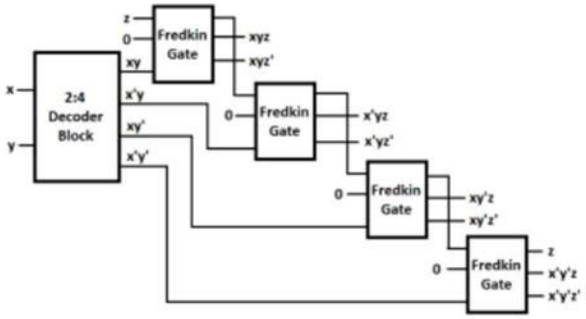

FIG : 3:8 DECODER USING 2:4 DECODER

FULL ADDER USING 3:8 DECODER:

A Full adder is designed using 3:8 decoder which is implemented by reversible gates as shown in the below figure.

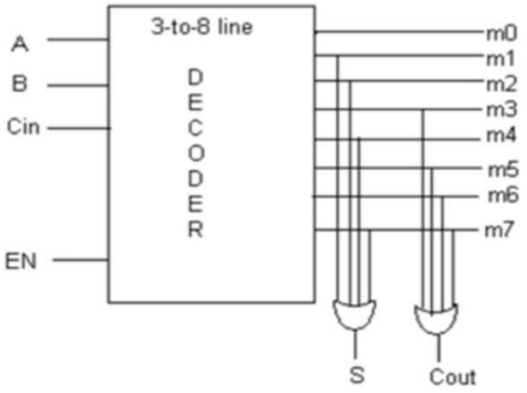

FIG 4.33: FULL ADDER USING 3:8 DECODER

FULL SUBTRACTOR:

A Full subtractor is designed using 3:8 decoder which is implemented by reversible gates as shown in the below figure.

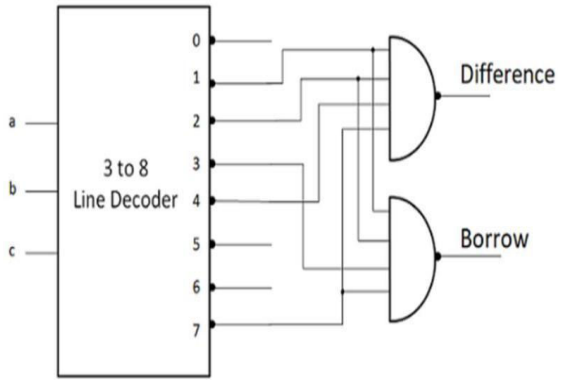

FIG 4.34: FULL SUBTRACTOR USING 3:8 DECODER

ONE BIT COMPARATOR:

A One-bit comparator is designed using a Feynman, a peres and a BJN gate as shown in the below figure.

FIG 4.35: ONE BIT COMPARATOR

4.2.2.6 D-LATCH:

A D-Latch is designed using an MF gate and two Feynman gates as shown in the figure below.

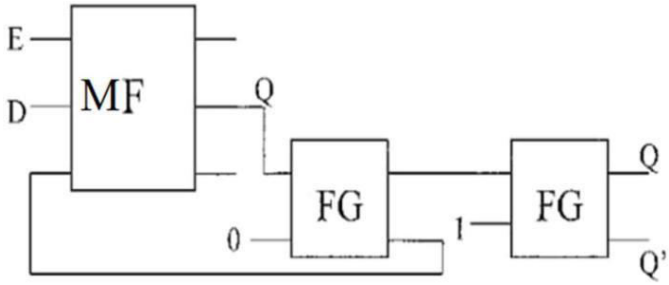

FIG 4.36: D LATCH

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4.2.2.7 SERIAL IN SERIAL OUT(SISO):

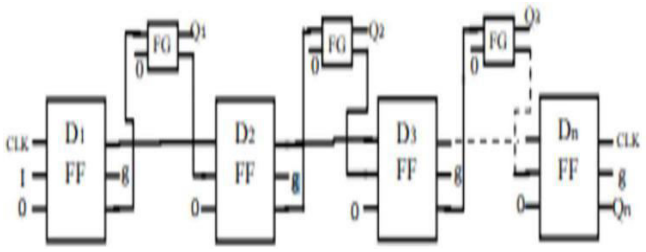

FIG 4.37: SERIAL IN SERIAL OUT.

4. CONCLUSION

In this paper, the modules presented are, that are proposed namely 2:4 Decoder, 3:8 Decoder, One Bit comparator, D-latch, SISO (Serial in Serial Out). These proposed modules are had less power consumption and fewer garbage outputs that means lesser delays. In the future, more work can be done on Power efficient, delay efficient Circuits using reversible gates.

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