International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

IJIEMR Transactions, online available on 8 June 2017. Link :
http://www.ijiemr.org/downloads.php?vol=Volume-6&issue=ISSUE-4

Title: **Design of F.T barrel Shifter Using 3 Input/Output Fredkin Gate.**

Volume 06, Issue 04, Pages: 729 – 735.

Paper Authors

*** MATTUPALLI.V.AJAY KUMAR, K.RAJKAMAL.**

*DEPT OF ECE , GUNTUR ENGINEERING COLLEGE.

.

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

DESIGN OF F.T BARREL SHIFTER USING 3 INPUT/OUTPUT FREDKIN GATE

MATTUPALLI.V.AJAY KUMAR
M.TECH – SCHOLAR – E.C.E
Dept. of E.C.E
GUNTUR ENGENERING COLLEGE
GUNTUR DT.

K.RAJKAMAL, M.Tech, [PH.D]
ASSOCIATE PROFESSOR
Dept. of E.C.E
GUNTUR ENGENERING COLLEGE
GUNTUR DT.

ABSTRACT: The logic of the reversible attains the supremacy in the sphere of overwhelming research in logic synthesis and also has the significant role in the quantum computing context because of loss-less information processing. Due to low power dissipation, the smaller components are first designed by the researchers with reversible gates that eventually lead to design reversible computer. We are going to propose in this paper, architecture's robust of logarithmic barrel shifter that performs bidirectional logical shifting and arithmetic, including the operation of rotate including error detection and correction with incorporating fault tolerance capability, the circuit is designed an fully professionally which exhibits greater performance over state-of-the-art design methods in terms of minimum gates in number, outputs of garbage's, inputs of ancilla, quantum cost, delay and others cost factors.

Keywords- barrel shifters, quantum cost, ancilla bits.

I.INTRODUCTION

According to Moore's law [1], the transistor count is doubled in every two years and the performance of it is continue to be dominate until semiconductor circuits reach its physical limit. Further, kT*log2 joules energy per bit information loss [2] is necessarily generated by irreversible logic computation , where T is the absolute room temperature and k is Boltzmans constant. On the other hand, Reversible Computing does not erase information, and performs numerous operations in a cycle of single and it is easily compliant to Fault Testing [3]. In terms of hardware design, computation of binary is favored over computation of decimal which is due to the ease of building hardware for binary number. Though, the requirement is approximation whilst performing computation in binary hardware because of incurs of complexity in the representation of most of the decimals numbers of fractional. Shifting is considered as the most powerful bit-wise operation amongst all computing system of high speed. Two well-known types of shifting circuits: Logarithmic [4] and Array shifters [5]. Generally, the shifter of the Logarithmic barrel is used widely because of its simplicity and robustness. There exists numerous methodologies to design the shifter of the barrel in reversible domain,

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

albeit each of them posses limitation to be considered as full-fledged reversible Barrel shifter. This paper attempts to overcome the limitations of the existing design approaches and improve the accuracy of the circuit.

II.REVERSIBLE GATES

A ***Reversible Gate*** is an n-output (denoted by *n* * *n*) and n-input circuit. Several dummy output signals are needed to maintain the property of reversibility for the reversible gates of logics to produce in order to equality in the input number to that of output. These signals are commonly known as ***Garbage Outputs***. For instance, for the operation of Exclusive-OR of reversible, Feynman gates are used which produce an extra dummy output along with its signal of principal output to defend reversibility. The quantum cost of reversible gate is equal to the number of 1x1 and 2x2 gates of reversible are required to be designed a 3x3 reversible gate. The quantum cost of all 1x1 and 2x2 reversible gates are going to consider as the unity of [18], [7], [2]. The gates of reversible of 3x3 are designed from 1x1 NOT gate, and 2x2 gates of reversible such as Controlled-V+ and Controlled-V (V+ is a square-root of NOT gate and V, the Feynman gate which is also known asthe gate of Controlled NOT.

A gate of NOT is 1x1 gate represented as shown in Fig. 1. Its cost of quantum is unity, because it is the gate of 1x1.

Fig. 1. GATE of NOT

For 2*2***Feynman Gate (FE)*** the input vector , Iv and output vector, Ov is defined as follows: *Ov = (P = A* and *Q=A ^B)* and *Iv = (A, B).* Feynman gates are typically used as copying gates. *Ov = (P =A* and *Q=A)*If *Iv = (A, B=0).* Inreversible logic Fanout is not allowed. Feynman gate is helpful in this view since it can be useful for signal copying by which it avoids the fanout problem as shown in Fig.2(c).

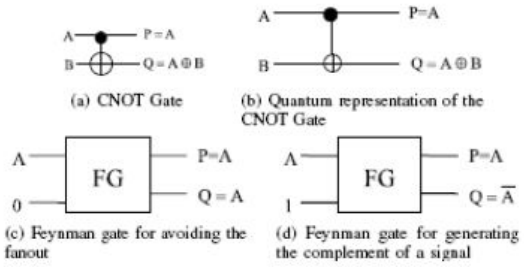


Fig. 2. Quantum implementation

The input and output vector for 3*3 ***Fredkin gate (FR)*** [1] are defined as follows: *Iv = (A, B,C)* and *Ov=(P=A, Q= A'B^AC* and *R = A'C ^ AB).* Figure 3(a) shows the block diagram of a Fredkin gate. A Fredkin gate can work as 2:1 MUX, as it is able to swap its other two inputs depending on the value of its first input. The first input A works as a controlling input while the inputs B and C work as controlled inputs as shown in the Fig. 3(a). Thus when A=0 the outputs P and Q will be directly connected to inputs A and B and if A=1 the inputs B and C will be swapped resulting in the value of the outputs as Q=C and R=B. The quantum implementation of a Fredkin gate with a quantum cost of is shown in Figure 3(b) [7]. In Fig. 3(b) each dotted rectangle is equivalent to a 2x2 Feynman gate and the

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

quantum cost of each dotted rectangle is considered as 1[18]. The same assumption is used for calculating the quantum cost of the Fredkin gate [7]. Thus, the quantum cost of the Fredkin gate is 5 as it consists of 2 dotted rectangles, 1 Controlled-V gate and 2 CNOT gate.

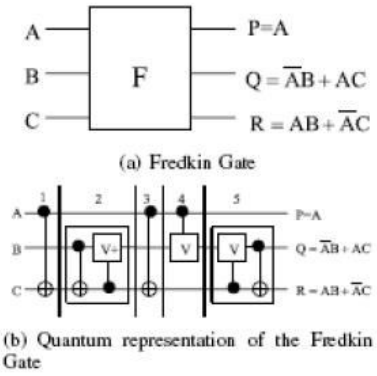


Fig. 3. Fredkin Gate and its quantum implementation

III.BIDIRECTIONAL BARREL SHIFTER

A combinational circuit known as a barrel shifter which has n-input and n-output and m select lines that controls bit shift operation. A barrel shifter having n inputs and k select lines is called (n,k) barrel shifter. Barrel shifter can be unidirectional allowing data to be shifted or rotated only to left (or right), or bi-directional which provides data to be rotated or shifted in both the directions. The logarithmic barrel is the most widely used among the different designs of barrel shifter, because of its less area, simple design and the elimination of the decoder circuitry. An n-bit logarithmic barrel shifter has a total of log2(n) stages. Each stage determines whether to shift or not to shift the input data. The stage *k* will shift the input 2□times if the control bit *sk* (where*k = 0, 1, ... (log2(n)-1)*) is set to 1otherwise the input will remain unchanged. Logarithmic shifter is more efficient in terms of design as well as area but delay cost is large [11]. This paper presents the designs of reversible bidirectional arithmetic and logical barrel shifter that can perform six operations: logical right shift, arithmetic right shift, right rotate, logical left shift, arithmetic left shift and left rotate. The existing shifter is a unidirectional logarithmic shifter consists of multiplexers. A 3x3 Fredkin Gate works as simple (2:1)multiplexers. Feynman gates are used for producing fan outs. The existing shifter is complex in design and requires large number of gates. As a result the total number of garbage outputs is high. Thus there is great room for improving the circuit complexity, total number of gates and garbage outputs, delay and quantum cost. For efficient designing of a reversible circuit several criteria are needed to be considered:

a. Minimize the number of gates as possible.
b. Minimize the quantum cost of the circuit.
c. Total number of garbage outputs and usage of constant inputs should be minimized.

IV.DESIGN OF REVERSIBLE BIDIRECTIONALBARREL SHIFTER

The proposed design of reversible bidirectional barrel shifter can perform logical right shifting, arithmetic right shifting, rotating right, logical left shifting, arithmetic left shifting and rotating left operations. The proposed reversible bidirectional arithmetic and logical barrel shifter design approach

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

The design of a reversible barrel shifter can be divided into six modules: (i) Data reversal control unit-I,(ii) Arithmetic right shift control unit, (iii) Shifter or rotation unit which consists of three sub-modules that performs Stage I, Stage II and Stage III operations, (iv)Rotation unit, (v) Arithmetic left shift control unit, (vi)Data reversal control unit-II. The working of the reversible design ofthe modules of the reversible bidirectional barrel shifter are explained as follows:

1. Data Reversal Control Unit-I

In reversible barrel shifter the direction of the shift operation performed is controlled by the control signal left as shown in the Table I. The reversible bidirectional barrel shifter performs the shift operation in the left direction if the value of control signal left as 1, that is, the arithmetic left shift operation or logical left shift operation. Otherwise, the shift operation is performed in the right direction for the value of left=0, that is arithmetic right shift operation or logical right shift operation.

Arithmetic Right Shift Control Unit

The reversible arithmetic right shift control unit isshown in Fig.4. The arithmetic right shift operation iscontrolled by the arithmetic right shift control unit.

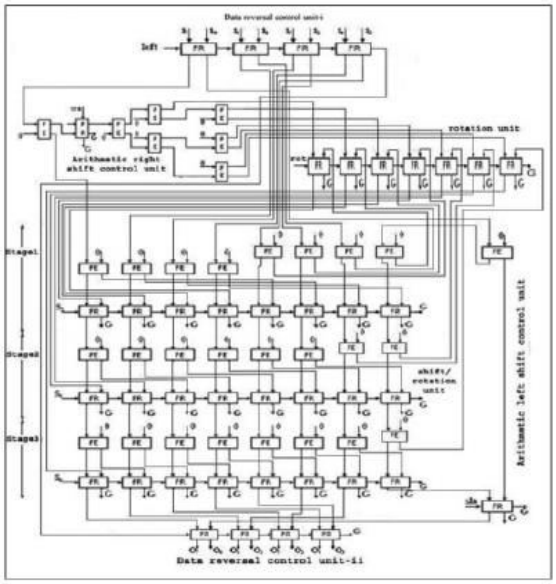


Fig. 4 Proposed reversible bidirectional barrel shifter

The designing of this unit is done using a single Fredkin gate controlled by the control signal sra, and preserves the sign bit of input data. The arithmetic right shift operation is performed if the value of control signal sra= 1, otherwise it simply passes the data to the next module. Multiple copies of the sign bit are created using the Feynman gates because fanout is not allowed inreversible logic.

2. Shifter Or Rotation Unit

The three stage design of the reversible shifter or rotation unit id as shown in Fig. 4. The amount of shift operation that has to be performed is done by the shifter unit in the design of reversible bidirectional barrel shifter. This unit is controlled by the control signals S2,S1 and S0. This unit can be divided into three stages. Depending on the value of control signal S2, S1 and S0,the first, second and the third stages of this unit right shifts the input data by 2^2, 2^1 and 2^0 bits respectively.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

3. *Rotation Unit*

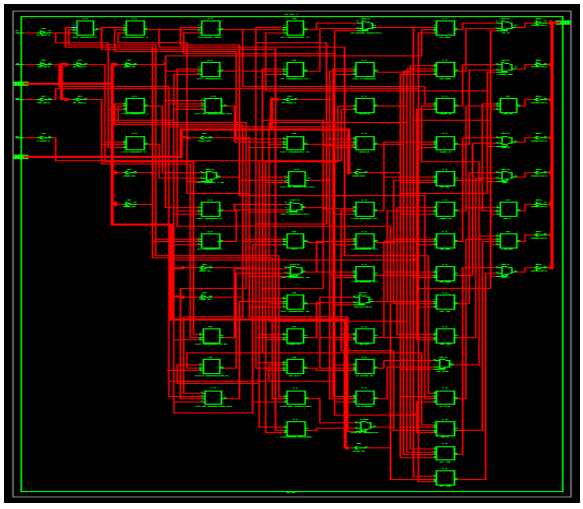
The rotation unit is shown in Fig.4. The rotation operation is controlled by the rotation unit. The designing of this unit is done using a chain of 8 Fredkin gates and controlled by the control signal rot, and performs the rotation operation of input data. The rotation operation is performed if the value of control signal rot = 1, otherwise it simply passes the data to the next module.

4. *Arithmetic Left Shift Control Unit*

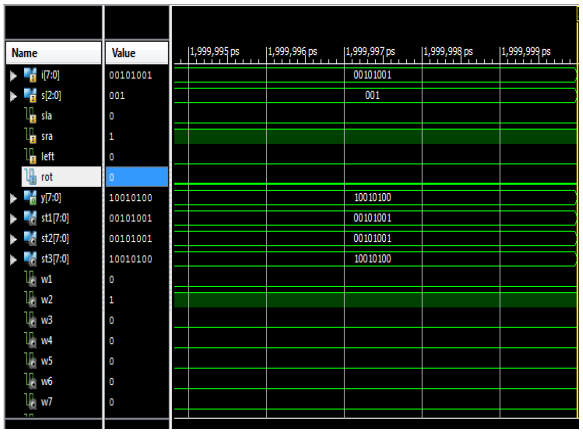
The arithmetic left shift control unit is shown in the Fig. 4. The design of the arithmetic left shift control unit and the design of the arithmetic right shift control unit are same. This control unit is controlled by the control signal sla and is responsible to perform the arithmetic left shift operation. This unit is implemented using asingle Fredkin gate. This unit preserves the sign bit needed to perform the arithmetic left shift operation if the value of control signal sla = 1, else it simply passes the LSB of the shifter or rotation unit.

V.RESULTS

TECHNOLOGY SCHEMATIC



OUTPUT WAVEFORM



VI.CONCLUSIONS

In this paper An Efficient Design of Reversible Logic Based Bidirectional Barrel Shifter has been proposed. The design of the proposed bidirectional shifter is done using Fredkin gates and Feynman gates. The number of garbage outputs, the number of ancilla inputs and the quantum cost of the (n,k) reversible bidirectional barrel shifter increase more rapidly by varying n and keeping k as a constant compared to the designs in which n is kept as a constant while k is varied. The proposed design of the reversible barrel shifters performs the functional verification through simulations using the Verilog HDL flow for reversible circuits with error correction and detection circuit. The design of bidirectional barrel shifter is been evaluated in terms of garbage outputs, ancilla inputs and the quantum cost. The proposed design of reversible bidirectional barrel shifter form logical right shifting, arithmetic right shifting, rotating right, logical left shifting, arithmetic left shifting and rotating left operations with error corrections in all levels of operations.

REFERENCES

[1] E. Fredkin and T. Toffoli, "Conservative logic,"International J. Theor. Physics, vol. 21, pp. 219–253, 1982.

[2] H. Thapliyal and N. Ranganathan, "Design ofefficient reversible binary subtractors based on anew reversible gate," in Proc. the IEEE ComputerSociety Annual Symposium on VLSI, Tampa,Florida, May 2009, pp. 229–23.

[3] C.H. Bennett, "Logical reversibility ofcomputation," IBM J. Research andDevelopment, vol. 17, pp. 525–532, Nov. 1973.

4] R. Landauer, "Irreversibility and heat generationin the computational process," IBM J. Researchand Development, vol. 5, pp. 183–191, Dec.1961.

[5] A. Peres, "Reversible logic and quantumcomputers," Phys. Rev. A, Gen. Phys., vol. 32,no. 6, pp. 3266–3276, Dec. 1985.

[6] T. Toffoli, "Reversible computing," MIT Lab forComputer Science, Tech. Rep. Tech memoMIT/LCS/TM-151, 1980.

[7] W. N. Hung, X. Song, G.Yang, J.Yang, and M.Perkowski, "Optimal synthesis of multiple outputboolean functions using a set of quantum gates bysymbolic reachability analysis," IEEE Trans.Computer-Aided Design, vol. 25, no. 9, pp.1652–1663, Sept. 2006.

[8] S. Kotiyal, H. Thapliyal, and N. Ranganathan"Design of a reversible bidirectional barrelshifter," in Proceedings of the 11th IEEEInternational Conference on Nanotechnology,Portland, Oregon, USA, Aug 2011, pp. 463-468.

[9] M. A. Nielsen and I. L. Chuang, QuantumComputation and Quantum Information. NewYork: Cambridge Univ. Press, 2000.

[10] S. Kotiyal, H. Thapliyal, and N. Ranganathan,"Design of a ternary barrel shifter using multiplevaluedreversible logic," in Proceedings of the10th IEEE International Conference onNanotechnology, Seoul, Korea, Aug. 2010, pp.1104–1108.

[11] S.Gorgin and A. Kaivani, "Reversible barrelshifters," in Proc. 2007 Intl. Conf. on ComputerSystems and Applications, Amman, May 2007,pp. 479–483.

[12] V. Vedral, A. Barenco, and A. Ekert, "Quantumnetworks for elementary arithmetic operations,"Phys. Rev. A, vol. 54, no. 1, pp. 147–153, Jul1996.

[13] H. Thapliyal and N. Ranganathan, "Design ofreversible sequential circuits optimizing quantumcost, delay and garbage outputs," ACM Journalof Emerging Technologies in ComputingSystems, vol. 6, no. 4, pp. 14:1–14:35, Dec. 2010.

[14] N. Nayeem, M. Hossain, L. Jamal, and H. Babu,"Efficient design of shift registers usingreversible logic," in 2009 InternationalConference on Signal Processing Systems, may2009, pp. 474 – 478.

[15] I. Hashmi and H. Babu, "An efficient design of areversible barrel shifter," in VLSI Design, 2010.VLSID '10. 23rd International Conference on,Jan 2010, pp. 93 –98.

[16] H. Thapliyal and N. Ranganathan, "Design ofefficient reversible logic based binary and bcdadder circuits," To appear

ACM Journal ofEmerging Technologies in Computing Systems,2011.

[17] M. H. Khan and M. A. Perkowski, "Quantumternary parallel adder/subtractor with partiallylook-ahead carry," vol. 53, no. 7, 2007, pp. 453 –464.

[18] J. A. Smolin and D. P. DiVincenzo, "Five two-bitquantum gates are sufficient to implement thequantumfredkin gate," Physical Review A, vol.53, pp. 2855–2856, 1996.