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DESIGN OF FAULT TOLERANT PARALLEL FILTERS USING PARSEVAL CHECKS

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ABSTRUCT:
Digital filters are widely usedin mostsignal processing and communication systems. Tolerant filter implementations are needed for the reliability of those systems because there are critical in some cases and fault. To achieve fault tolerance many techniques that exploit the filters structure and properties have been proposed over the years. It enables more complex systems as technology scales that incorporate many filters. It is common in those complex systems that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, to achieve fault tolerance a simple technique that exploits the presence of parallel filters has been proposed. To show that using error correction codes (ECCs)the parallel filters can be protected in which each filter is the equivalent of a bit in a traditional ECC is discussed and this is the idea generalized. When the number of parallel filters is large the new scheme allows more efficient protection. The technique is evaluated using a case study of parallel finite impulse response filters showing the effectiveness in terms of protection and implementation cost
.

Keywords: filters, Error correction codes(ECCs), soft errors.

INTRODUCTION: Electronic circuits are increasingly present in automotive, medical and space applications where reliability is critical. In those applications, the circuits have to provide some degree of fault tolerance. This need is further increased by the intrinsic reliability challenges of advanced CMOS technologies that include, e.g., manufacturing variations and soft errors. A number of techniques can be used to protect a circuit from errors. Those range from modifications in the manufacturing process of the circuits to reduce the number of errors to adding redundancy at the logic or system level to ensure that errors do not affect the system functionality.Triple modular redundancy (TMR) is a general technique used to add redundancy.

The TMR, which triplicates the design and adds voting logic to correct errors, is commonly used. However, it more than triples the area and power of the circuit, something that may not be acceptable in some applications. When the circuit to be protected has algorithmic or structural properties, a better option can be to exploit those properties to implement fault tolerance. One example is signal processing circuits for which specific techniques have been proposed over the years. Digital filters are one of the most commonly used signal processing circuits and several techniques have been proposed to protect them from errors. Most of them have focused on finite-impulse response (FIR) filters. For example, the use of reduced precision replicas was proposed to reduce the cost of implementing modular redundancy in FIR filters. In a relationship between the memory elements of an FIR filter and the input sequence was used to detect errors. The FIR properties have been exploited by other schemes at a word level to also achieve fault tolerance. The use of residue number systems and arithmetic codes has also been proposed to protect filters. Finally, the use of different implementation structures of the FIR filters to correct errors with only one redundant module has also been proposed. In all the techniques mentioned so far, the protection of a single filter is considered. However, it is increasingly common to find systems in which several filters operate in parallel. This is the case in filter banks and in many modern communication systems

. The protection of the filters can be addressed at a higher level for those systems by considering the parallel filters as the block to be protected. Two parallel filters with the same response that processed different input signals were considered and this is the idea that explored in. It was shown that with only one redundant copy, single error correction can be implemented. Therefore, a significant cost reduction compared with TMR was obtained. To protect parallel filters a general scheme is presented. As in, parallel filters with the same response that process different input signals are considered. The new approach is based on the application of error correction codes (ECCs) using each of the filter outputs as the equivalent of a bit in and ECC codeword. This is a generalization of the scheme presented in and enables more efficient implementations when the number of parallel filters is large. The scheme can also be used to provide more powerful protection using advanced ECCs that can correct failures in multiples modules. The rest of this brief introduces the new scheme by first summarizing the parallel filters considered in Section 2. Then, in Section 3, the proposed scheme is presented. Section 4 presents a case study to illustrate the effectiveness of the approach. Finally, the conclusions are summarized in Section 5.

Parallel Filters with the Same Response:

A discrete time filter implements the following equation:

$$y[n]= \sum_{l=0}^{\infty} x[n-l].h[l] \qquad (1)$$

where $x[n]$ is the input signal, $y[n]$ is the output, and $h[l]$ is the impulse response of the filter. When the response $h[l]$ is nonzero, only for a finite number of samples, the filter is known as a FIR filter, otherwise the filter is an infinite impulse response (IIR) filter. To implement both FIR and IIR filters there are several structures.

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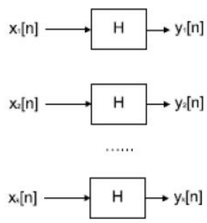

Fig. 1. Parallel filters with the same response

A set of *k* parallel filters with different input signals and same response are considered in the following. These parallel filters areillustrated in Fig. 1. This kind of filter is found in some communication systems that use several channels in parallel. In data acquisition and processing applications is also common to filter several signals with the same response. By adding the corresponding inputs Xi[n] and filtering the resulting signal with the same filter h[l] the sum of any combination of the outputs Yi[n] is obtained and this is the interesting property of these parallel filters. For example

$$y_1[n]+y_2[n] = \sum_{l=0}^{\infty}(x_1[n-l]+x_2[n-l]).h[l] \quad (2)$$

This simple observation will be used in the following to develop the proposed fault tolerant implementation.

Fault Tolerance System:

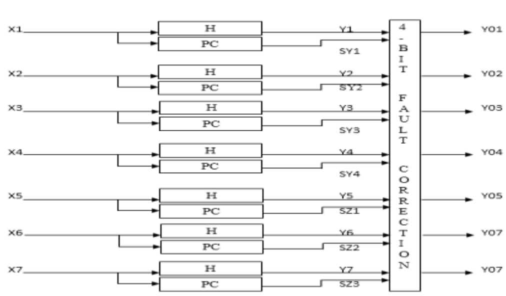

Fig 2 fault tolerant parallel filter using parseval checks

In the event of the failure of (or one or more faults within) some of its components the property that enables a system to continue operating properly is the fault tolerance. As compared to a naively designed system in which even a small failure can cause total breakdown and the decrease is proportional to the severity of the failure if its operating quality decreases. In high-availability or life-critical systems the fault tolerance is particularly soughed. The graceful degradation is the ability of maintaining functionality when portions of a system break down.

Possibly at a reduced level, rather than failing completely a fault tolerant design enables a system to continue its intended operation, when some part of the system fails. The term is most commonly used to describe computer systems designed to continue more or less fully operational with, perhaps, a reduction in throughput or an increase in response time in the event of some partial failure. That is, the system as a whole is not stopped due to problems either in the hardware or the software. A motor vehicle designed is example in another field so it will continue to be drivable if one of the tires is punctured. A structure is able to retain its integrity in the presence of damage due to causes such as fatigue, corrosion, manufacturing flaws, or impact This invention relates to forward error correction and detection codes, and more particularly to a forward error correction and detection code method and apparatus having parity check bits (or symbols) added to information bits (or symbols) to form a code word.

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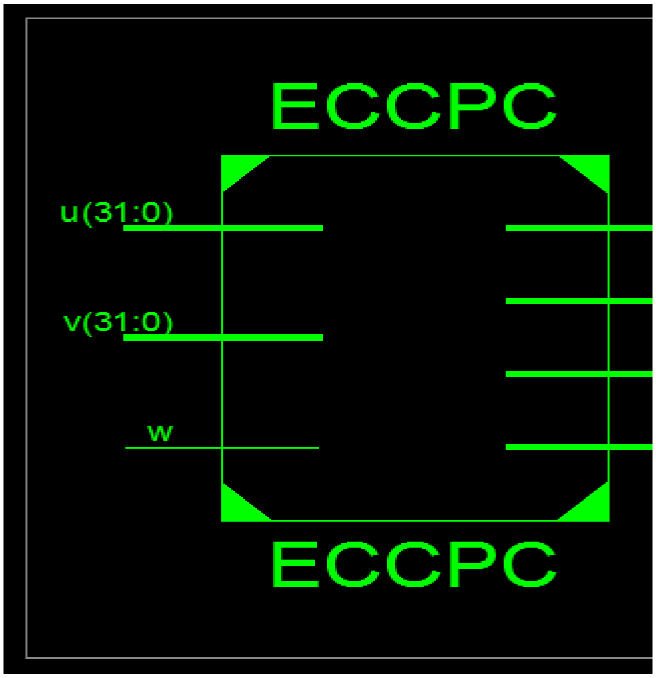
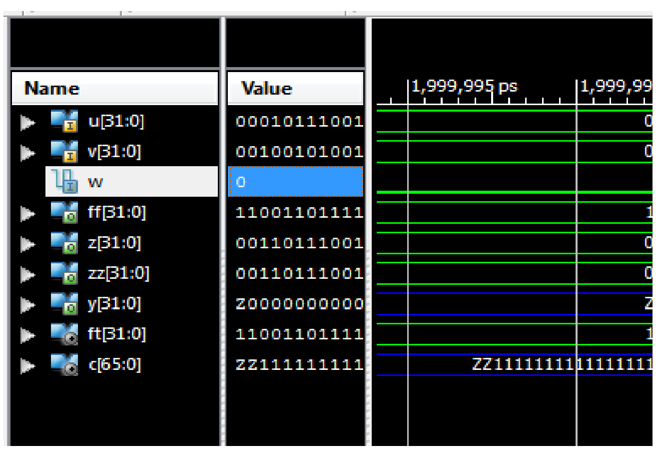
RESULTS:

RTL SCHEMATIC





CONCLUSTION:

To protect parallel filters a new scheme is presented that are commonly found in modern signal processing circuits. To detect and correct errors the approach is based on applying ECCs and the parallel filters outputs. For parallel filters that have the same response and process different input signals the scheme can be used. Multi-bit errors is detected by TMR method, in any filters but consumes more area and power whereas ECC scheme can detect and correct only single bit error.

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