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DESIGN AN BYPASS MULTIPLIER FOR WIRELESS COMMUNICATION

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ABSTRACT: Redundant Based Multiplier Over Gaulo is Field (GF(2m)) has gained more popularity in elliptic curve cryptography (ECC) mainly due to their negligible hardware cost for squaring and modular reduction. In this paper, we have proposed a novel recursive decomposition algorithm for RB multiplication to obtain high throughput digit-serial implementation. Depends up on a specific feature of redundant representation in a class of finite fields, two new multiplication algorithms along with their pertaining architectures are proposed to alleviate this problem. Consider an area-delay product as a measure of evaluation, it has been shown that both the proposed architectures considerably outperform existing digit-level multipliers by utilizing the same basis. It is also shown that for a subset of the fields, the proposed multipliers are of higher performance in terms of area-delay complexities among several recently proposed optimal normal basis multipliers. The main characteristics of the post place & route application specific integrated circuit implementation of the proposed multipliers for three practical digit sizes are also reported.

KEYWORDS: Digit-level architecture, finite field arithmetic, multiplication algorithm, redundant representation.

I. INTRODUCTION

Digital multipliers are among the most critical arithmetic functional units in many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The through put of these applications depends on multipliers, and if the multipliers are too slow, the performance of entire circuits will be reduced. Furthermore, negative bias temperature instability (NBTI) occurs when a pMOS transistor is under negative bias (Vgs = −Vdd). In this situation, the interaction between inversion layer holes and hydrogen-passivity Si atoms breaks the Si–H bond generated during the oxidation process, generating H or H2 molecules [1]. When these molecules diffuse away, interface traps are left. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage (Vth), reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing the NBTI effect. However, the reverse reaction does not eliminate all the interface traps generated during the stress phase, and Vth is increased in the long term [2].

Hence, it is important to design a reliable high-performance multiplier. The corresponding effect on an nMOS transistor is positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias [3]. Compared with the NBTI effect, the PBTI effect is much smaller on oxide/polygate transistors, and therefore is usually ignored. However, for high-k/metal-gate nMOS transistors with significant charge trapping, the PBTI effect can no longer be ignored. In fact, it has been shown that the PBTI effect is more significant than the NBTI effect on 32-nm high- k/metal-gate processes. A traditional method to mitigate the aging effect is overdesign, including such things as guard-banding and gate over sizing; however, this approach can be very pessimistic and area and power inefficient. To avoid this problem, many NBTI- aware methodologies have been proposed [4]. An NBTI-aware technology mapping technique was proposed in to guarantee the performance of the circuit during its lifetime. In this paper, we propose an aging-aware reliable multiplier design with novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects

II. LITERATURE SURVEY

Due to aggressive scaling of device geometries continues to diminish with the developments in fabrication technology, the ensuing processors square measure progressively changing into vulnerable to effects like aging. Moreover, negative bias temperature instability (NBTI) happens once a PMOS junction transistor is beneath negative bias ends up in aging result [5]. Aging result degrades junction transistor speed by increase in threshold voltage, which ends up in real time delay issues. The corresponding result on associate nMOS junction transistor is positive bias temperature instability (PBTI) that happen once associate nMOS junction transistor is beneath positive bias. Integrated-circuit aging phenomena discovered in sub-90nm CMOS technologies square measure as follows:

2.1 Hot Carrier Injection (HCI): Hot carriers square measure particles that get a awfully high K.E. from being accelerated in a very high field. These energetic carriers may be injected into `forbidden' region of the device like the gate compound, rather than following their meant mechanical phenomenon. Once injected into such a vicinity they will get treed or cause the generation of interface states. These defects successively result in shifts within the electrical characteristics of the semiconductor unit like a shift of the Vth, this issue β and also the output electrical phenomenon goes. Hence, HCI became less of a problem. HCI will still be a drag since provide voltage scaling is deceleration down due to the non-scalability of the sub-threshold slope [6]. HCI is primarily a drag in nMOS devices though pMOS devices square measure less sensitive to HCI, the result will enhance alternative aging effects like negative bias temperature instability (NBTI).

2.2 Time-Dependent Dielectric Break-down (TDDB): The correct operation of a MOS semiconductor unit electronic transistor semiconductor device semiconductor unit semiconductor depends on the insulating properties of the stuff layer

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below the gate conductor of the transistor. Every stuff material encompasses a most field of force within which it will sustain. Once a bigger field of force is applied, this ends up in arduous Breakdown (HBD). HBD is a particularly native development, characterized by a loss of the gate compound insulating properties and permitting an outsized gate current to flow. At lower electrical fields, the stuff will wear-out when a while and at last break down fully. This can be known as Time Dependent stuff Breakdown (TDDB) [7].

2.3 Bias Temperature Instability (BTI):- Bias Temperature Instability (BTI) has gained plenty of attention because of its more and more adverse impact in nano-meter CMOS technologies. It's a threshold voltage (Vth) shift once a bias voltage has been applied to a MOS gate at elevated temperature [8]. It causes threshold voltage (Vth) increments to the MOS transistors. Threshold voltage Vth increment during a exceedingly in a very pMOS semiconductor electronic transistor semiconductor device semiconductor unit semiconductor that happens underneath the negative gate stress is remarked as Negative Bias Temperature Instability (NBTI) and therefore the one that occur in an nMOS transistor underneath positive gate stress is thought as Positive Bias Temperature Instability (PBTI). The NBTI or PBTI impact will become a lot of important reckoning on the material kind. For a MOS semiconductor unit, there square measure 2 BTI phases. a. Stress part. b. Relaxation part. These 2 phases dissent by the gate biasing (i.e. VDD or –VDD) of the MOS transistors.

2.4 Electro-migration (EM): Electro-Migration (EM) is associate degree aging impact going down in interconnect wires, contacts associate degreed via in an computer circuit. The impact causes material transport by gradual movement of the ions during a conductor because of the momentum transfer between conducting electrons and therefore the diffusive metal atoms. EM is very important in applications wherever high electricity densities area unit used. These aging effects area unit caused because of scaling of transistors in VLSI chips. The device aging causes loss on circuit performance and lifelong that area unit the most factors within the responsibility degradation of VLSI circuit. Thus, to cut back this aging impact on CMOS, associate degree adaptive Hold Logic (AHL) circuit is based to be a lot of economical than different ways [10].

III.PROPOSED ARCHITECTURE

One column-or row-bypassing multiplier, two m-bit inputs (m is a positive number), one $2m$-bit output, $2m$ 1-bit Razor flip-flops, and an AHL circuit which included in proposed architecture. Our proposed architecture overall flow is as follows: the AHL circuit and the column- or row-bypassing multiplier execute simultaneously when input patterns arrive. The AHL circuit decides if the input patterns require one or two cycles according to the number of zeros in the multiplicand (multiplicator). The AHL will output 0 to disable the clock signal of the flip-flops if the input pattern requires two cycles to complete. Otherwise, for normal operations the AHL will output 1. The result will be passed to the Razor flip-flops when the column- or row- bypassing multiplier finishes the operation. Whether there is the path delay timing violation is checked by the Razor flip-flops. For the current operation the cycle period is not long enough to complete if timing violations occur and that the execution result of the

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multiplier is incorrect. Thus, the current operation needs to be re-executed to ensure the operation is correct using two cycles to inform the system that the Razor flip-flops will output an error. In this situation, the extra re-execution cycles which is caused by timing violation incurs a penalty to overall average latency. However, whether the input patterns require one or two cycles can accurately predicted by our proposed AHL circuit in most cases. When the AHL circuit judges incorrectly only then it caused to timing variation for a few input patterns. In this case, the extra re-execution cycles did not produce significant timing degradation.

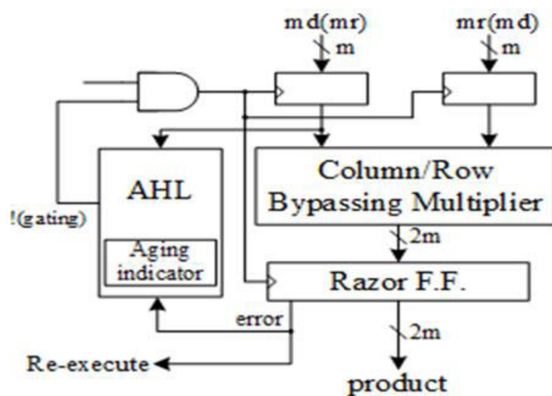

Fig 1: PROPOSED ARCHITECTURE

The column-or row-bypassing multiplier is not able to complete these operations successfully, if the cycle period is too short causing timing violations. These timing violations will generate error signals which be caught by the Razor flip-flops. If errors happen frequently and exceed a predefined threshold, it means the circuit has suffered significant timing degradation due to the aging effect, and the aging indicator will output signal 1; otherwise, it will output 0 to indicate the aging effect is still not significant, and no actions are needed.

Hence, by using similar architecture, the difference between the two bypassing multipliers lies in the input signals of the AHL and the two aging-aware multipliers can be implemented. According to the bypassing selection in the column or row-bypassing multiplier, in the architecture with the column-bypassing multiplier the input signal of the AHL is the multiplicand, whereas that of the row-bypassing multiplier is the multiplicator. By using Razor flip-flops timing violations occur before the next input pattern arrives can be detected.

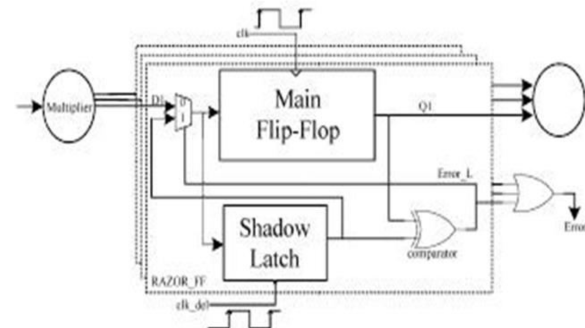

Fig. 2: RAZOR FLIP-FLOPS

A 1-bit Razor flip-flop contain main flip-flop, shadow latch, XOR gate and multiplexer. The shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal and the main flip-flop catches the execution result for the combination circuit using a normal clock signal. The path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result if the latched bit of the shadow latch is different from that of the main flip-flop. To notify the system the Razor flip-flop will set the error signal to 1 to re execute the operation if any errors occur and notify the AHL circuit that an error has occurred. To detect whether an operation that is considered to be a one-cycle pattern can really finish in a cycle we use Razor flip-flops. If not, the operation is re-executed with two cycles. Although the re-execution may seem costly, because the re-execution frequency is low and the overall cost is low.

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In the aging-ware variable-latency multiplier the AHL circuit is the key component. The AHL circuit contains an aging indicator, two judging blocks, one mux, and one D flip-flop. Due to the aging effect the aging indicator indicates whether the circuit has suffered significant performance degradation. Over a certain amount of operations the aging indicator is implemented in a simple counter that counts the number of errors and is reset to zero at the end of those operations.

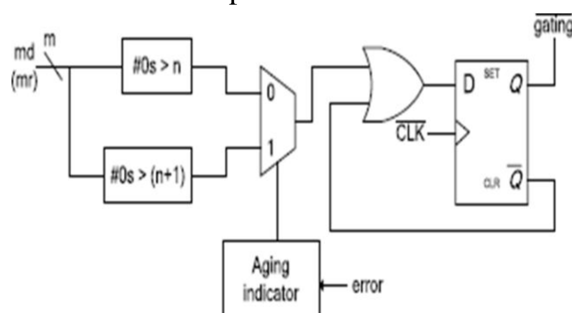

Fig. 3: DIAGRAM OF AHL

The operation details of the AHL circuit are as follows: whether the pattern requires one cycle or two cycles to complete when an input pattern arrives and pass both results to the multiplexer will decided by both judging blocks. In the AHL circuit first judging block will output 1 If the number of zeros in the multiplicand is larger than n. The second judging block in the AHL circuit will output 1 if the number of zeros in the multiplicand (multiplicator) is larger than n + 1. Whether an input pattern requires one or two cycles, they are both employed to decide but only one of them will be chosen at a time. The aging effect is not significant, and the aging indicator produces 0, in the beginning, so the first judging block is used. When the aging effect becomes significant, after a period of time the second judging block is chosen. The second judging block allows a smaller number of patterns to become one-cycle patterns when compared with the first judging block, because it requires more zeros in the multiplicand (multiplicator).

Based on the output of the aging indicator, multiplexer selects one of either result. Then between the result of the multiplexer, an OR operation is performed and the Q signal is used to determine the input of the D flip-flop. The output of the multiplexer is 1 when the pattern requires one cycle, the signal will become 1, and in the next cycle the input flip flops will latch new data. On the other hand, when the output of the multiplexer is 0, which means the input pattern requires two cycles to complete, the OR gate will output 0 to the D flip-flop. Therefore, the signal will be 0 to disable the clock signal of the input flip-flops in the next cycle. Note that only a cycle of the input flip-flop will be disabled because the D flip-flop will latch 1 in the next cycle.

IV. RESULTS

Synthesis Report of the High speed bypass Multiplier

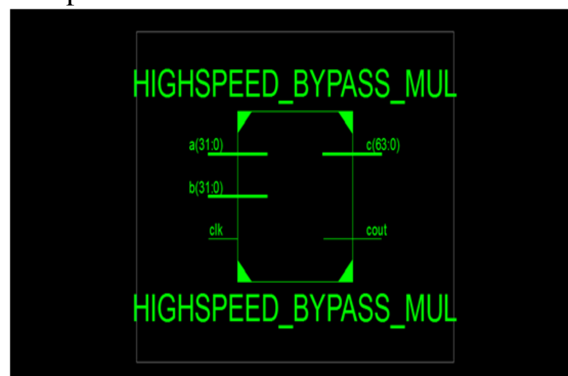

Fig. 4: RTL SCHEMATIC

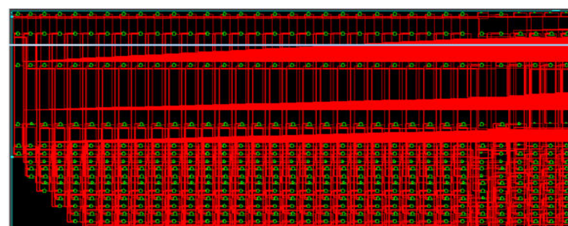

Fig. 5: TECHNOLOGY SCHEMATIC

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Simulation Report of the High speed bypasses Multiplier

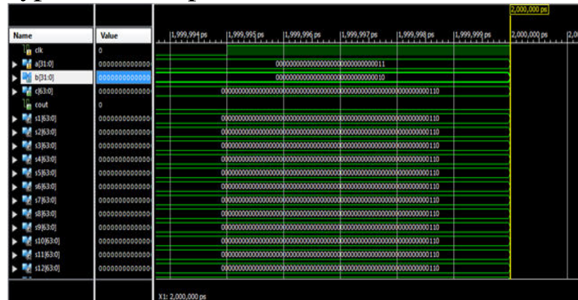

Fig. 6: OUTPUT SIMULATION

V. CONCLUSION

This paper proposed an aging-aware variable latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The proposed variable latency multipliers have less performance degradation due to the variable latency multipliers which have less timing waste, but traditional multipliers need to consider the degradation which is caused by both the BTI effect and electro-migration and utilize the worst case delay as the cycle period. In this project we increase the speed of the multiplier for 32-bit input. In future we can design for 64-bit and 128-bit also and we can also design the DSP applications by using this multiplier.

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