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FPGA Implementation Of Reconfigurable Address Generator Of Deinterleaver For WiMAX Applications

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ABSTRACT:

In this project, a low-intricacy and innovative technique is proposed to efficiently implement the address generation circuitry of the 2-D deinterleaver used in the WiMAX transreceiver using the Xilinx field-programmable gate array (FPGA). The floor function associated with the implementation of the steps, required for the permutation of the incoming bit stream in channel Interleaver/deinterleaver for IEEE 802.16e standard is very difficult to implement in FPGA. A simple algorithm along with its mathematical background developed in this brief, eliminates the requirement of floor function and thereby allows low-complexity FPGA implementation. The use of an internal multiplier of FPGA and the sharing of resources for quadrature phase-shift keying, 16-quadrature-amplitude modulation (QAM), and 64-QAM modulations along with all possible code rates makes our approach to be novel and highly efficient when compared with conventional look-up table-based approach. The proposed approach exhibits significant improvement in the use of FPGA resources. Exhaustive simulation has been carried out to claim supremacy of our proposed work. The IEEE 802.16 standard, commonly known as WiMAX, is the latest technology that has promised to offer broadband wireless access over long distance. Since 2001 WiMAX has evolved from 802.16 to 802.16d for fixed wireless access, and to the new IEEE 802.16e standard with mobility support.

Keywords: Digital circuits, error correction, field programmable gate arrays (FPGAs), wireless systems.

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I INTRODUCTION

REMENDOUS increase in use of internet in the last decade has put the quest of Broadband Wireless Access (BWA). BWA has emerged as the last mile access solution and a challenging competitor to existing 3G technologies [1]. It is increasingly gaining popularity as an alternative solution to Digital Subscriber Line (DSL) or cable modem for internet access. BWA has stringent requirements like high processing speed, flexibility and fast design Turn Around Time (TAT). These requirements make the designers to choose reconfigurable hardware platform like Field Programmable Gate Array (FPGA). Moreover, any new technology like Worldwide Interoperability for Microwave Access (WiMAX) needs some time to mature. Thus a product implemented on FPGA can easily be upgraded by making necessary changes in the Hardware Description Language (HDL) code and thus becomes obsolescence free. In addition, the TAT of FPGA based circuit is much shorter compared to Application Specific Integrated Circuit (ASIC). Design flexibility is another important advantage of FPGA based implementations. The proposed system could have also been implemented using software. The principal drawback of such approach is that a powerful computer is to be used to run the program for achieving high processing speed, a prerequisite for WiMAX system. Employment of such powerful computer may be a costly solution but may be detrimental to the popularity of WiMAX.

WiMAX is based on the IEEE 802.16 standard for BWA system. IEEE 802.16d, now known as, IEEE 802.16-2004 defines fixed BWA (FBWA) in the frequency band of 2 to 11GHz [2]. Amended IEEE 802.16e adds mobility support to IEEE 802.16 and defines standard for mobile BWA (MBWA) in the frequency band 2 to 6GHz.Typical data rate in IEEE 802.16e is 5 Mbps with bandwidth 1.25 to 20 MHz. Both IEEE 802.16-2004 and IEEE 802.16e permit Non Line of Sight (NLOS) connectivity [3].

Orthogonal Frequency Division Multiplexing (OFDM) [3] technique offers promising solution that has gained tremendous research interest in recent years due to its high transmission capability and also for alleviating the adverse effects of Inter Symbol Interference (ISI) and Inter Channel Interference (ICI). In an OFDM system, the data is divided into multiple parallel substreams at a reduced rate, and each is modulated and transmitted on a separate orthogonal subcarrier. This increases symbol duration and improves system robustness [4]. OFDM is achieved by providing multiplexing on users' data streams on both uplink and downlink transmissions. OFDM is the fundamental building block of the IEEE 802.16 standard. Interleaving plays a vital role in improving the performance of Forward Error Correction (FEC) codes in terms of Bit Error Rate (BER). Interleaving is the process to

rearrange code symbols so as to spread burst of errors into random like errors and thereafter FEC techniques could be applied to correct them. In conventional block interleaver [5], the bits received from the encoder are stored row wise in the interleaver's memory and read column wise. WiMAX uses a special type of block interleaver in which the Interleaver Depth (ID) and pattern vary depending on the code rate and modulation type.

II.LITERATURE SURVEY

Due to the continuously decreasing feature sizes and the increasing clock frequencies on integrated digital circuits, power dissipation is growing to be one of the major concerns during the design of an integrated circuit. Examples of this phenomenon are for instance the DEC Alpha chip (dissipating 30 Watts at 3.3V , 200 MHz) and the SUNViking (dissipating 8 Watts at 5V, 50 MHz). Currently many circuits are designed by describing them in a behavioral description language like VHDL or Verilog. By using a synthesizer, this description is synthesized into a gate level netlist. This way of designing saves a lot of design time compared to traditional design methodologies like schematics entry. Most synthesizers are currently targeted towards fully synchronous designs, suitable for scan chain insertion, to be able to test the circuit by scan testing. One of the main contributors to power dissipation is the clock tree. The clock net is one of the nets with the highest switching density. The clock net is also a net with a large fanout (all flip–flops are connected to the clock net) , resulting in high power dissipation.

This clocking produces power dissipation on two points:

- Dissipation in the clock drivers and the clock lines.
- Dissipation in the flip–flops (most flip–flops contain an inverter connected to the clock signal.)

In micro processor like designs there is a large number of registers that are there to hold their data most of the clock cycles. Analysis of the circuits generated by logic synthesizers dissolves that this functionality is implemented by providing a conditional loop back from the output of the flip–flop to its input. If such a loop back is active, the flip– flop needs not to be clocked, because the value of the flip–flop will not change; the flip–flop is in the so called ”hold mode”, however due to the implementation with a loop back unnecessary power is consumed. A promising technique to reduce the power dissipation of the clock net is selectively stopping the clock in parts of the circuit, called ”clock gating”. This technique is not new at all and already applied in a number of ways. In (Schutz 1994) and (Suessmith et al. 1994) this technique is applied during the design of microprocessors, however the places where the gated–clocks are inserted are determined by the designer. In (Beniniet al. 1995) an automatic method to insert gated–clocks

in finite state machines is presented. Although every sequential circuit can be modeled as a finite state machine, this technique only works if the symbolic transition table of the implemented finite state machine is known. For large circuits this is an impractical approach. In (Benini et al. 1997) the problem of generation the state transition table is circumvented, but still the idea of modelling the circuit as a single finite state machine is used. So only clock gating can be applied if the whole FSM (or design) performs a so called ”self loop”. In practice however only some parts of a design can be switch off by clock gating. The tool presented in (Benini et al. 1997) will not be able to find these situations. In (Papachristou et al. 1995) a power saving technique is shown that during architectural synthesis determines which flip–flop can be switched off during the operation of the circuit. In this paper we present a method to generate gated–clock circuits starting from a netlist resulting from for instance a logic synthesizer. The idea of the developed method is to identify the flip–flops in the design that keep their data for a large portion of the clock cycles. For these flip–flops the condition will be determined for which they keep their data and the circuit will be transformed in such a way that the clock signal will be switched off if the condition is satisfied.

III. PROBLEM OUTLINE

EXISTING SYSTEM

The present systems has not much has been done regarding the hardware efficiency and resource utilization. Out of all the 2D realization of WiMAX channel interleaver for efficient hardware implementation and Novel design of address generator for WiMAX multimode interleaver using FPGA based finite state machine, 2D realization of WiMAX channel interleaver for efficient hardware implementation has mathematical limitations. Whereas Novel design of address generator for WiMAX multimode interleaver using FPGA based finite state machine incorporate random code rates with hardware efficient. In upcoming section we have results and discussion with final conclusion on this project.

PROPOSED SYSTEM

In this project, a novel, low-complexity, high-speed, and resource-efficient address generator for the channel deinterleaver used in the WiMAX transreceiver eliminating the requirement of floor function is proposed. As compared with the complicated and lengthy expressions, particularly for 16-QAM and 64-QAM, due to the 2-D translation, a compact and user-friendly mathematical representation and subsequent algorithm is proposed.

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IV. METHODOLOGY

In order to meet the requirements of 4G mobile networks targeted by the cellular layer of IMT-advanced, next generation mobile WiMAX devices based on IEEE 802.16m will incorporate sophisticated signal processing, seamless handover functionalities between heterogeneous technologies and advanced mobility mechanisms. This survey provides a description of key projected features of the physical (PHY) and medium access control (MAC) layers of 802.16m, as a major candidate for providing aggregate rates at the range of Gbps to high-speed mobile users. Moreover, a new unified method for simulation modeling, namely the evaluation methodology (EVM), introduced in 802.16m, is also presented.

Interleaving is a technique commonly used in communication systems to overcome correlated channel noise such as burst error or fading. The interleaver rearranges input data such that consecutive data are spaced apart. At the receiver end, the interleaved data is arranged back into the original sequence by the **de-interleaver**. As a result of interleaving, correlated noise introduced in the transmission channel appears to be statistically independent at the receiver and thus allows better error correction.

Interleaving may refer to:

- interleaving, a technique for making forward error correction more robust with respect to burst errors;
- an optical interleaver, a fiber-optic device to combine two sets of dense wavelength-division multiplexing (DWDM) signals;
- interleaved memory, a technique for improving the speed of access to memory;
- interleaving (disk storage), a technique for improving the speed of access to blocks on disk storage;
- interleaved posting, an e-mail posting style;
- interleaving (bitmaps), a technique for encoding bitmapped images;
- Interleaving the bits of the binary representation of coordinate values to produce a Z-order (curve) for points.
- Interleave sequence, a mathematical sequence formed by interleaving members of two other sequences in alternation.

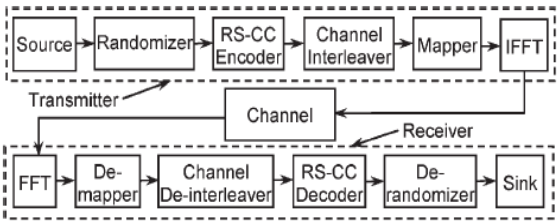

Fig. 1. Block diagram of the WiMAX transreceiver.

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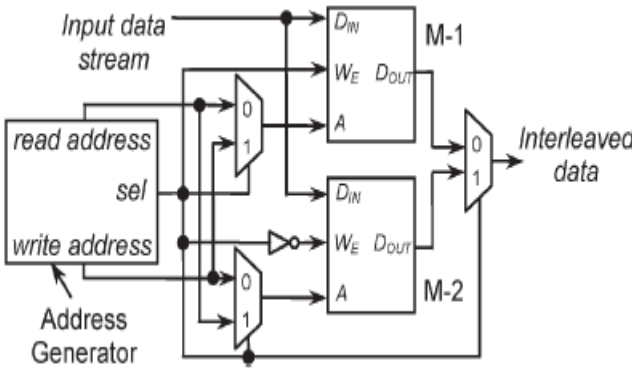

Fig 2: Block diagram of interleaver/deinterleaver structure

Steps in the WIMAX transceiver:

1. Data stream received from a source is randomized.
2. Data encoded by two forward error correction (FEC) coding techniques, namely, Reed–Solomon (RS) and convolution coding (CC).
3. The channel interleaver permutes the encoded bit stream to reduce the effect of burst error.
4. Modulation and construction of orthogonal frequency-division multiplexing symbols are performed by the two subsequent blocks, namely, mapper and inverse fast Fourier transform.
5. In the receiver, the blocks are organized in the reverse order enabling the restoration of the original data sequence at the output.

V.RESULTS

SCEMATIC DESIGNS:

RTL SCHEMATIC:

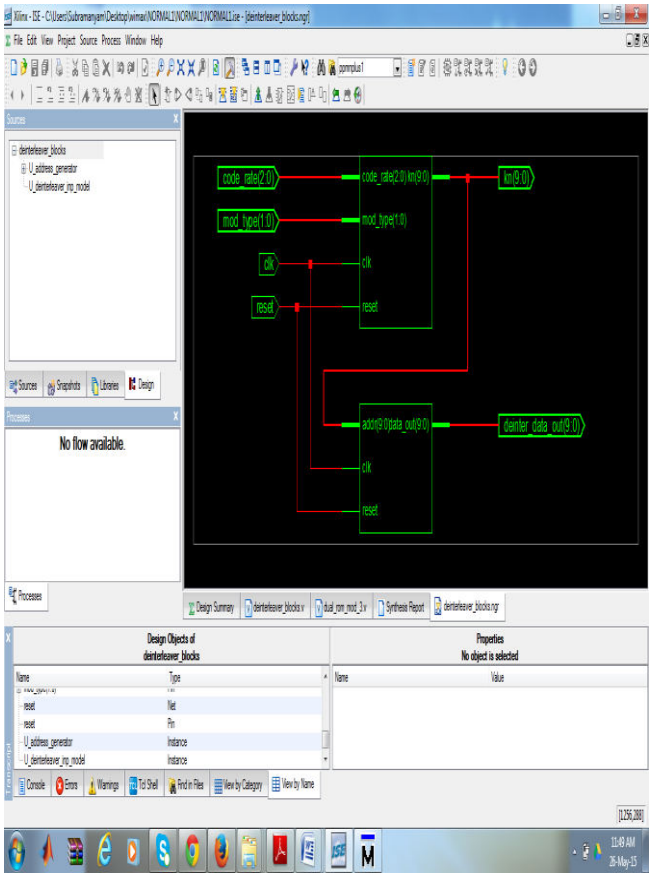

Fig 3: RTL Schematic

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TECHNOLOGY SCHEMATIC:

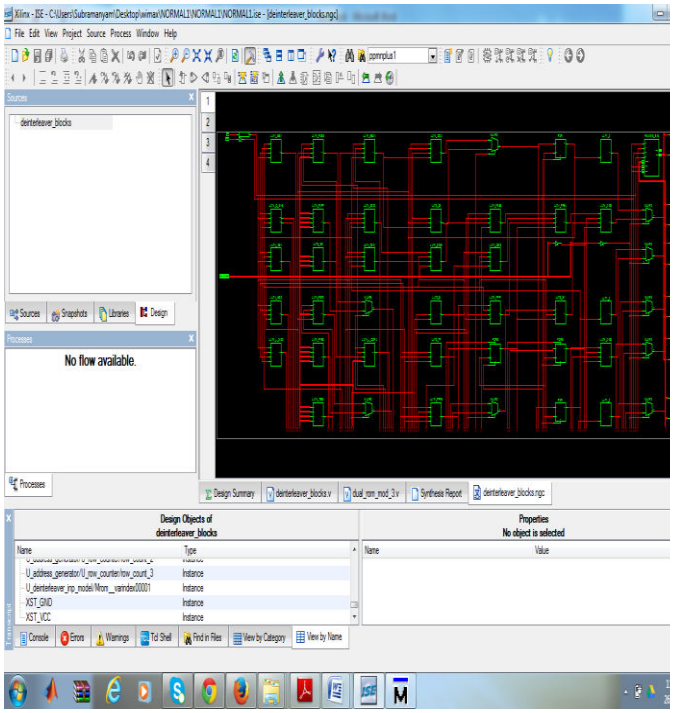

Fig 4: Technology Schematic

DESIGN SUMMARY:

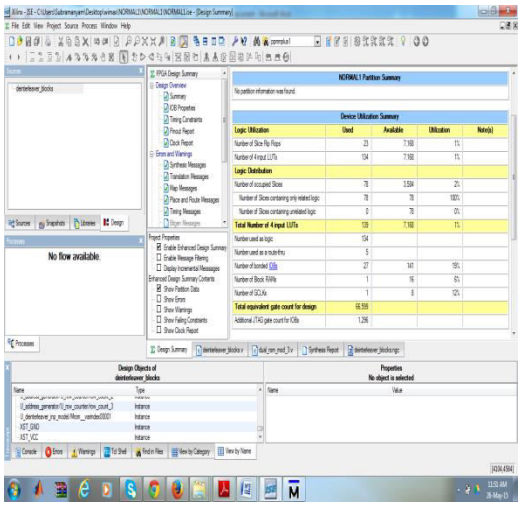

Fig 5: Design Summary

VI.CONCLUSION

This project has proposed a novel algorithm along with its mathematical formulation, including proof for address generation circuitry of the WiMAX channel deinterleaver and interleaver supporting all possible code rates and modulation patterns as per IEEE 802.16e. The proposed algorithm is converted into an optimized digital hardware circuit. The hardware is implemented on the Xilinx ISE 12.3 using Verilog. Comparison of our proposed work with a conventional LUT-based method and also with a recent work show significant improvement on resource utilization and operating frequency.

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