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DATA ENCODING AND DECODING TECHNIQUES FOR REDUCING ENERGY CONSUMPTION

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ABSTRACT:

The technology increases in the present world even though; some of the power dissipation problems are diminishing the technology in the field of NoC. This power dissipation was mainly seen in the other elements of the communication subsystem, which are routers and network interfaces. In this project, we are developing the data encoding and decoding schemes to reduce the power dissipated by the links of a NoC. The proposed design was implemented using verilog HDL. Which allow saving us for saving power dissipation and energy consumption without any affect on performance degradation.

In this project, we are proposing three different schemes to reduce the power in the links of the NoC. Here in this project we are reducing the coupling switching activity and the normal switching activity to reduce the total power dissipation in the links of the NoC by using different encoding schemes. By these proposed techniques, the consecutive bits are taken care not to have opposite values so that coupling switching activity is reduced. Similarly, the bits passed through the particular links are encoded in such a way that toggling (opposite previous and present values) of the bit values in that particular links is prevented. In this way normal switching activity is reduced.

Keywords: Coupling switching activity, data encoding, interconnection on chip, low power, network-on-chip (NoC), power analysis.

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I INTRODUCTION

Every technology has facing some problems like power dissipation, energy problems etc. In VLSI technology the wire densities increases to support every small transistor geometries and then it leads to energy and power problems. By increasing the delay between on chip unit will get high latency of cross-chip communication system can still limit the total performance. By using on-chip packet-switched of interconnects are generally known as Network-on-Chip (NoC) architecture, we satisfied scalable bandwidth requirement. The traditional large-scale multi-processors and distributed computing network leads to get the basic idea to the NoC-based system implementation.

In order to meet typical SoC of network interconnection like switching logic and the packet definition should be light-weighted to get easy implementation solutions. Another way to exceed such limitation of communication and overcome wiring delay in future.

As mentioned the basic concept of such kind of interconnections is from the modered compute ring network evolution. By applying network-like communication system which inserts some routers in-between each communicating object, the required wiring can be shorten. Therefore, switch-based interconnecting mechanism provides a lot of scalable and freedom from the limited of complex wire. Replacement of SoC bussing by NoCs will follow the same path of data communicating when the economics proving that the NoC either reduces SoC manufactured cost, SoC time to marketed, SoC time to volumeing, and SoC designing risk or increases SoC, performances. According to the NoC approaches has a clear advantaging over traditional buss sing and most notable system throughput. And hierarchies of crossbars or multi-layering busses have characteristic somewhere in between traditional busses and NoCs, however they still fall far short of the NoC with respect to performance and complex. The success of the NoC designing on the research of the interfaces between processed elements of NoC and interconnection fabric.

The interconnecting of a SoC established procedures has some points in those respected of slow bus response time, scalability problem, and energy, bandwidth limitations. Bus interconnection composed of a large number of components in a network interfacing can cause slow interface time though the influence of sharing the bus.

In addition the interconnected has a defect, which is power consumption is high on the scouring of connecting all objects in the communication system. Moreover it is impossible to increasing the number of connection of the elements infinitely by reason of the limitation of bandwidth in a bus. In fact, the communicating subsystem increasingly impacts the traditional design objectives, including cost, performances, power dissipation, energy consumption etc.

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In this project, a low-power data encoding scheme is proposed system. In general, system-on-chip (soc) based systems has so many disadvantages in powered-dissipation as well as clock rate wise, the such transfer the data from one system to another system in on-chip. A higher operating system does not support the lower operated in the bus network for data transfer information. However an alternative system scheme is proposed for high speed data transfer in system. But this scheme is limited to SOCs. Unlike SoC, network on- chip (NOC) system has so many advantages for data transfer techniques. It has a special feature to transfer the data in on-chip network named as transitional encoder. Its operation is based on transitions of input data. At the same time it which are operated at higher frequencies performance. The proposed system yields lower dynamic powered dissipation due to the reduction of switched activity and coupling switched activity in the existing system when compared to existing system. Even-though many factors which are based on power dissipation, the dynamic power dissipation is only considerable for reasonable advantage

II.LITERATURE SURVEY

Most of the energy in traditional SoCs are dissipated in data buses and long interconnects due to dynamic power consumptions during charging and discharging of internal node capacitances as well as inter-wire capacitances. Crosstalk is dominated by inter-wire capacitance during charging as well as discharging.

The serial links in network on chip, NoC architectures can provide savings in the power dissipation, reduction of wire area, reduction of noise, simpler layout and timing verification, and controlled throughput by adjusting the frequency of the serialize. It also eliminates line drivers and buffers.

Disadvantages of serial communication, such as inter symbol interference between successive and high speed operation, can be appropriately handled by proper encoding and asynchronous protocols.

As a consequence, the performance of the network on chip NoC design relied greatly on the interconnection paradigms. Though the network technology in computer networking is already well developing, it is almost the impossible chip-level intercommunication environmental without any modification or reduction. For that reasoning, many researchers are trying to developing appropriate network architectures for on-chip communication. To be eligibly for NoC architecture, the basic functionality should and light-weighted because the implementing component of NoC architecture should be small enough in the form of the basic technique to be a basic component constructing a SoC. In order to be low powering one has to consider many parameters such as clock rate, operated voltages, power management.

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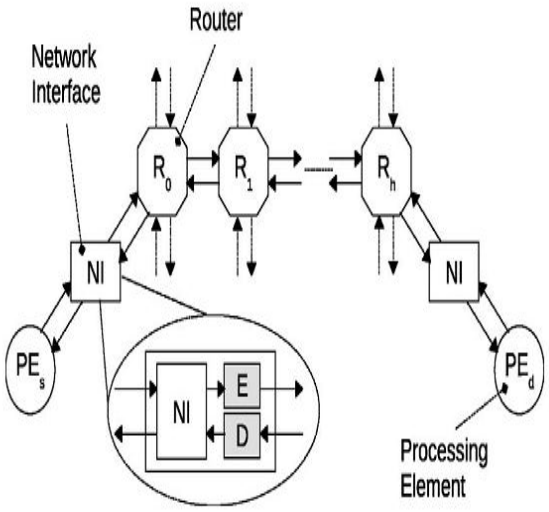

Fig 1: Fundamental concept of NOC

As shown in Fig the NI is augmented with an encoder (E) and a decoder (D) block. With the exception of the header flit, the encoder encodes the outgoing flits of the packet in such a way as to minimize the by the inter-router point-to-point links which form the routing path of the current packet. which have to be processes by the routers through the routing path. Similarly to the above description, all the incoming flits in the network interface (with the exception of the header flit) are decoded by the encoder block.

III. PROBLEM OUTLINE

EXISTING SYSTEM AND ITS DRAWBACKS

Mainly data encoding techniques are classified into two groups. In the first group, encoding techniques are concentrates on lowering the power due to self switched activity of individual bus lines while ignoring power dissipation due to their coupling switching activity.

In this group, bus invert (BI) and INC-XOR were proposed in the case of random data patterns are transmitted through these lines. On the other hand, T0, working-zone encoded and T0-XOR were suggested for the case of correlating data patterns. Here we were also proposed Application-specific proposals. This group of encoding is not suitable to be applied for deep sub micron meter technology nodes. Where the coupling capacitance comprises major part of the total interconnect capacitance of the link. Drawbacks of present existing system are:

- Increase the chip area
- Increasing line-to-line spacing
- More power consumption

PROPOSED SYSTEM

The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimized the self-switching activity and the coupling switching activity in the linked traversed by the flits. In fact, self-switching activity and coupling switching activity are responses for link power dissipation.

IV. METHODOLOGY

Proposed Encoding Architecture:

We consider a link width of *w* bits. If no encoding is used, the body flits are grouped in *w* bits

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by the NI and are transmitted via the link. In our approach, one bit of the link is used for the inversion bit, which indicates if the flit traversing the link has been inverted or not. More specifically, the NI packs the body flits in $w - 1$ bits. The encoding logic E, which is integrated into the NI, is responsible for deciding if the inversion should take place and performing the inversion if needed. To make the decision, the previously encoded flit is compared with the current flit being transmitted. This latter, whose w bits are the concatenation of $w - 1$ payload bits and a "0" bit, represents the first input of the encoder, while the previous encoded flit represents the second input of the encoder. The $w - 1$ bits of the incoming (previous encoded) body flit are indicated by Xi (Yi), $i = 0, 1, \ldots, w - 2$. The wth bit of the previously encoded body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). In the encoding logic, each Ty block takes the two adjacent bits of the input flits (e.g., $X1X2Y1Y2$, $X2X3Y2Y3$, $X3X4Y3Y4$, etc.) and sets its output to "1" if any of the transition types of Ty is detected. This means that the odd inverting for this pair of bits leads to the reduction of the link power dissipation (Table I). The Ty block may be implemented using a simple circuit. The second stage of the encoder, which is a majority voter block, determines if the condition is satisfied (a higher number of 1s in the input of the block compared to 0s). If this condition is satisfied, in the last stage, the inversion is performed on odd bits. The decoder circuit simply inverts the received flit when the inversion bit is high.

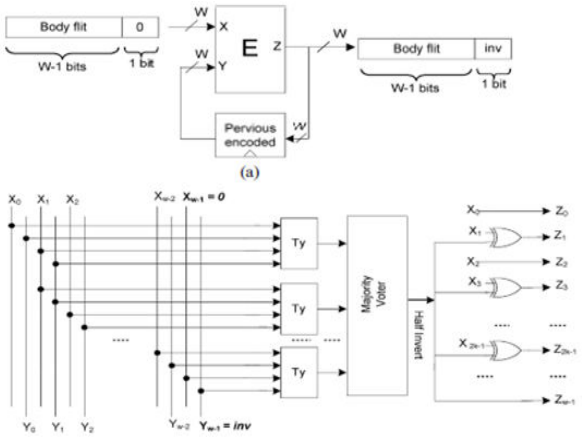

Fig.2: Encoder Architecture For Scheme 1

In scheme I, we focus on reducing the number of Type I transitions and Type II transitions. The scheme compares the current data with the previous one to decide whether odd inversions or no inversions of the current dating can lead to the link power reduction.

In Scheme II, both Types I and II transitions are taken into account for deciding between half and full invert, which is depending up on the amount of switching reduction.

SCHEME 2: ENCODER AND DECODER DESIGN

In the proposed encoding scheme II, we are making use of both odd and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. This scheme compares the current data

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with the previous one to decide whether the odd, full, or no inversion can give rise to the link power reductions.

Power Model:

Let us indicate with P, P', and $P''$the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, and full inversion, respectively. The odd inversion leads to power reduction when $P' < P''$ and $P' < P$. The power $P\_\_$ is given by

$$P'' \alpha\ T_1 + 2T_4^{***}$$

Neglecting the self-switching activity, we obtain the condition $P' < P''$ as

$$T_2 + T_3 + T_4 + 2T_1^{***} < T_1 + 2T_4^{**}$$

$$2(T_2 - T_4^{**}) < 2T_y - \omega + 1$$

The odd inversion condition is obtained as

$$2(T_2 - T_4^{**}) < 2T_y - \omega + 1 T_y > \left(\frac{\omega - 1}{2}\right)$$

$$T_2 > T_4^{**}$$

Therefore,, the full inversion condition is obtained as

$$2(T_2 - T_4^{**}) > 2T_y - \omega + 1 T_2 > T_4^{**}$$

Proposed Encoding Architecture:

The operating principles of this encoder are similar to those of the encoder implementing Scheme I. The proposed encoding architecture, which is based on the odd invert condition of (16) and the full invert condition of (18), is shown in Fig. 2. Here again, the *w*th bit of the previously and the full invert condition of (18) is shown in Fig. 2. Here again, the *w*th bit of the previously encoded body flit is indicated with inv which defines if it was odd or full inverted (inv = 1) or left as it was (inv = 0). In this encoder, in addition to the *Ty* block in the Scheme I encoder, we have the *T*2 and $T * *$ 4 blocks which determine if the inversion based on the transition types *T*2 and *T* 4 should be taken place for the link power reduction. The second stage is formed by a set of 1s blocks which count the number of 1s in their inputs. The output of these blocks has the width of log2 *w*. The output of the top 1s block determines the number of transitions that odd inverting of pair bits leads to the link power reduction. The middle 1s block identifies the number of transitions whose full inverting of pair bits leads to the link power reduction. Finally, the bottom 1s block specifies the number of transitions whose full inverting of pair bits leads to the increased link power. Based on the number of 1s for each transition type, Module A decides if an odd invert or full invert action should be performed for the power reduction.

In this encoder, in addition to the *Ty* block in the Scheme I encoder, we have the *T*2 and *T* **4 blocks which determine if the based on the transition types *T*2 and *T***4 should be taken place for the link

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power reduction. Then the second stage is formed by a set of 1s blocks which count the number of 1s in their inputs. The output of these blocks having the width of $\log_2 w$. The output of the top 1s block determines the number of transitions that odd inverting of pair bits leads to the link power reduction. The middle 1's block identifies the number of transitions whose full inverting of pair bits leads to the link power reduction.

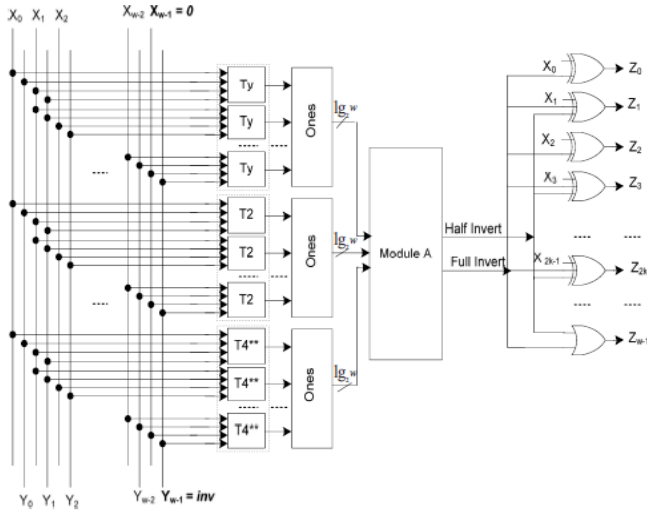

Fig.3: Encoder Architecture For Scheme 2

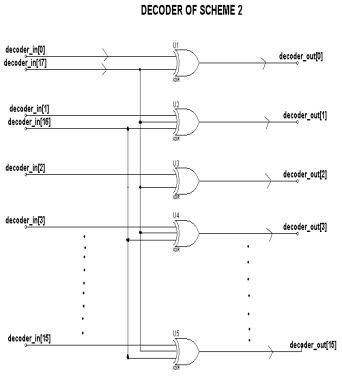

Fig.4: Decoder of Scheme II

V.RESULTS

SIMULATION RESULTS

The simulation is done to check the functionality of the design and to see if the design is working correctly or not by considering the modules written in verilog. The inputs are given and the outputs are checked in parallel if they are appropriate.

EXISTING RESULTS: SCHEME 2

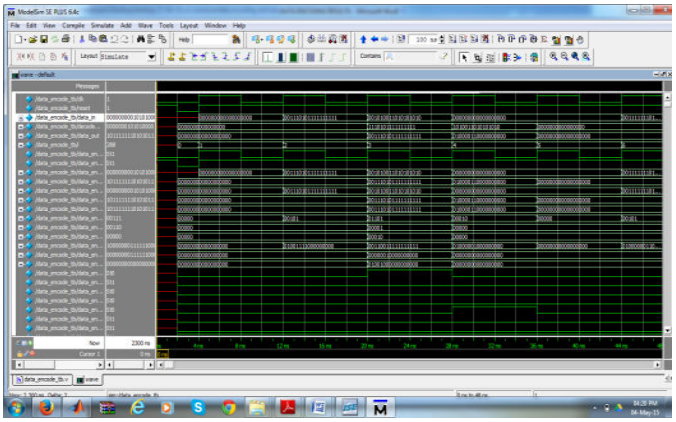

Fig.5: Scheme 2

PROPOSED RESULTS: SCHEME3

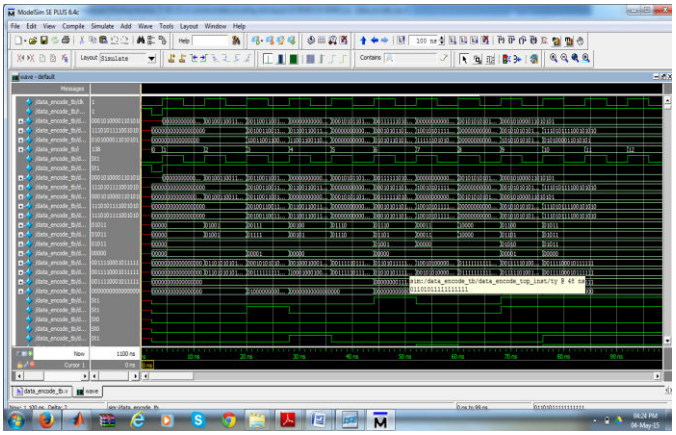

Fig.6: Scheme 3

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DESIGN SUMMARY

EXISTING METHOD

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	18	7,168	1%	
Number of 4 input LUTs	333	7,168	4%	
Number of occupied Slices	173	3,584	4%	
Number of Slices containing only related logic	173	173	100%	
Number of Slices containing unrelated logic	0	173	0%	
Total Number of 4 input LUTs	333	7,168	4%	
Number of bonded IOBs	37	141	26%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	3.88			

Table 1: Existing Method Design Summary

PROPOSED METHOD

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	18	7,168	1%	
Number of 4 input LUTs	467	7,168	6%	
Number of occupied Slices	249	3,584	6%	
Number of Slices containing only related logic	249	249	100%	
Number of Slices containing unrelated logic	0	249	0%	
Total Number of 4 input LUTs	467	7,168	6%	
Number of bonded IOBs	38	141	26%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	3.73			

Table 2: Proposed Method Design Summary

VI.CONCLUSION

We have implemented two schemes proposed in the paper (namely scheme-II and scheme-III) to reduce coupling switching activity and normal switching activity in links of Network-on-Chips. By these proposed techniques, the consecutive bits are taken care not to have opposite values so that coupling switching activity is reduced.

Similarly, the bits passed through particular links are encoded in such a way that toggling (opposite previous and present values) of the bit values in that particular links is prevented. It is the way to reduce the switching activity.

Note that in the Table-I of the IEEE paper, our aim is to covert Type-I and Type-II to Type-III and Type-IV bit combinations as far as possible. This is because, Type-III and Type-IV combinations result in less coupling switching and normal switching activities.

Out of the two schemes those are implemented, scheme-III have even lesser coupling switching and normal switching activity compared to scheme-II. This was achieved by the inclusion of "even inversion" module "te module" in the Scheme-III. By this, Type-I and Type-II bit combinations are converted in to Type-III and Type-IV bit combinations mentioned in Table 1. Whereas Scheme-II converts some Type-I bit combinations to Type-II bit combinations. So, as we discussed

earlier, Scheme-III is more optimized than Scheme-II.

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