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# IMPLEMENTATION OF QCA BINARY ADDERS USING VERILOG HDL

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**ABSTRACT:**

As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. The quantum-dot cellular automata (QCA) approach represents one of the possible solutions in overcoming this physical limit, even though the design of logic modules in QCA is not always straightforward. In this brief, we propose a new adder that outperforms all state-of-the-art competitors and achieves the best area-delay tradeoff. The above advantages are obtained by using an overall area similar to the cheaper designs known in literature. The 16-bit, 32-bit and 64-bit version of the novel adder is implemented by verilog language and simulated using xilinix ISE9.1.

Keywords: Adders, nanocomputing, quantum-dot cellularautomata (QCA).

## I INTRODUCTION

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to

modify an adder into an adder–subtractor. Other signed number representations require a more complex adder.Quantum-dot cellular automata (QCA) is an attractive emerging technology suitable for the development of ultradense low-power high-performance digital circuits [1]. For this reason, in the last few years, the design of efficient logic circuits in QCA has received a great deal of attention. Special efforts are directed to arithmetic circuits [2]–[7], with the main interest focused on the binary addition that is the basic operation of any digital system. Of course, the architectures commonly employed in traditional CMOS designs are considered a first reference for the new design environment. Ripple-carry (RCA), carry look-ahead (CLA), and conditional sum adders were presented. The carry-flow adder (CFA) shown in was mainly an improved RCA in which detrimental wires effects were mitigated. Parallel-prefix architectures, including Brent–Kung (BKA), Kogge–Stone, adner–Fischer, and Han–Carlson adders, were analyzed and implemented in QCA. Recently, more efficient designs were proposed for the CLA and the BKA, and in [for the CLA and the CFA. In this brief, an innovative technique is presented to implement high-speed low-area adders in QCA. Theoretical formulations demonstrated in for CLA and parallel-prefix adders are here exploited for the realization of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay of just one majority gate (MG). In addition, the clever top level architecture leads to very compact layouts, thus avoiding unnecessary clock phases due to long interconnections.An adder designed as proposed runs in the RCA fashion, but it exhibits a computational delay lower than all state-of the art competitors and achieves the lowest area-delay product (ADP).

## II.LITERATURE SURVEY

A QCA is a nanostructure having as its basic cell a square four quantum dots structure charged with two free electrons able to tunnel through the dots within the cell [1]. Because of Coulombic repulsion, the two electrons will always reside in opposite corners. The locations of the electrons in the cell (also named polarizations *P)* determine two possible stable states that can be associated to the binary states 1 and 0.Quantum - dot cellular automata (QCA) are an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. For this reason, in the last few years, the design of efficient logic circuits in QCA has received a great deal of attention. Special efforts are directed to arithmetic circuits,

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# III. PROBLEM OUTLINE

### EXISTING SYSTEM

The Existing adder design follows that of a conventional ripple carry adder, but with a new layout optimized to QCA technology. The proposed adder design shows that a very high delay can be obtained with an optimized layout. This is in contrast to the conventional ripple carry adder. To avoid confusion, the new layout is referred to as the Carry Flow Adder (CFA) here. In this Carry Flow Adder occupy more Number of gate Counts and More Delay.

### EXISTING SYSTEM TECHNIQUE:

- QCA Design Scheme

### EXISTING SYSTEM DRAWBACKS:

Compare to proposed system

- Low operation speed and more Delay
- Adders can be implemented in larger Area

**PROPOSED SYSTEM:**

An innovative technique is presented to implement high-speed low-area adders in QCA. The CLA and parallel-prefix adders are here exploited for the realization of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay of just one majority gate (MG). In addition, the clever top level architecture leads to very compact layouts, thus avoiding unnecessary clock phases due to long interconnections.

**PROPOSED SYSTEM TECHNIQUE:**

- QCA Design Based Majority gate

**PROPOSED SYSTEM ADVANTAGES:**

- Area Efficient
- Delay Efficient

# IV. METHODOLOGY

**Majority QCA:**

The fundamental logic gates inherently available within the QCA technology are the inverter and the MG. Given three inputs *a*, *b,* and *c*, the MG performs the logic function reported in equation (1) provided that all input cells are associated to the same clock signal clk*x*, whereas the remaining cells of the MG are associated to the clock signal clk*x*+1.

$$M(abc) = a \cdot b + a \cdot c + b \cdot c. \quad \text{---------- (1)}$$

In this project, a novel quantum-dot cellular automata (QCA) adder design is presented that decrease the number of QCA cells. The proposed one-bit QCA adder design is based on a new algorithm that requires only three majority gates and two inverters for the QCA addition. A novel 64-bit adder designed in QCA was implemented. It achieved speed performances higher than all the existing. QCA adders, with an area requirement comparable with the cheap RCA and CFA established. The novel adder operates in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. In adding together, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the explanation was limited. As transistors reduce in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot find much smaller than their current size. The quantum-dot cellular

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automata approach represents one of the possible solutions in overcome this physical limit, even though the design of logic modules in QCA is not forever straightforward.

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The prefix operation has three stages:

1. Pre calculation of pi,gi in each stage.

2. Calculation of carry ci for each stage.

3. Combine ci,pi to generate the sum bit and the carry bit “Si” and Cout

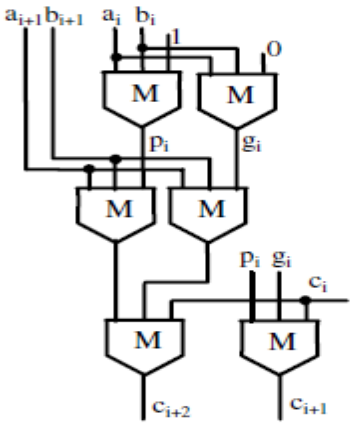


**Fig 1: novel 2-bit basic module**

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To introduce the novel design proposed for implementing ripple adders in QCA, let consider two *n*-bit addends *A* = an-1,……..a0, and *B* = bn-1,……..b0 and suppose that for the *i* th bit position (with $i = n - 1, \ldots, 0$) the auxiliary propagate and generate signals, namely pi=ai+bi and gi=ai.bi, are computed ci being the carry produced at the generic $(i-1)$th bit position, the carry signal $ci+2$, furnished at the $(i+1)$th bit location. an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA.

### *QCA Basics*

QCA is based on the interface of bi-stable QCA cells constructed from four quantum-dots. A high-level design of two polarized QCA cells is shown in Fig. 2. Each cell is constructed from four quantum dots arranged in a square pattern. The cell is charged with two electrons, which are free of charge to tunnel between adjacent dots. These electrons tend To take up antipodal sites as a result of their mutual electrostatic repulsion. Thus, there exist two equal energetically minimal arrangements of the two electrons in the QCA cell as shown in Fig. 2. These two arrangements are denoted as cell polarization P = +1 and P = -1 correspondingly. By using cell polarization P = +1 to represent logic "1" and P = -1 to represent logic "0", binary information can be encoded.

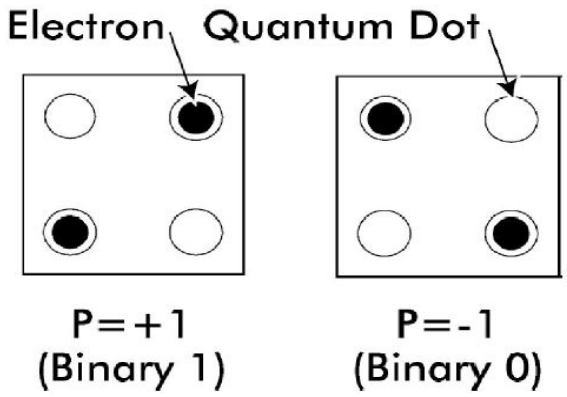


**Fig 2: QCA cells**

Arrays of QCA cells can be set to perform all logic functions. This is owed to the Columbic interactions, which influences the polarization of neighboring cells. QCA designs have been proposed with potential barriers between the dots that can be controlled and used to clock QCA designs.

### QCA Logical Devices:

The fundamental QCA logic devices are the QCA wire, majority gate and inverter. **QCA wire**: In a QCA wire, the binary signal propagates from input to output because of the Columbic connections between cells. This is a result of the system attempting to settle to a ground state. Any cells along the wire that are anti-polarized to the input would be at a high

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energy level, and would soon settle to the correct ground state. The propagation in a 90-degree QCA wire is shown in Figure. Other than the 90-degree QCA wire, a 45-dgree QCA wire can also be used. In this case, the propagation of the binary signal alternates between the two polarizations. Advance, there exists a so-called non-linear QCA wire, in which cells with 90-degree orientation can be placed next to one more, but off center.

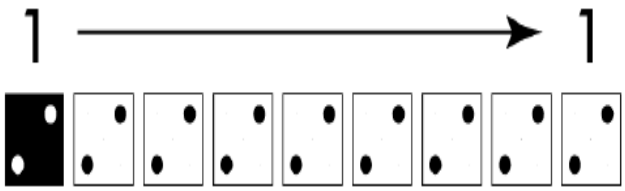


**Fig 3: AQCA wire (90-degrees)**

**Majority gate and inverter**: The majority gate and inverter are shown in below Figures respectively. The majority gate performs a three-input logic function. Assuming the inputs is A, B and C, the logic function of the majority gate is

$$m(A, B, C) = A|B + B|C + A|C$$

By fixing the polarization of one input as logic "1" or "0", we can get an OR gate and an AND gate respectively. More complex logic circuits can then be designed from OR and AND gates.

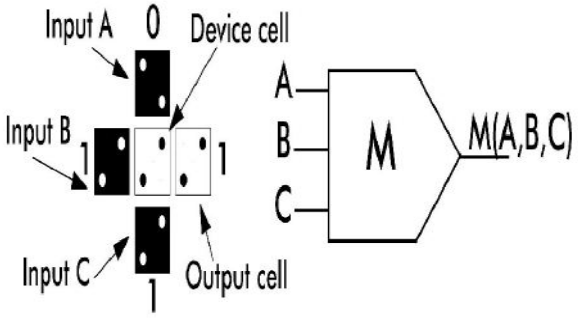


**Fig 4: A QCA majority gate**

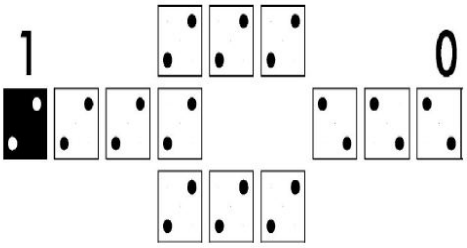


**Fig 5: A QCA inverter**

## V.RESULTS

### SIMULATION RESULTS:

### 16-BIT QSD ADDER:

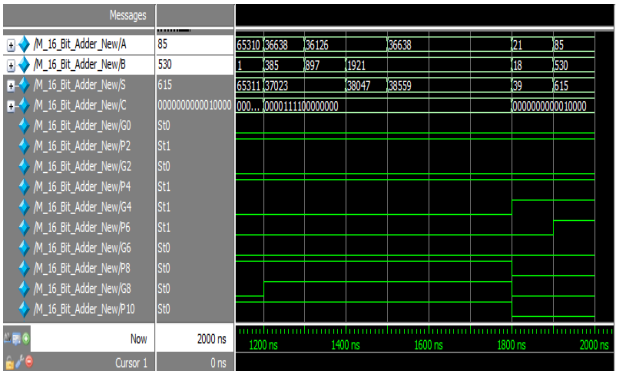


**Fig 6 : 16-Bit Qsd Adder**

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## 32-BIT QSD ADDER:

Fig 7 : 32-Bit QSD Adder

## 64-BIT QSD ADDER:

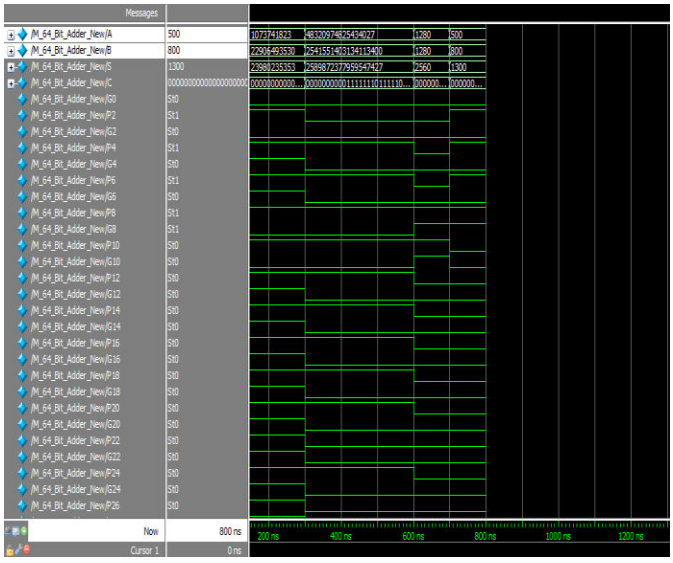

Fig 8 : 64-Bit Qsd Adder

## MODIFICATION PART:

## SYNTHESIS RESULTS:

## RTL SCHEMATIC:

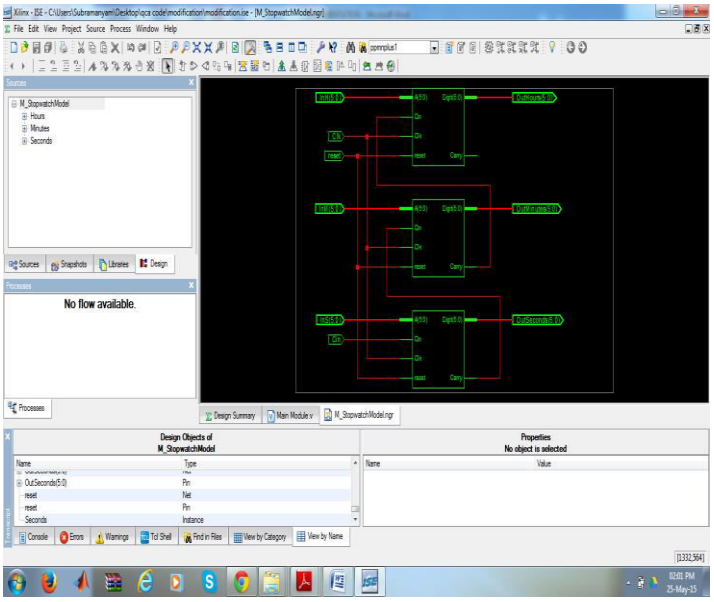

Fig 9: RTL SCHEMATIC

## TECHNOLOGY SCHEMATIC:

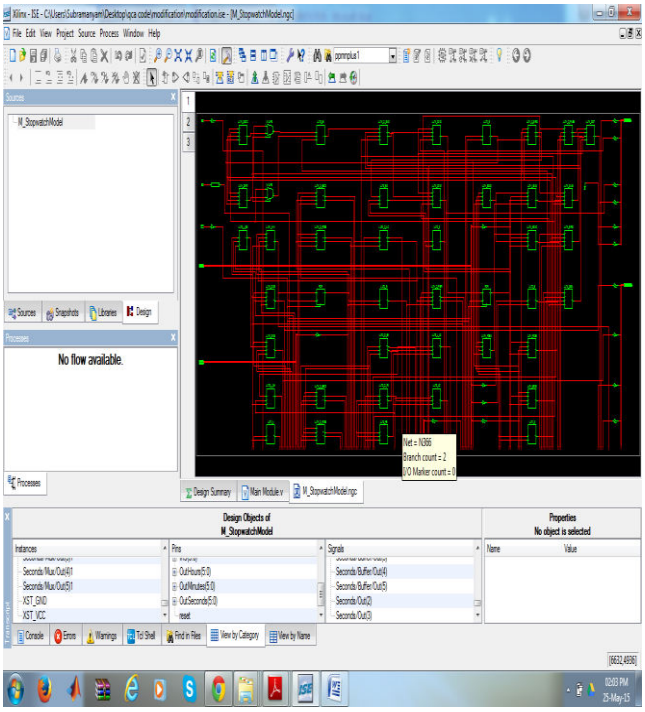

Fig 10: Technology Schematic

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## DESIGN SUMMARY:

| Device Utilization Summary | | | | |
|---|---|---|---|---|
| Logic Utilization | Used | Available | Utilization | Note(s) |
| Number of Slice Flip Flops | 16 | 7,168 | 1% | |
| Number of 4 input LUTs | 113 | 7,168 | 1% | |
| Logic Distribution | | | | |
| Number of occupied Slices | 61 | 3,584 | 1% | |
| Number of Slices containing only related logic | 61 | 61 | 100% | |
| Number of Slices containing unrelated logic | 0 | 61 | 0% | |
| Total Number of 4 input LUTs | 113 | 7,168 | 1% | |
| Number of bonded IOBs | 39 | 141 | 27% | |
| Number of GCLKs | 1 | 8 | 12% | |
| Total equivalent gate count for design | 830 | | | |
| Additional JTAG gate count for IOBs | 1,872 | | | |

| Performance Summary | | | |
|---|---|---|---|
| Final Timing Score: | 0 | Pinout Data: | Pinout Report |
| Routing Results: | All Signals Completely Routed | Clock Data: | Clock Report |

Fig 11: Design Summary

## SIMULATION RESULT:

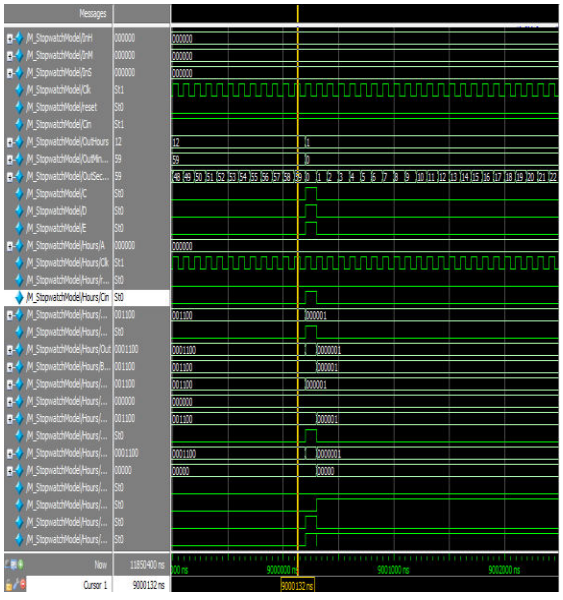

Fig 12: Simulation Result

# VI.CONCLUSION

In this project, we have considered primitives in QCA and have presented an efficient QCA design for an *n*-bit ripple carry adder. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. So, from the results we can observe that the QCA adder will occupy less area than the normal adders and also produce less delay when compared to the normal adder.

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## VIII AUTHORS

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