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Title IMPLEMENTATION OF A NEW SEVEN LEVEL DC-AC INVERTER

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IMPLEMENTATION OF A NEW SEVEN LEVEL DC-ACINVERTER

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Abstract: *This study proposes a novel multistage direct current-to-alternating current converter. The suggested multilevel inverter may produce seven various levels of alternating current (AC) output voltage with the proper gate signals. The low pass filter can reduce the overall harmonic content of the sinusoidal output signal. Switching losses and voltage stress for power components are avoided in the proposed multi-level inverter. The functioning principles of the recommended inverter and the voltage balancing strategy employing input capacitors are discussed. Finally, a prototype multilayer inverter with an input voltage of 400 V and an output voltage of 220 V rms / 2 kW is produced in the lab. This multilayer inverter is controlled by sinusoidal modulation of pulse widths (SPWM).*

Keywords*: DC-AC inverter, Sinusoidal Pulse-Width Modulation (SPWM), Maximum Power Point Tracking (MPPT)*

I. INTRODUCTION

Both the quantity and quality of electricity are increasing as a consequence of rapid technological progress. The development of semiconductors has spurred the promotion of power device specifications and power conversion technology. The term "inverter" is used to describe a specific kind of power converter that can change direct current to alternating current. Renewable energy sources, as seen in Fig. 1, are connected through an inverter to various additional electrical devices, such as a battery backup system, a servo motor, an air conditioning unit, and a smart grid. Varied loads have different requirements; hence the output frequency and voltage must vary accordingly. [1]-[3].

There has been a rise in the quantity of high-powered machinery in recent years. Consequently, power system harmonic pollution has worsened. IEEE Std. 1547, UL 1741, etc. are only a few examples of the many standards and regulations created to control the harmonics and power factor of electrical devices. [4]-[6]. In addition, the industry is demanding greater power applications, which has led to increased power device specifications. IGBT has the advantages of high-power rating and high voltage stress, but it is not suitable for high-frequency operation. The complexity lies in the IGBT gate driver design. At high frequencies, MOSFET is the best choice of component, although its power rating is inferior to that of IGBT. Many multilevel topologies use low-rated components in high-power applications to circumvent this issue.

A multilayer architecture is employed to reduce the necessary voltage for the power switch. As a result, it is frequently employed in high-power situations. By combining output voltages in multilayer form, the benefits of low dv/dt, low input current distortion, and reduced switching frequency are realised. Other topologies have emerged in recent years [7, 8] as a result of the advantages of multilevel topology. The authors construct and test a novel multilayer inverter in this work. The proposed topology is notable for its capacity to dramatically reduce power usage.

II.POWER STAGE

A. Circuit Configuration

Figure 2 depicts the redesigned architecture proposed for the seven-level inverter. Three series-connected capacitors, designated by C1, C2, and C3,

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create an input voltage divider. The fractioned voltage is carried to the H-bridge via four MOSFETs and four diodes. The H-bridge is composed of four MOSFETs and transmits voltage to the output terminal. The suggested multilevel inverter may produce seven various levels of alternating current (AC) output voltage with the proper gate signals.

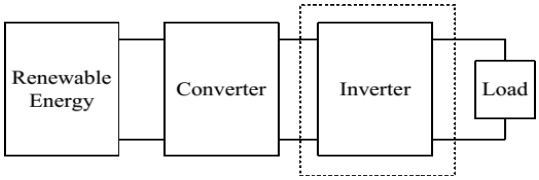

Fig 1. Block diagram of renewable system

B. Operating Principles

All seven terminal voltage levels (1/3V ac, 2/3V 12v, V dc, 0) are generated in the following manner:

1) When S 1 is triggered to generate a voltage level of V o = 1/3V dc, the positive half cycle begins. The power is supplied by capacitor C1, and the voltage across the H-bridge is 1/3V dc. A voltage of 1/3V dc is applied to the load terminals, and the switches S 5 and S 8 are turned on. Figure 3 depicts the current course of this mode.

2) When S 1 and S 4 are turned on, a voltage of V o = 2/3V dc is generated. The power is supplied by capacitors C1 and C2. The H-bridge uses a dc voltage of 2/3V. S 5 and S 8 are both

3 Switches S1 and S2 are turned on, resulting in a voltage of V o = V dc. The power is supplied by the capacitors C1, C2, and C3. V is the dc voltage across the H-bridge. Switches S5 and S8 are turned on, and V dc is delivered to the load terminals. Figure 5 depicts the current mode's course.

4) S 2 is triggered during the negative half cycle to generate a voltage level of V o = -1/3V dc. Capacitor C3 supplies the voltage across the H-bridge, which is 1/3V dc. Switches 6 and 7 are turned on, and the load terminals are supplied with -1/3V dc. Figure 6 depicts the present course in this manner.

5). S2 and S3 are turned on, resulting in a voltage of V o = -2/3V dc. The energy is supplied via capacitors C2 and C3. The H-bridge uses a dc voltage of 2/3V. The voltage at the load terminals is -2/3V dc when both S 6 and S 7 are active. Figure 1 depicts the current mode. 7.

6) We may obtain a voltage of V o = -V dc by engaging S 1 and S 2. The energy is supplied by capacitors C1, C2, and C3, and also the voltage out across H-bridge is V dc. When S6 and S7 are both turned on, a dc voltage of -V is applied to the input terminal. The current trajectory of this mode is depicted in Fig. 8.

To produce a zero voltage, S 5 and S 7 are triggered to create a voltage of V o= 0. The load terminals are not conducting any current. Figure 9 depicts the current trajectory in this mode. Table I shows the different output levels for each switching combination.

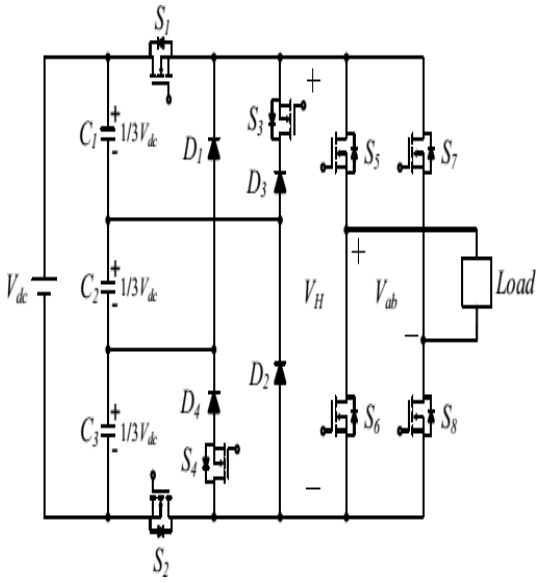

Fig. 2. 7-level inverter topology is proposed.

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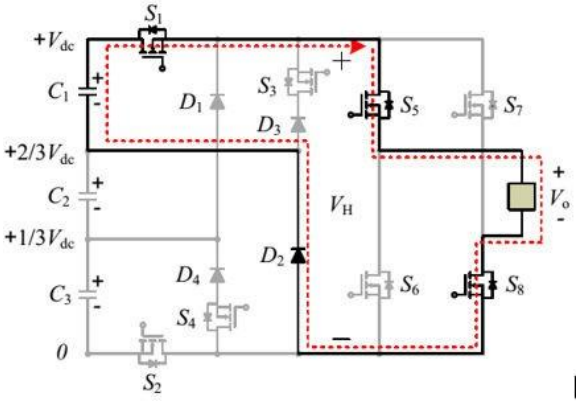

Fig. 3Alternating Current with Output Voltage of 3.3Vdc

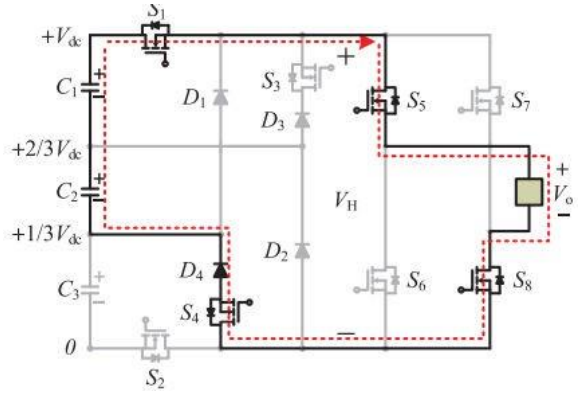

Fig. 4. Modulating between 2- and 3-volts dc at the output

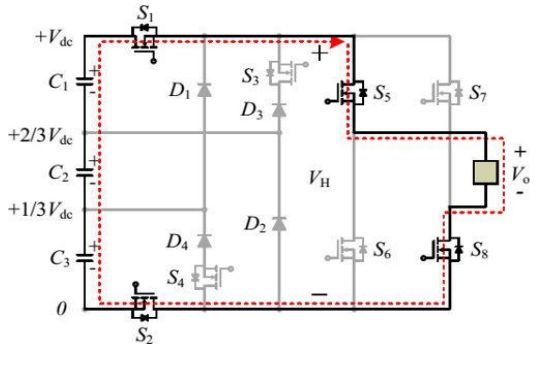

Fig. 5. Synchronizing Vdc-level output switching.

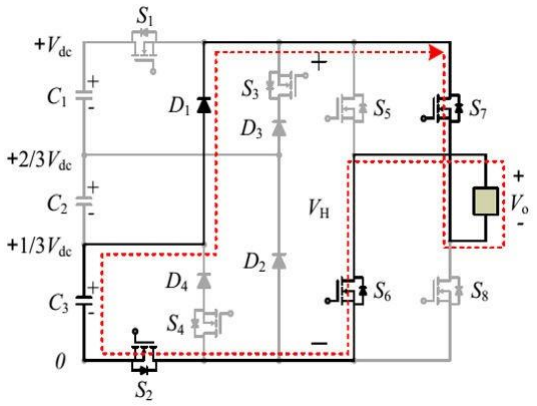

Fig. 6. The Output Voltage is Switched to Be -1/3Vdc

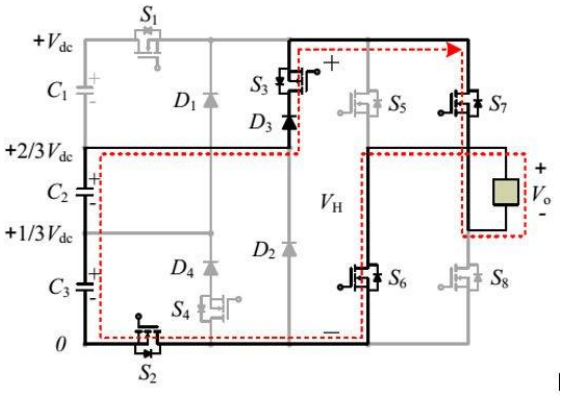

Fig. 7. Modulating the output voltage by a factor of -2/3Vdc.

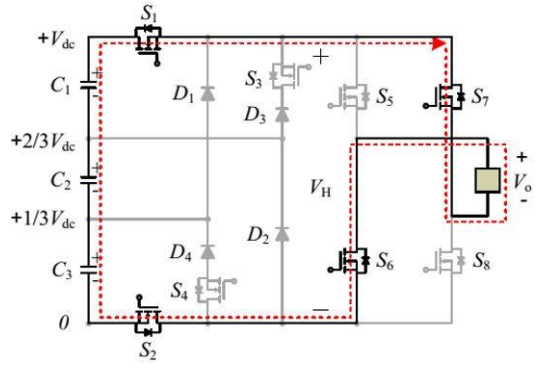

Fig. 8. Alternating Voltage DC Output Switching

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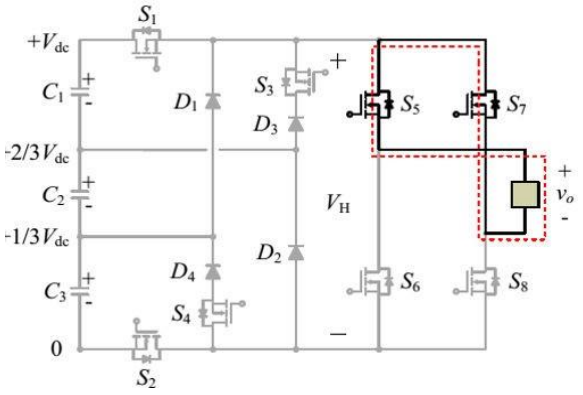

Fig. 9. Combinational switch for a voltage output of zero.

TABLE I

SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM REQUIRED SWITCHING COMBINATIONS

	Switching combinations							
Output voltage V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

C. Comparison of Topologies

Table II shows how many parts are required to construct a seven-level inverter with the recommended topology as well as three others [9, 10] that may be regarded of as standard multilevel architectures: the varistor inverter, the capacitor-clamped alternator, and the cascaded cross inverter. As demonstrated in Table II, the new architecture reduces the number of power devices. Table III examines several inverter types in terms of the voltage stress they impose.

TABLE II COMPONENT COMPARISON OF FOUR DISTINCT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-Clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

TABLE III

COMPARISON OF VOLTAGE STRESS BETWEEN Three DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-Clamped	Cascaded multicell
Input sources	V_o	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	V_o	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

III. VOLTAGE BALANCING CIRCUIT

ON THE BASIS OF RSCC Capacitors in multilayer inverters must be connected to voltage balancing circuits [11]-[15] because voltage variance increases harmonics distortion in the output voltage. The voltage imbalance of the input capacitors is corrected by utilizing a resonant switching capacitor converter. The RSCC unit's circuit setup is seen in Fig. 10. Each switch has a duty cycle of 50%. C1 has a greater voltage than C2, which is much lower. At any given switching cycle, more charges flow from C1 to C2 due to the former's greater average current. After a small number of transitions, the voltage on capacitors C1 and C2 will balance out. Its waveforms are shown in Fig. 11.

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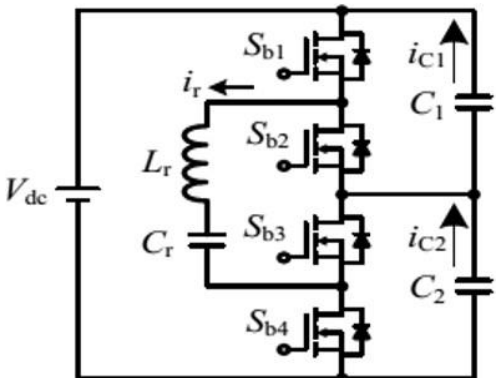

Fig. 10. The RSCC circuit configuration.

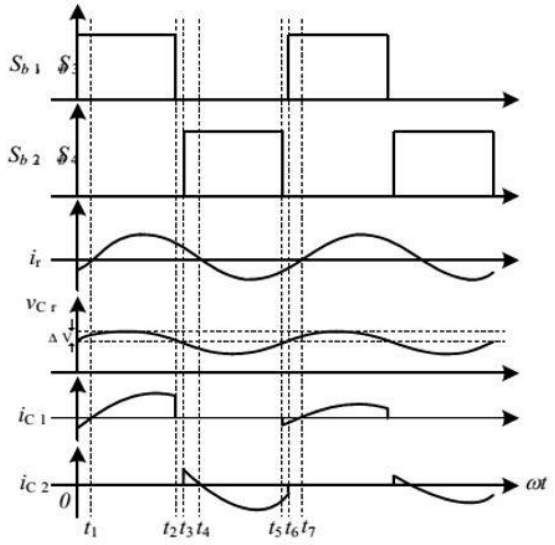

Fig. 11. The RSCC circuit configuration.

This is the recommended arrangement for the seven-stage inverter with RSCC. To implement RSCC in a seven-level configuration, two extra switches, S b5 and S b6, a resonant inductor L r, and a resonant capacitor Cr are required. Switches S b1, S b3, and S b5 are concurrently activated for this reason, as are switches S b2, S b4, and S b6. Each switch is responsible for 50% of the work.

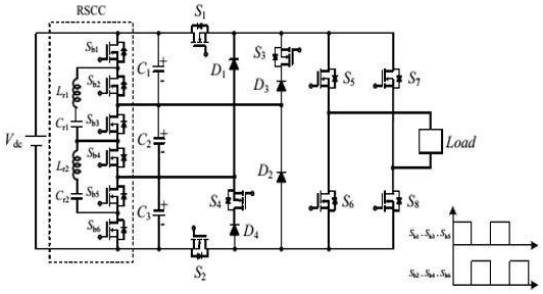

Fig. 12. The planned RSCC-equipped multilevel inverter.

IV.APPLICATION OF SPWM

The phase placement method is used in this study to allocate triangular carriers. With phase disposition, total harmonic distortion is minimised, and the technique is straightforward to execute [16], [17]. To establish the state of the switches, these carriers are compared to a conventional sine wave (v sin). The peak-to-peak range of a triangle carrier is. Carrier frequency is the same as inverter switching frequency. Where is the maximum value of the reference sine wave, and is the modulation index mA.

$$m_A = \frac{\hat{V}_{\sin}}{3 \cdot \hat{V}_{\text{tri}}} \qquad 1$$

The relationship between the highest value for the output sine wave and the current in amps (1) may be expressed as follows:

$$V_o = m_A \cdot V_{dc} \qquad 2$$

Figure 1 depicts the reference wave pattern, carrier, and switch control signals. 13.

Fig. 1 depicts methods for recognising switch signals. 12:

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(a) v sin < 0 and v sin > v tri2 → S 2 is turned on

(b) v sin > v tri4 → S 4 is turned on

(c) v sin < v tri8 → S 7 is turned on (d) v sin > v tri8 → S 8 is turned on

(e) v sin > 0 and v sin < v tri1 → S 1 is turned on

(f) v sin < v tri3 → S 3 is turned on

(g) v sin > v tri6 → S 5 is turned on

(h) v sin < v tri6 → S 6 is turned on

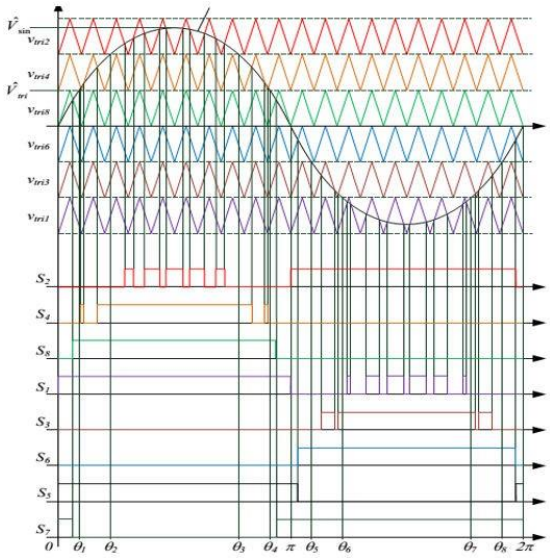

Fig. 13. Note the sine wave, carrier, and switch control signals as references.

V. PI CONTROL USED IN MODIFIED SPWM

We apply a PI-control-based variation of the SPWM in this study [18, 19]. Figure 14 depicts a PI control block diagram. The block diagram in S domain may be expressed as:

$$u(s) = \left[K_p + \frac{K_i}{s}\right] e(s). \quad 3$$

Z-domain forms of the equation may be derived from (11), as follows:

$$u(z) = \left[K_p + \frac{K_i}{1 - z^{-1}}\right] e(z) \quad 4$$

This means that we must use transformation to create a new difference in (12). The equation may be written as

$$u[n] = K_p e[n] + K_i e[n] - K_p e[n-1] + u[n-1] \quad 5$$

The block diagram of the system's setup and control is shown in Fig. 15. The system begins by detecting the voltage at its output, which it then compares to a fixed value. When a mistake occurs, the system reports it to the Controller. At last, the PI controller sends out a command signal to the gate driver.

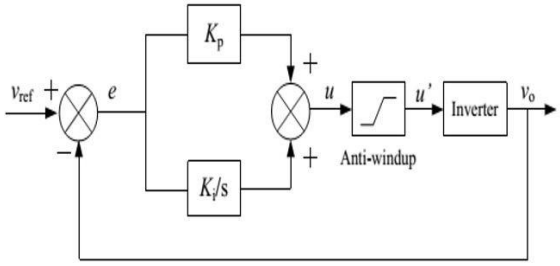

Fig. 14A PI control block schematic.

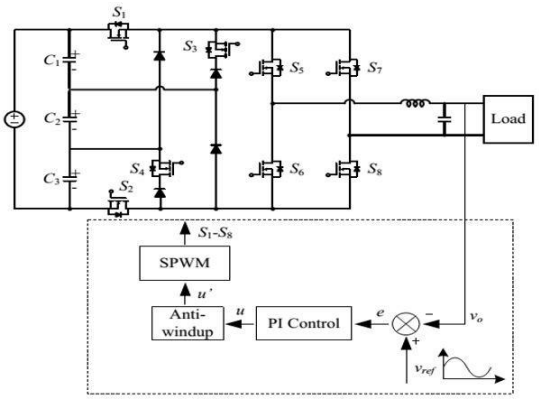

Fig. 15. An inverter with seven stages and an algorithm for controlling it.

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The basic concept behind modified SPWM is to keep track of the output voltage error that occurred in the previous cycle and then provide an appropriate correction in the most recent cycle. Switching occurs 300 times due to the difference between the carrier frequency of 18 kHz and the output sine wave frequency of 60 Hz. The updated SPWM layout is seen in Fig. 16.

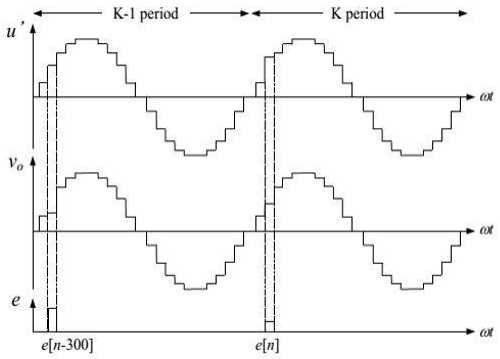

Fig. 16. Schematic of modified SPWM

$$e[n] = v_{\text{ref}}[n] - v_o[n]. \quad 6$$

The error between the reference output and the feedback output, denoted by e[n], is defined as (14), where v ref[n] is the reference output voltage, v o[n] is the feedback of output voltage.

$$u'[n] = K_1 \cdot e[n] - K_2 \cdot e[n-300] + u'[n-300] \quad 7$$

To do this, we set K1 = Kop + Ki and K2 = Kop, and then multiplied e[n] by K1 and e[n-300] by K2. After that, we include the output from before, u'[n-300]. After being processed by the anti-windup, the PI controller's output is then available.

VI.SIMULATION RESULTS

The seven-level inverter's Simulink model may be seen in Fig. 17. This prototype includes a sensor, a gate driver, a digital signal processor, a synchronous buck converter, and seven different levels of voltage.

Tabulated Information Regarding the Proposed Inverter

Input voltage V_{dc}	400 V
Output voltage V_o	220 V_{rms}
Rated output power P_o	2 kW
Switching frequency f_s	18 kHz

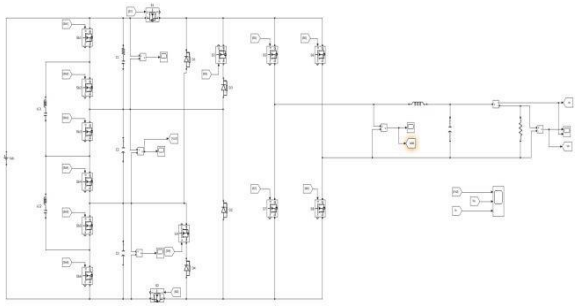

Fig. 17. MATLAB/SIMULINK circuit diagram of the proposed system

Figure 18 depicts the voltage output waveform (v ab), which comprises the desired seven voltage levels and waveform, as well as the output voltage and current. Figures 19 and 20 depict seven-level input voltage THD and output voltage THD.

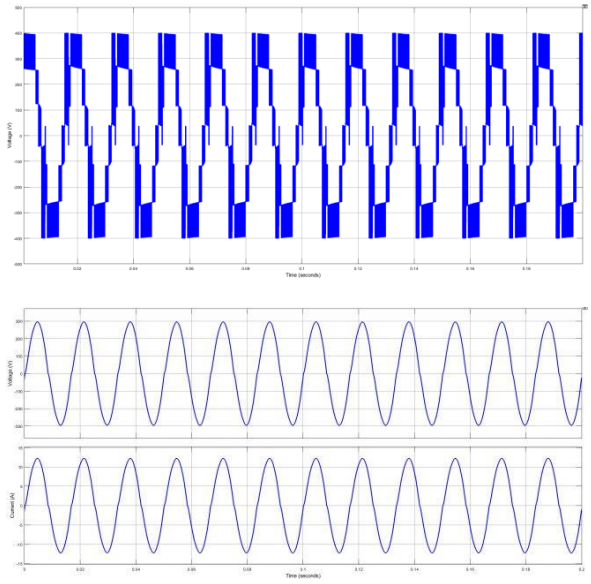

Fig. 18. The VA, Vo, and Iota Waveforms

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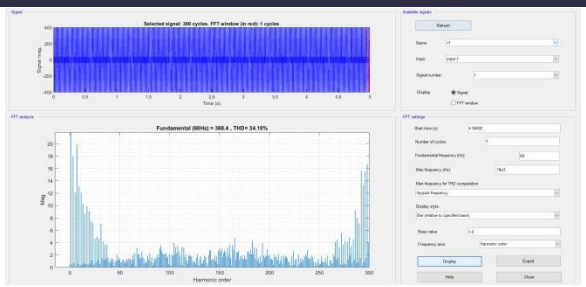

Fig. 19. FFT harmonic spectrum analysis of vat output voltage.

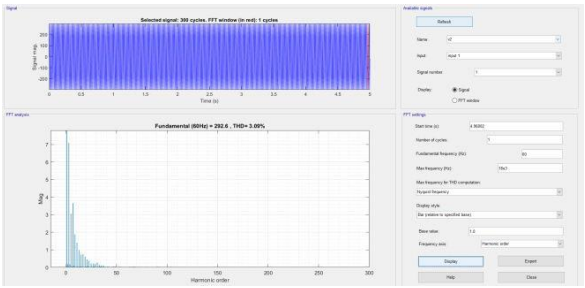

Fig. 20. Output voltage harmonic spectrum

Fig. 21 shows capacitor voltage V C2, output voltage v o, and output current io.

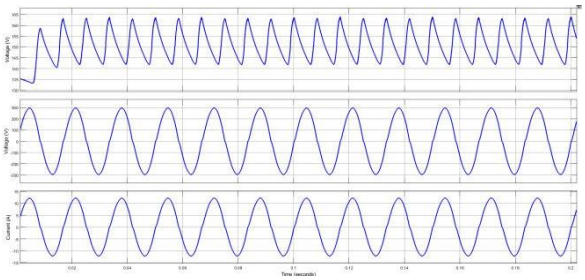

Fig. 21. Waveforms of vC2, vow, and io at 1000 W

VII. CONCLUSION

We employ digital signal processing to construct an entirely new seven-level inverter in this work. The basic idea behind the recommended design is to reduce the number of power devices. When we compare the new design to the old, we can observe that it dramatically reduces power consumption. Finally, a prototype seven-level inverter with a 400 V input voltage and an output voltage of 220 V rms /2 kW was produced in the lab. Experiments show that the maximum efficiency is 96.9% and the full load efficiency is 94.6%.

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