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Paper Authors

SRIKAKULAPU.RADHA SRAVANI, D.SRIDHAR (Ph.D) .
Sri Sunflower College of Engineering and Technology, Lankapalli , (A.P),INDIA.

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REALIZATION OF BIST ARCHITECTURE USING SRAM CELL BASED ON INPUT VECTOR MONITORING

***SRIKAKULAPU.RADHA SRAVANI **D.SRIDHAR (Ph.D)**

,PG Scholar, Dept of ECE (VLSID), Sri Sunflower College of Engineering and Technology, Lankapalli, (A.P),India.
Associate Professor,Head of the Department of ECE, Sri Sunflower College of Engineering and Technology, Lankapalli , (A.P),India.

Email ID: srikakulapu.radhasravani@gmail.com, sridhar.done@gmail.com.

ABSTRACT:

Input vector monitoring concurrent built-in self test (BIST) schemes perform testing during the normal operation of the circuit without imposing a need to set the circuit offline to perform the test. These schemes are evaluated based on the hardware overhead and the concurrent test latency (CTL), i.e., the time required for the test to complete, whereas the circuit operates normally. In this brief, we present a novel input vector monitoring concurrent BIST scheme, which is based on the idea of monitoring a set (called window) of vectors reaching the circuit inputs during normal operation, and the use of a static-RAMlike structure to store the relative locations of the vectors that reach the circuit inputs in the examined window; the proposed scheme is shown to perform significantly better than previously proposed schemes with respect to the hardware overhead and CTL tradeoff.

Keywords: Built-in self-test, design for testability, testing.

I INTRODUCTION

Built-In Self-Test (BIST), a large scale arrangement uses Test Generator to generate the test signals that are applied to the inputs of the Circuit under Test (CUT) [1]. In BIST, the normal operation of the CUT is stopped in order to carry out the test. Thus, if the CUT is connected for the function of the circuit, the performance of process is degraded. Input quantity checking existing BIST schemes [2] – [9] use vectors appearing to the inputs of the CUT during normal operation to perform on-line testing. The measures to evaluate this class of schemes are (a) the Concurrent Test Latency (CTL), i.e. the number of cycles that the CUT must operate in

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normal mode in order to expect that the existing test is completed and (b) the hardware in the system.

The Built-In Concurrent Self-Test (BICST) scheme is shown in Fig. 2.1. BICST is based on a pre-calculate test set and observing the vectors V arriving at the combinational CUT inputs and the respective outputs B. The Concurrent BIST Unit (CBU) measures the incoming signal against the pre-calculated test set and, if the input vector belongs to the test set, compares the result of the CUT with the known result; if the two quantities differ, an error is assumed to have happen in the CUT and the error signal is instantly active.

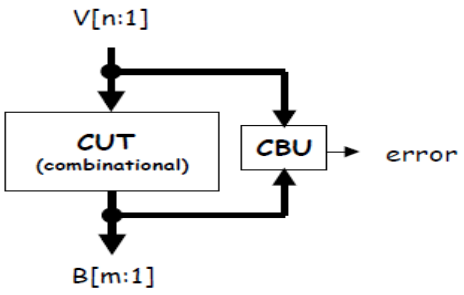

Fig 1: Input Vector Monitoring Concurrent BIST

In this, based on the idea of selecting a large group of the input signals and assumes them as inputs to a convert-based structure, successfully reduce the hardware overhead, compared to the scheme presented in while at the same time it gives for down test capabilities [16]. Other happening online BIST schemes use test patterns containing don't care values. An Input quantity testing on line existing BIST on relating to the decoding logic was presented. In this paper, a novel input vector monitoring concurrent BIST technique is presented, for Monitoring Input vectors based on minimum basic test sets, an idea proposed. The presented scheme is based on a basic test set with minimum number of patterns, and a number of patterns that differ from them exactly one bit.

II.LITERATURE SURVEY

Flip-flops and latches (collectively referred to as timing elements inthis paper) are heavily studied circuits, as they have a large impact onboth cycle time and energy consumption in modern synchronous systems. Previous work has focused on the energy-delay productof timing elements (TEs), but real designs include many TEs that arenot on the critical path and this timing slack can be exploited by usingslower, lower energy TEs. Instead of simultaneously optimizing fordelay and energy, critical TEs should be optimized to reduce delay andnoncritical TEs should be optimized to reduce energy. For example,used different structures for critical and noncritical flip-flops inthe context of a logic synthesis design flow.

Previous work often measured energy consumption using a limitedset of data patterns with the clock switching every cycle. But real designs have a wide variation in clock and data activity cross different TE instances. For

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example, low-power microprocessorsmake extensive use of clock gating resulting in manyTEs whose energy consumption is dominated by input data transitionsrather than clock transitions. Other TEs, in contrast, have negligibledata input activity but are clocked every cycle. Show significant energy savings when each TE instanceis selected from a heterogeneous library of designs, each tunedto a different operating regime. Detailed energy analysis to comparea number of TE designs, including designs that exploit particularcombinations of signal activity and timing slack. We gather statisticson TE activity in a pipelined MIPS microprocessor running SPECint95benchmarks and show that activity-sensitive TE selection can reducetotal TE energy without increasing cycle time. To the best of our knowledge,this paper is the first work that systematically exploits *signal activity*together with timing slack to reduce TE energy by selecting differentstructures.

III. PROBLEM OUTLINE

OBJECTIVE

In this project, input vector monitoring concurrent BIST scheme is planned, that compares favorably to previously planned schemes [2]-[7] with reference to the hardware overhead/CTL exchange. Input vector monitoring concurrent built-in self-test (BIST) schemes perform testing during the conventional operation of the circuit without imposing the circuit off- line to carry out the test. These arrangements are evaluated for supporting the hardware overhead and therefore the Concurrent Test Latency (CTL), i.e., the time needed for the test to complete the test, whereas the circuit operates normally.

EXISTING SYSTEM

In Existing system, many low-power approaches have been proposed for scan-based BIST. The design in existing system modifies scan-path structures, and lets the CUT inputs are unchanged throughout a shift operation, giving a multiple scan chains with several scan enable (SE) inputs to activate one scan chain at a time.

DRAWBACKS:

- More Complexity
- High power
- High cost

PROPESED SYSTEM

Let us take into account a combinational CUT with n input lines. Hence the possible input vectors for this CUT are 2^n. The planned theme is predicated on the thought of monitoring a window of vectors, whose size is W, with $W = 2^w$, where w is an integer, $w < n$. Each moment, test vectors belonging to the

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window are monitored, and if a vector performs successful, the RV is enabled. The bits of the input vector are divided into two different sets consisting w and k bits, respectively, such that w + k = n. The k (high order) bits of the input vector show whether or not the input vector belongs to the window under consideration. The w remaining bits show the relative location of the incoming vector within the current window. If the incoming vector belongs to the present window and has not been received during the examination of the present window, we say that the vector has performed successful and also the RV is clocked to capture the CUT's response to the vector. Input vector monitoring concurrent built-in self-test (BIST) schemes perform testing during the conventional operation of the circuit without imposing the circuit off- line to carry out the test. These arrangements are evaluated for supporting the hardware overhead and therefore the Concurrent Test Latency (CTL), i.e., the time needed for the test to complete the test, whereas the circuit operates normally.

IV. METHODOLOGY

In this project, a completely unique input vector monitoring concurrent BIST theme is planned, that compares favorably to previously proposed schemes with reference to the hardware overhead/CTL exchange.

The bits of the input vector are separated into two different sets containing w and k bits, specified w + k = n. The k (high order) bits of the input vector show whether or not the input vector belongs to the window under consideration. The w remaining bits show the relative location of the incoming vector within the current window. If the incoming vector belongs to this window and has not been received throughout the examination of the this window, we are saying that the vector has performed a hit and therefore the response verifier is clocked to capture the CUT's response to the vector. Once all vectors that belong to this window have reached the CUT inputs, we tend to proceed to examine next window. The below fig. shows the SRAM based concurrent input vector monitoring BIST architecture.

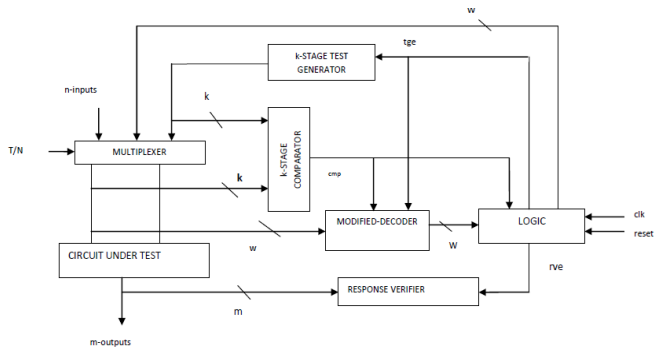

Fig.2: SRAM based concurrent input vector monitoring BIST

Let us think about a combinational CUT with n input lines, as shown in the above figure; hence the possible input vectors for this CUT are 2^n. The planned scheme depends on the concept of watching a window of vectors, whose size is W,

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with $W = 2^w$, wherever w is an integer, $w < n$. Every moment, the test vectors in the window are monitored, and if a vector performs hit, the rv is enabled. It operates in one out of two modes, normal, and test, depending on the value of the signal T/N. once T/N = 0 (normal mode) the inputs to the CUT are driven by the normal input vector. The inputs of the CUT are also given to the CBU as follows: the k (high order) bits are driven to the inputs of a k-stage comparator; the other inputs of the comparator are driven by the outputs of a k-stage test generator TG.

PROPOSED ARCHITECTURE:

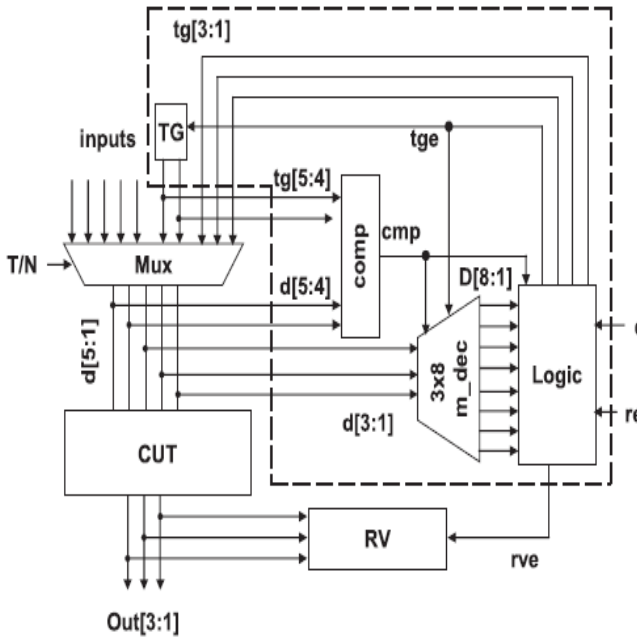

Fig.3: The proposed architecture with n=5, w=3 and k=2

The bits of the input vector are separated into two different sets containing w and k bits, specified w + k = n. The k (high order) bits of the input vector show whether or not the input vector belongs to the window under consideration. The w remaining bits show the relative location of the incoming vector within the current window. If the incoming vector belongs to this window and has not been received throughout the examination of this window, we are saying that the vector has performed a hit and therefore the response verifier is clocked to capture the CUT's response to the vector. Once all vectors that belong to this window have reached the CUT inputs, we tend to proceed to examine next window. The above fig. shows the SRAM based concurrent input vector monitoring BIST architecture.

V.RESULTS

RTL SCHEMATIC:

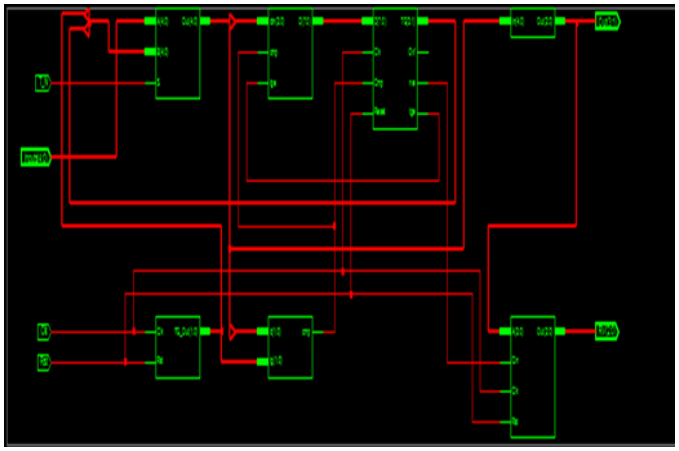

Fig. 4: RTL Schematic of clock gating

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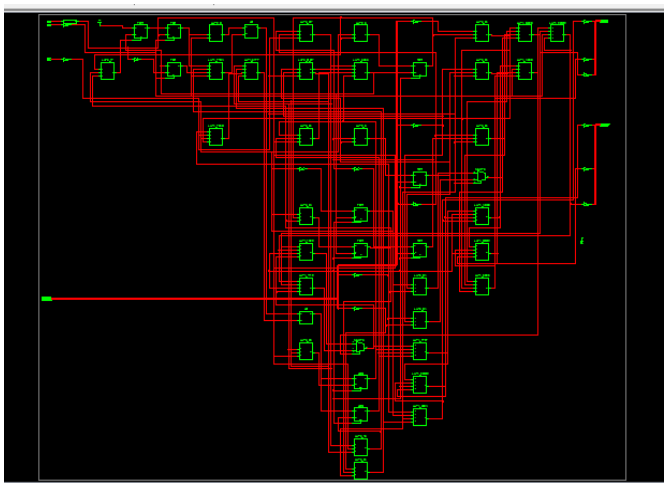

Fig 5: Technology Schematic of clock gating

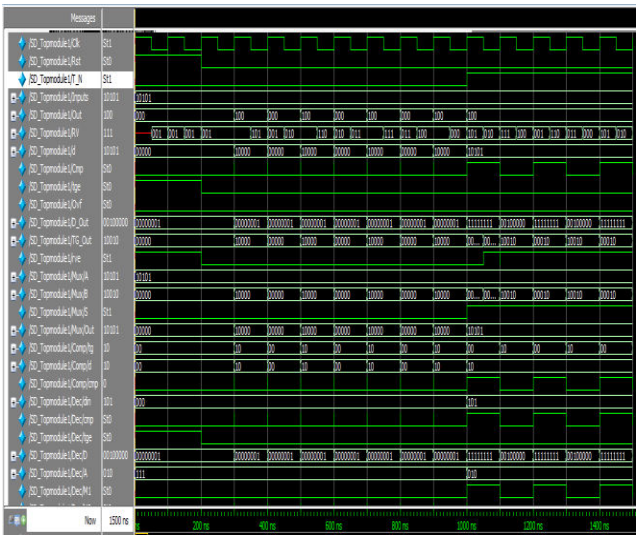

Fig. 6.: Simulation result of clock gating

RTL Schematic diagrams of modified circuit

Below shows the RTL Schematic window, from that we have to open that Synthesis –XST and then go to the RTL Schematic,

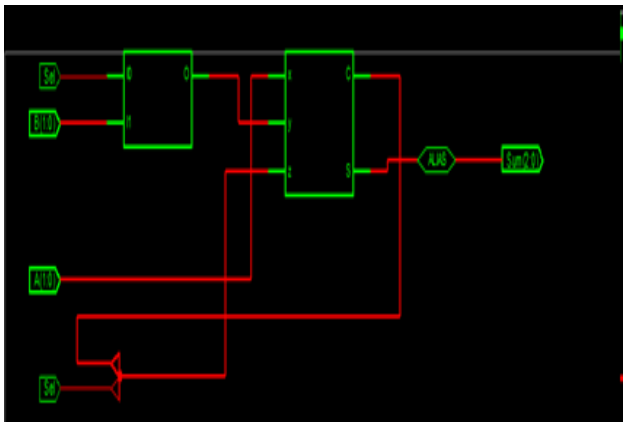

Fig.7: RTL schematic of clock gating of modified circuit.

Fig.8 shows the Technology schematic diagram of the entity model and when we have to do the double click on that each block, then it generates the internal diagrams those are shown

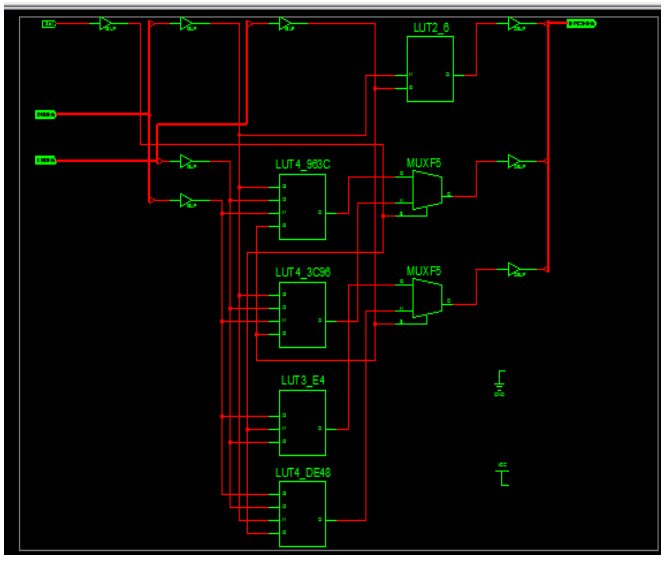

Fig.8: Technology diagram of clock gating of modified circuit

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SIMULATION RESULT

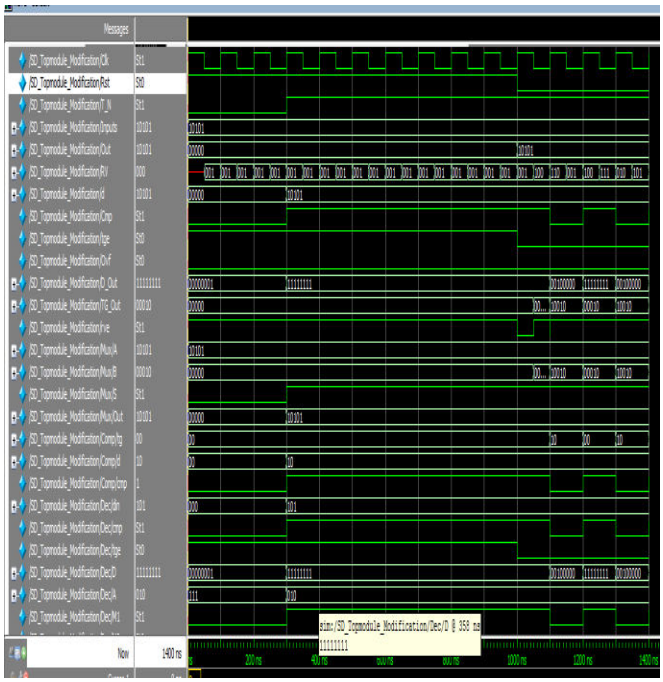

Fig.9: Simulation Result of the modified circuit.

SYNTHESIS REPORT

PAPER Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	12	7,168	1%	
Number used as Flip Flops	8			
Number used as Latches	4			
Number of 4 input LUTs	31	7,168	1%	
Logic Distribution				
Number of occupied Slices	21	3,584	1%	
Number of Slices containing only related logic	21	21	100%	
Number of Slices containing unrelated logic	0	21	0%	
Total Number of 4 input LUTs	31	7,168	1%	
Number of bonded IOBs	14	141	9%	
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	279			
Additional JTAG gate count for IOBs	672			

Table 1: Device Utilization Summary

Timing Summary:

Speed Grade: -4

Minimum period: 7.906ns (Maximum Frequency: 126.486MHz)

Minimum input arrival time before clock: 4.532ns

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Maximum output required time after clock: 22.263ns

Maximum combinational path delay: 22.324ns

MODIFICATION Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	5	7,168	1%	
Logic Distribution				
Number of occupied Slices	3	3,584	1%	
Number of Slices containing only related logic	3	3	100%	
Number of Slices containing unrelated logic	0	3	0%	
Total Number of 4 input LUTs	5	7,168	1%	
Number of bonded IOBs	8	141	5%	
Total equivalent gate count for design	36			
Additional JTAG gate count for IOBs	384			

Performance Summary			
Final Timing Score:	0	Pinout Data:	Pinout Report

Table 2: Modification Partition Summary

VI.CONCLUSION

BIST schemes constitute a pleasing result to the matter of testing VLSI devices. Input vector monitoring concurrent BIST schemes perform testing during the circuit normal operation without forcing the circuit off-line to perform the task; therefore they can prevent problems appearing in offline BIST techniques. In this project, input vector monitoring concurrent BIST architecture has been presented, based on the use of a SRAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. In this project we are successfully performed circuit operations and also testing the circuit.

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AUTHORS

D. SRIDHAR Working as Head of the Department of ECE, received the **M.Tech** degree in VLSI System Design from Avanthi Institute of Engineering and Technology, Narsipatnam, B.Tech degree in Electronics and Communication Engineering at Gudlavalleru Engineering College and also Pursuing his **Ph.D** in Low Power VLSI. He has total Teaching Experience (UG and PG) of 11 years. He has guided and co-guided 8 P.G students .His Research areas included VLSI system Design, Digital signal Processing, Embedded Systems.

SRIKAKULAPU.RADHA SRAVANI, PG scholar Dept of ECE (VLSID), Sri Sunflower College of Engineering and Technology, B.Tech degree in Electronics and Communication at eluru college of engineering and technology.