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IJIEMR Transactions, online available on 20 May 2017. Link :
http://www.ijiemr.org/downloads.php?vol=Volume-6&issue=ISSUE-3

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Volume o6, Issue 03, Pages: 185 – 191.

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DESIGN EFFICIENT 4-BIT ERROR CORRECTION & DETECTION FOR 16-BIT TRANSFORMATION

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ABSTRACT- As the complexity of communications and signal processing systems increases, so does the number of blocks or elements that they have. In many cases, some of those elements operate in parallel, performing the same processing on different signals. A typical example of those elements are digital filters. The increase in complexity also poses reliability challenges and creates the need for fault-tolerant implementations. A scheme based on error correction coding has been recently proposed to protect parallel filters. In that scheme, each filter is treated as a bit, and redundant filters that act as parity check bits are introduced to detect and correct errors. In this brief, the idea of applying coding techniques to protect parallel filters is addressed in a more general way. In particular, it is shown that the fact that filter inputs and outputs are not bits but numbers enables a more efficient protection. This reduces the protection overhead and makes the number of redundant filters independent of the number of parallel filters. The proposed scheme is first described and then illustrated with two case studies. Finally, both the effectiveness in protecting against errors and the cost are evaluated for a field-programmable gate array implementation.

Keywords- Coding, parallel filters, Hamming code,Sos checks, soft errors.

I. INTRODUCTION

Fault-tolerance is defined as the ability to produce correct results even in the presence of faults. Fault-tolerance is not a replacement of fault-prevention approach but a complement to it. Research activities in the area of fault-tolerant design have increased recently due to the following factors which have had a majorimpact on the design of these systems. I- Advances in Very Large Scale Integration (VLSI) technology have resulted in complex chips. This complexity could make the IC's susceptible to a diverse variety of failures and could lead to a decrease in reliability. II- Lower cost of extremely complex components and devices have made it

economical to introduce redundancy into the system.

III- Testing of complex components and systems are time-consuming and expensive, moreover there is a shortage of test equipment and experts.

IV- There is an ever-increasing demand for high reliability systems to undertake safety-critical applications, despite the fact that there is an upper limit to the reliability levels that can be achieved, using the fault-prevention approach.

V- In many applications, the system down-time needs to be minimized or even eliminated to improve the availability of the system. Basic to the design and implementation of fault-tolerant computing systems are consideration of the following three factors. Firstly, it is necessary to identify the basic principles which underlie all fault tolerant systems. Principles that can be applied at all levels in a system. Secondly, the measures and mechanisms to support and implement techniques based on these principles must be investigated. Thirdly, a framework is required to support a well structured approach to fault-tolerance in order to ensure that the additional complexity introduced by the fault tolerance techniques does not reduce rather than increase the reliability of the system.

Principles of Fault – Tolerance

To prevent faults leading to system failures five phases should be identified.

1] Error detection The presence of a fault in a system can produce an error which can cause a failure in the system. In order to tolerate a fault in a system generally its effects must first be detected, therefore an error detection mechanism should be deployed.

II) Reconfiguration If a fault is detected and a permanent failure located, the system should be able to reconfigure its components to replace the failed component or to isolate it from the rest of the system.

III) Retry In many cases a second attempt at an operation may be successful. This is particularly true in case of a transient fault. Thus a retry mechanism should be available in the system to handle these cases.

IV) Reset An error may cause too much damage to the system such that retry can not be successful and recovery may not be possible. In this case the system needs to be reset or restarted and therefore the design should provide these facilities.

IV) Fault treatment and continued service

After detection and (if necessary) reconfiguration, the effects of errors must be eliminated, and retry or reset should be used to check if the component can be used again (e.g. if failure caused by transient error). If possible the failed component should be replaced, repaired, and then put back to service. It is possible to have a fault-tolerant design with different permutations of this procedure. However to have an effective independent system all five phases are required. Having identified the principles of fault-tolerant design, now their implementation in hardware systems must be considered. The question of *how* fault-tolerance can be implemented in a system will be addressed in the next sections. But the questions of where fault-tolerance is

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actually required and how muchis necessary, which concerns the reliability requirement, will be discussed in chapter five.

II. ECC-BASED PROTECTION OF PARALLEL FILTERS

The impulse response $h[n]$ completely defines a discrete time filter that performs the following operation on the incoming signal $x[n]$:

$$y[n] = \sum_{l=0}^{\infty} x[n-l] \cdot h[l].$$

The impulse response can be infinite or be nonzero for a finite number of samples. In the first case, the filter is an infinite impulse-response (IIR) filter, and in the second, the filter is a finite impulse-response (FIR) filter. In both cases, the filtering operation is linear such that

$$y_1[n] + y_2[n] = \sum_{l=0}^{\infty} (x_1[n-l] + x_2[n-l]) \cdot h[l]$$

This property can be exploited in the case of parallel filters that operate on different incoming signals, as shown on Fig. 1. In this case, four filters with the same response process the incoming signals $x1[n]$, $x2[n]$, $x3[n]$, and $x4[n]$ to produce four outputs $y1[n]$, $y2[n]$, $y3[n]$, and $y4[n]$. To detect and correct errors, each filter can be viewed as a bit in an ECC, and redundant filters can be added to form parity check bits . This is also illustrated in Fig. 1, where three redundant filters are used to form the parity check bits of a classical single error correction Hamming code . Those correspond to the outputs $z1[n]$, $z2[n]$, and $z3[n]$. Errors can be detected by checking if

$$z_1[n] = y_1[n] + y_2[n] + y_3[n]$$
$$z_2[n] = y_1[n] + y_2[n] + y_4[n]$$
$$z_3[n] = y_1[n] + y_3[n] + y_4[n].$$

When some of those checks fail, an error is detected. The error can be corrected based on which specific checks failed. For example, an error on filter $y1$ will cause errors on the checks of $z1$, $z2$, and $z3$. Similarly, errors on the other filters will cause errors on a different group of zi. Therefore, as with the traditional ECCs, the error can be located. To correct the error, the failing output is reconstructed from the correct outputs. For example, when an error on $y1$ is detected, it can be corrected by making

$$y_{c1}[n] = z_1[n] - y_2[n] - y_3[n].$$

This ECC-based scheme reduces the protection overhead compared with the use of TMR. Table I summarizes the number of redundant filters needed for different parallel filter configurations. It can be observed that the number grows with the logarithm in base two on the number of filters. Therefore, the cost is

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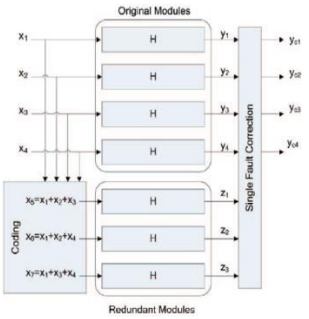
much smaller than TMR, in which the number of filters is tripled. The cost reductions were confirmed by some case study implementations. In this ECC-based scheme, the coding of the redundant filters is based on simple additions that replace the XOR binary operations in traditional ECCs. However, since both the inputs and outputs of the filters are sequences of numbers, a more general coding can be used. This type of coding has been explored for linear time-invariant systems (see, for example, but not for parallel filters. In those works, the processing of the linear system is modified to incorporate error detection and correction mechanisms. This is different from the approach proposed in this brief, where inputs are encoded but the processing of the filters is not modified. In the following, the use of a coding scheme for parallel filters in which the redundant filters are constructed as linear combinations of the original filters with arbitrary coefficients is explored.



ECC-based scheme for four filters and a Hamming code

FIG. 1 EXISTED SYSTEM

TABLE I
NUMBER OF REDUNDANT FILTERS IN THE ECC-BASED APPROACH

Number of parallel filters	Number of redundant filters
4	3
8	4
16	5
32	6

III.PROPOSED SYSTEM

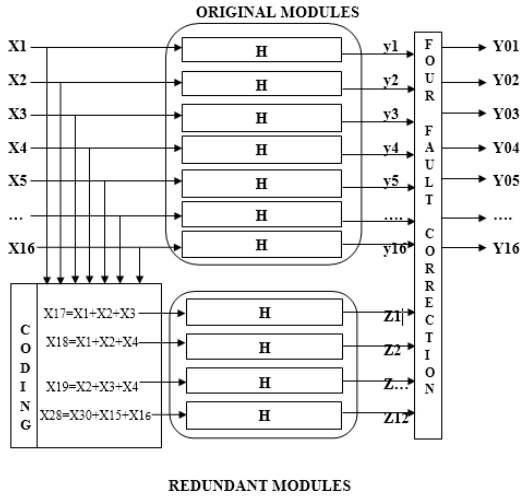


FIG. 2 PROPOSED SYSTEM

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of (or one or more faults within) some of its components. If its operating quality decreases at all, the decrease is proportional to the severity of the failure, as compared to a naively designed system in which even a small failure can cause total breakdown. Fault tolerance is particularly sought after in high-availability or life-critical systems.In

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parallel FFTS, the sum of squares techniques is combined to detect the errors and correct them. So this can be done by using the equivalent of simple parity bit for all the FFTS. In this when an error is found, the old of the parity FFT is used to correct the errors.

Now, this will be explained in a proposed technique for sixteen parallel FFTS. Here to the input a redundant FFT is added that as sum of two original FFTS. Sum of squares also added to check the error. IP error is found then correction can be done by recomputing the FFT in error using old of parity FFT (x) and rest of FFT outputs.

So in this way also we can detect the errors. There is a technique to detect errors (i.e.) we combine the sum of squares and ECC approach then we can detect the errors. Same process is applied to this technique to check the errors.

IV. RESULTS

The output waveform is shown in below figure for proposed system

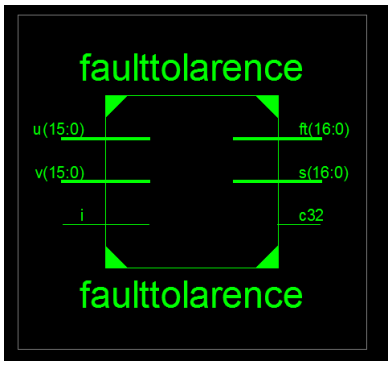

FIG. 3 RTL SCHEMATIC

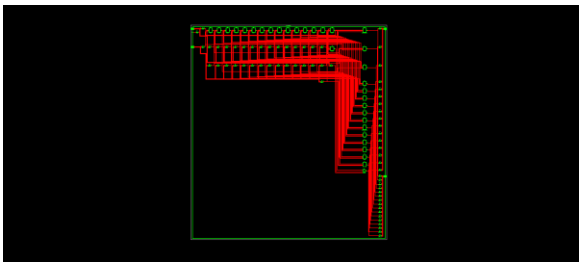

FIG. 4 TECHNOLOGY SCHEMATIC

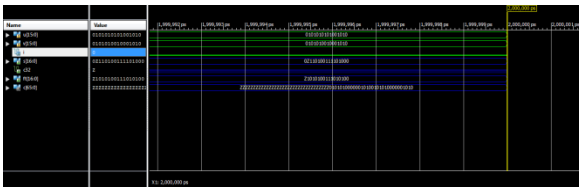

FIG. 5 OUTPUT WAVEFORM

V. CONCLUSION

This brief has presented a new scheme to protect parallel filters that are commonly found in modern signal processing circuits. The approach is based on applying ECCs to the parallel filters outputs to detect and correct errors. The scheme can be used for parallel filters that have the same response and process different input signals. The technique provides larger benefits when the number of parallel filters is large. The proposed architecture can be easily used to implement high order FIR filters e.g. 20-tap with different coefficients wordlength without suffering from large architecture reconstruction and with low hardware complexity needed for the design. The proposed scheme can also be applied to the IIR filters. The future work is to perform a VLSI implementation of pulse

shaping FIR filter for ultra wideband communications.

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