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# DESIGN AND IMPLEMENTATION OF REVERSE CARRY PROPAGATE ADDER (RCPA) ON FPGA

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**Abstract:** This work presents a reverse carry propagate adder (RCPA). In this adder, the carry sign propagates in a counter flow way that is from the maximum extensive bit to the least good-sized bit. subsequently, the deliver input sign has a better significance than the output carry. This RCPA is a new method to reduce the delay when compared to conventional adders. In RCPA the carry propagation leads to higher stability in the delay variations. Three different reverse carry propagate adder structures are implemented and their corresponding delay, area, and accuracy levels are evaluated on the FPGA device. The RCPFA which is having the approximate output is taken into consideration and the rate of error is also found that RCPFA is examined in the discrete cosine transform (DCT) block of the JPEG compression to estimate the accuracy of the proposed structure in Image processing applications.

## 1. Introduction

In very large scale integrated circuits we focus on delay, area, and power with these metrics one must even focus on the speed performance of the module. To increase speed and reduce power consumption we must compromise with the computation exactness of the module. These leads to the rough figuring which might be used for the submissions where up to some level of errors are tolerated [1]. These can be used in digital signal processing (DSP) which performs on humanoid sense-related indications [2].

In earlier explorations on approximate adders has reserved widespread procedures on fault weightiness and blunders opportunity deductions [3]-[7]. in this, the primary method is based totally on hybrid shape adders in which distinctive elements are applied this is precise most significant bits and approximate least significant bits. The error seems inside the bring input of exacts MSB part and seeing that maximum of processing's is finished in LSBs portion, power reduction of extra than 70% can be accomplished consuming the hybrid adder method [7]. in the second technique, the estimated adder constructions are taken into consideration. on this decreasing error chance, delay and power are the important thing layout standards [8]-[10].

In this proposed work focused on hybrid adders where we can make use of

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the estimated RCPFA. Here the contribution carry propagates in a hostage flow method that is from the most significant bit to the least significant bit to procedure the carry output. In this RCPA proliferation is achieved by presenting a prediction signal substitute as an output signal. As carry propagates from MSB to LSB the carry weight decreases so this adder is known as approximate reverse carry propagate adder. This adder improves the delay compared to the existing approximate adders. This type of adder is less vulnerable to delay variations when compared to the conventional ones.

## 2. Literature Survey

some estimated full adders are used in mixture adders are contemplated. An adder plays out the expansion of two paired numbers. Two essential adders are ripple carry adders and carry look-ahead adders. In an n-bit RCA, the convey of every FA is spread to the following FA along these lines the postponement and circuit unpredictability increments. The CLA comprises of n units that work in corresponding to create the entirety and spread signs for producing the lookahead conveys. The postponement of CLA is shorter than RCA. Be that as it may, a CLA requires bigger circuit territory, causing higher force dispersal.

Many approximate plans have been projected by lessening the basic way and equipment multifaceted nature of an exact adder. The ripple carries adder (RCA) has the most minimal force and zone utilization among all the current adder structures. In any case, it experiences a huge delay. and to improve the speed and vitality effectiveness of this adder and some earlier works have relinquished the precision.

The five approximate mirror adders (AMA) structure having a more modest number of transistors contrasted with that of traditional adder has been anticipated. These plans depend on disentangling the inner structure of the mirror adder prompting the littler region and force utilization just as higher speed, the reality table of AMA-1 to AMA-4 has appeared in the table.

Table I: Function table for different adders

| Inputs | | | Conv FA | | AMA -1 | | AMA-2 | | AMA -3 | | AMA-4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | $C_n$ | S | $C_o$ | S | $C_o$ | S | $C_o$ | S | $C_o$ | S | $C_o$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |

At the point when fundamental doors depend on the pass transistors (PT) or transmission gate (TG) brings about lower power utilization. These prompts a decrease in vitality and deferral [4]-[6] These outcomes in lower dc commotion edge. In [5], similar to take a shot at AMA by rearranging the inward structure of the TG-based ordinary FA, Like the TGA's surmised FA's called estimated XNOR-based adders and inaccurate adders dependent on PT have been proposed in [4] and [6], separately. In these structures,

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lower region and force utilization was accomplished by bringing down the quantity of transistors check gets less than ten. Then again, by utilizing the static rationale, the adequacy of the proposed estimated FA has vanished. It ought to be referenced that in [6], just the adequacy of a solitary FA has been concentrated without assessing its viability in the RCA's.

## 3. Reverse Carry propagate Adder

The reverse carry propagate adder is designed using the conventional full adders. The main working principle of RCPA is to propagate the carry in a counter flow manner from the most significant bit to the least significant bit. The reverse carry propagate adder is introduced to reduce the delay in carry propagations, this operation is done by introducing a forecast signal. Three implementations of reverse carry propagate adder are considered to improve the efficiency of the circuits.

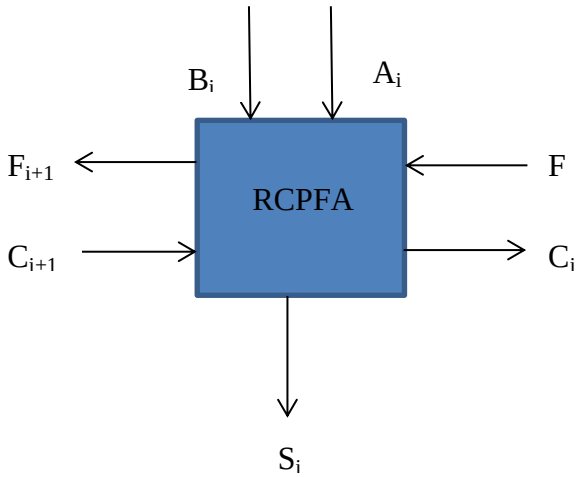


Fig.1: Basic RCPFA Adder

The RCPFA has four inputs ($A_i$,$B_i$,$C_{i+1}$,$F_i$) and two outputs($C_i$,$S_i$).The inputs A and B are considered of same weight and $C_{i+1}$ is the carry of the next stage which is given as the input. The outputs $S_i$ is the sum result and the $C_i$ is the carry generated. The generation of forecast signal($F_i$) optimizes the RCPFA structure. Initially, the input carry and the forecast signal are considered as 0 bit.

The RCPFA1 structure consists of 26 transistors. These transistors are used to build the AOI and OAI circuits. There are two AOI and OAI circuits. The input of First AOI is $A_i$,$B_i$,$C_{i+1}$ and the output obtained is $X_i$.

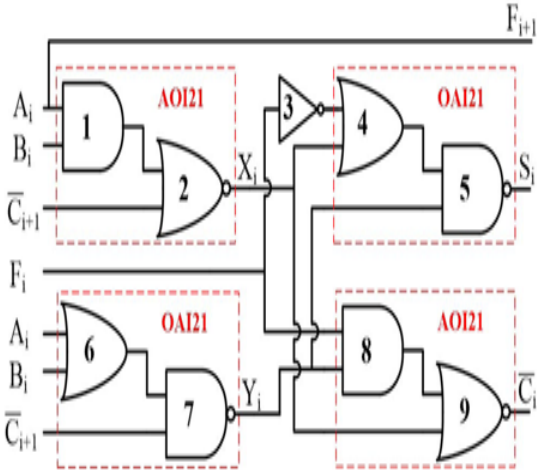


Fig.2: RCPFA1 Structure

The input of second OAI is $A_i$,$B_i$,$C_{i+1}$ and the output obtained is $Y_i$. The forecast signal is initially taken as 0 which is given as the input to the succeeding circuits. The final output of the first implementation of the RCPFA (RCPFA-I) is sum result $S_i$ and carry $C_i$. The input $A_i$ is given as the forecast signal for the next stage ($F_{i+1}$).

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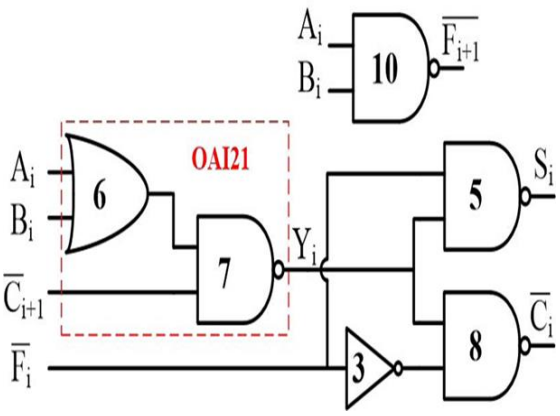


Fig.3: RCPFA2 Structure

The RCPFA2 structure consists of 16 transistors. These transistors are used to build the AOI and two NAND circuits. The input of First AOI is $A_i$, $B_i$,$\wedge C_{i+1}$ and the output obtained is $Y_i$ .The forecast signal is initially taken as 0 which is given as the input to the NAND gates. The forecast signal of the next stage is the NAND of $A_i$ and $B_i$. This implementation is better than the above implementation as it optimizes the forecast signal and uses a smaller number of gates.

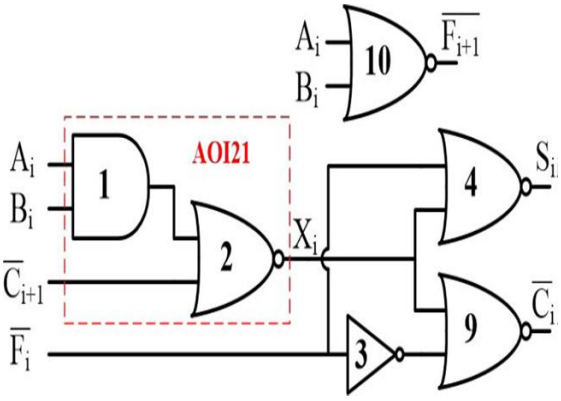


Fig.4: RCPFA3 Structure

The RCPFA3 structure consists of 16 transistors. These transistors are used to build the AOI and two NOR circuits. The input of First AOI is $A_i$, $B_i$,$\wedge C_{i+1}$ and the output obtained is $X_i$ .The forecast signal is initially taken as 0 which is given as the input to the NOR gates. The forecast signal of the next stage is the NOR of $A_i$ and $B_i$. This implementation is better than the above implementation as it optimizes the forecast signal.

## 4. Implementation and Results

As the above three implementations are approximate. There is a need to design an accurate adder. The first implementation is worst case adder, so we have been designing an accurate RCPFA-III which shows the rate of error as the difference in these results.

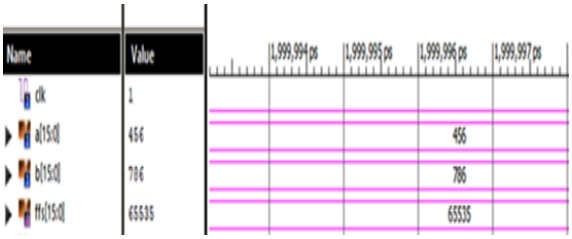


Fig.5: Simulation results of RCPFA1
Inputs: 456 , 786
Output: 65535

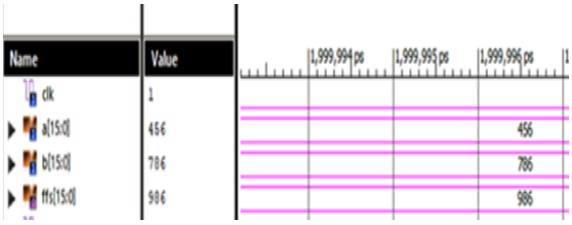


Fig.6: Simulation results of RCPFA2
Inputs: 456 , 786
Output: 986

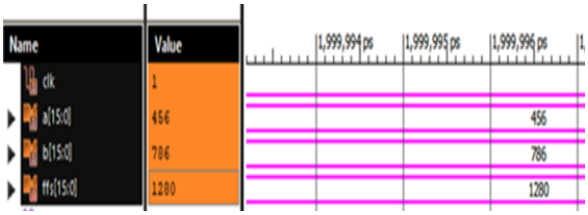


Fig.7: Simulation results of RCPFA3

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Inputs: 456 , 786
Output: 1280

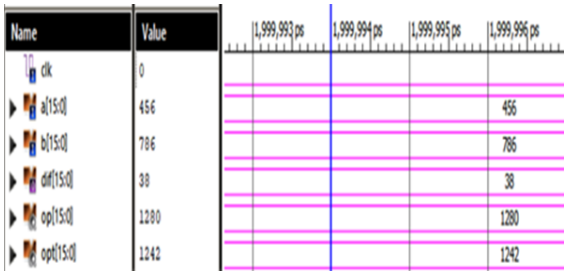


Fig.8: Simulation results of Error Analysis using RCPFA

Input: 456 , 786
Output: 1280(the output we got)
Output to be obtained is 1242
Difference in outputs is 38

Fig.9: Simulation results of Image compression.

Table II: Resource utilization Summary

| FPGA: Spartan 3 Xc3s100e-5-vq100 | Slices | Flip-flops | LUTs |
|---|---|---|---|
| RCPFA-I | 79 | 125 | 75 |
| RCPFA-II | 95 | 154 | 62 |
| RCPFA-III | 95 | 154 | 78 |

Table III: Delay and Power Report

| FPGA: Spartan 3 Xc3s100e-5-vq100 | Delay (ns) | Power (W) |
|---|---|---|
| RCPFA-I | 2.787 | 0.034 |
| RCPFA-II | 2.81 | 0.034 |
| RCPFA-III | 2.81 | 0.034 |

The RCPFA-III approximate adder is used for image compression using DCT algorithm. The DCT takes the input image in the form of bits (converted pixels) and the bits are processed, and compressed bits are again given to the MATLAB code which results in the output image.

## 5. Conclusion

In this work, a new technique of estimated RCPFAs which propagates convey from furthermost substantial to least significant bits. The converse carry propagation provides sophisticated steadiness in delay variations. The effectiveness of the anticipated estimated full adders and the amalgam adders which comprehended them has been investigated in XILINX ISE 14.7 and as well MATLAB software for image compression method using DCT. All the implementations are carryout on Spartan 3Xc3s100e-5-vq100 FPGA module. The outcomes designated that exploiting the anticipated RCPFAs in the hybrid adders delivers most efficient optimizations. Error analysis shows significant variance in difference when compared with accurate addition.

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