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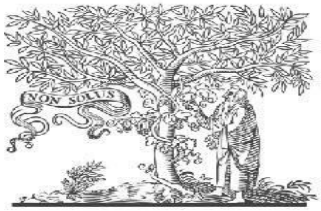

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Multilevel Inverter with Lower Switch Count

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Abstract

Industrial drives use multilevel inverters (MLI) in a variety of ways. MLI applications in industrial drives have multiplied dramatically over the past 20 years. But, for more efficiency and dependability, we always require fewer devices. A Multilevel Inverter (MLI) output voltage can be adjusted using several modulation techniques. Intensive study is underway to reduce the number of DC power supplies and switches used in Multilevel Inverter without minimize the number of output levels. To increase the power handling capacity without purchasing new converters, MLI's modular design is implemented. This project demonstrates a cascaded H-bridge (CHB) converter with a decreased switch count that generates a seven-level output from a single stiff DC source (battery). To get a better output voltage waveform, gate pulses for the switches have been generated using the nearest level control (NLC) pulse-width modulation technology. The provided mathematical analysis is supported by simulation and experimental findings. The fluctuation of total harmonic distortion (THD) with modulation index is also investigated.

Keywords: Cascaded H-bridge (CHB) converter, MATLAB, Nearest level control (NLC), Total harmonic distortion (THD), Multilevel Inverter (MLI).

1. Introduction

In 1981, the concept of a multilevel inverter was proposed [1,2]. Using a variety of DC voltage sources, these converters provide a sinusoidal-looking stepped output voltage [2-4]. Because the output of inverters has less harmonic distortion, they are frequently employed in industrial applications. In industrial applications, it is commonly used. The application field includes static VAR generation, the flexible AC transmission system (FACTS), solar photovoltaic systems [6, 7], and rechargeable batteries [8]. As a rectifier in the car for regenerative braking, MLI is also employed in traction drive [9]. The use of several switches and DC sources in multilevel inverters has increased the complexity of the circuitry, setting new possibilities for research to minimize it. The number of DC sources and switches

used in MLI is being minimized without affecting the number of output levels [10, 11]. The research project may be effectively split into two parts: developing appropriate control algorithms and discovering fresh topologies for attaining the previously mentioned purpose. Diode clamped, flying capacitor, and cascaded multilevel converters are the three categories for conventional multilevel converters. Cascaded multilevel converters are said to provide a simple, dependable, and modular structure. Asymmetrical CHB converter and symmetrical CHB converter are additional categories for cascading multilevel converters [12]. Asymmetrical CHB converters employ sources of DC voltage which are not equivalent to those used by symmetrical CHB converters. In compared to the various control approaches described in [13–16], overall least THD is produced with a simpler control.

An eight-switch cascaded H-bridge asymmetrical multilevel inverter with seven levels is investigated in this work. Increasing the level count improves the shape of the output waveform [17]. Multilevel inverter modulation control often uses both space vector PWM technologies and conventional PWM control techniques. The downside of the old PWM systems is the power waste in the switches owing to the high switching frequency. For motor driving applications, low switching frequency control techniques like the fundamental frequency approach and the concept of active harmonic removal has been proposed. A simulation model for the proposed seven-level CHB converter is constructed in the MATLAB®/Simulink environment. The study also includes results on the converter's performance.

2. Working of Multilevel Cascaded H-Bridge Inverter

With (n -1) /2 DC sources and 2(n-1) switches can generate n-level output in a cascaded H-bridge inverter. Hence, three DC sources are needed to provide 7-level output with 12 switches, The switch count will be significantly reduced by asymmetric-cascaded CHB, though at the cost of a reduction in redundant states. Also, irrespective of the modulation approach, the output voltage will be asymmetric. Yet, the financial advantages of fewer switches and DC voltage sources are crucial in these kinds of inverter configurations for their use. The circuit design for two cascaded H-bridge converters is shown in Figure 1.The switching strategy for various output levels that might be produced by an asymmetric-cascaded CHB with various DC source combinations is shown in Fig 2. Using a battery voltage combination of Vdc and 2Vdc, a seven-level output might be produced.

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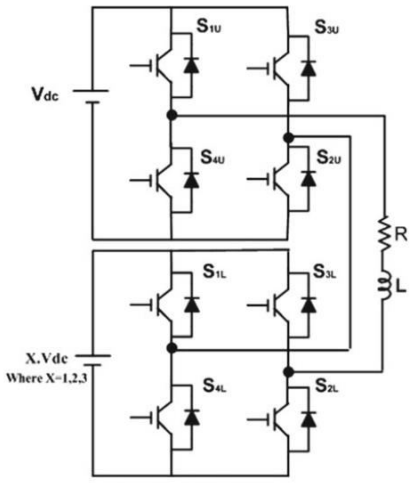

Figure1: Two Cascaded H-Bridge Converters

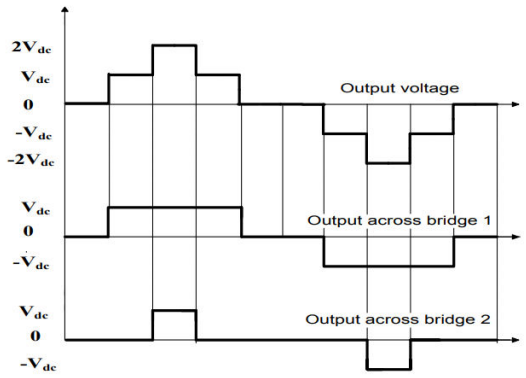

Figure2: Five levels of output over each H-bridge

3. Nearest Level Control

The performance of a standard NLC degrades for a small count of levels, and the THD in the resultant voltage is considerable. Modified NLC is implemented in a modular multilevel converter suggested in [18] using model predictive control. To control and reduce the variations in a 4 level MLI of capacitor voltage, a control mechanism based on SPWM is utilized in [19]. While being easy to implement, the THD produced with the SPWM is high by IEEE standards at 24.7% [19]. A stepped voltage waveform for a cascaded multilevel inverter structure is produced in [20] using a phase-shifted PWM modulation approach. An enhanced NLC approach for MLI is put out in [21], and it is discovered that for a given number of submodules, the number of levels grows, lowering the THD in the resultant voltage. For grid-connected inverters, writers in [22] propose a hybrid PWM/Pulse Amplitude Modulation strategy. The converter's efficiency is raised by the suggested hybrid modulation approach. In [23], 15-levels are produced using the NLC switching approach.

4. Execution of the Suggested CHB Strategy

Fig. 1 shows the cascaded h-bridge (CHB) inverter's generalized circuit configuration. One dc supply and four switches are included in one h-bridge device. Using two H-bridge units, the suggested NLM approach is applied on the seven-level CHB inverters. DC sources have magnitudes of V1 = V and V2 = 2V.

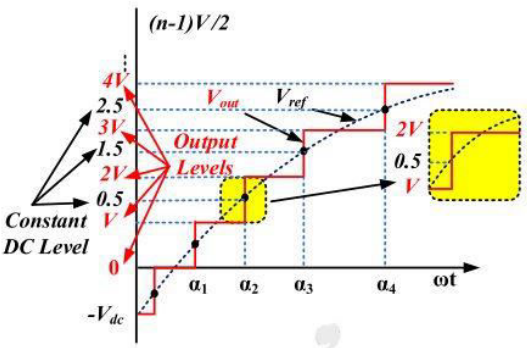

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Figure3: Figure shows how a n level CHBMLI is implemented using the NLC scheme.

5. Modulation and Switching Control

Equations provide the set of equations needed to perform the NLM system**.**

3msin (α1) = g -----(1)

3msin (α2) = 1 + g----- (2)

3msin (α3) = 2 + g -----(3)

The switching angles in this case are αi(i = 1, 2, and 3), and g is the variable DC level of the VSNLM. The range of values is 0 to 1. The THD formula in eq. (A) was computed for harmonics up to 49 using data from [29]. By minimizing the THD expression provided in eq, one might determine g for a given value of the modulation index m. (A). As a result, appropriate values of g are found for minimal THD for all values of m between (0, 1). Equations (4) and (5) yield the set of (m, g) points, which may be used to determine the connection between m and g (Fig (5).

g = 1.37m − 0.87 for (m > 2/3) ---- (4)

g = 1.38m − 0.42 for (1/3 < m < 2/3) ---(5)

$$THD_{7L} = \sqrt{\left(\frac{\pi^2}{8}\right).\frac{9V_{dc}^2 - \frac{2}{\pi}\left[\alpha_1 V_{dc}^2 + 3\alpha_2 V_{dc}^2 + 5\alpha_3 V_{dc}^2\right]}{(V_{dc}\cos\alpha_1 + V_{dc}\cos\alpha_2 + V_{dc}\cos\alpha_3)^2} - 1}$$

------[A]

6. Multilevel Output Generation Using Cascaded H-Bridge Converter

By cascading two or more H-bridge converters, multilevel output can be produced. In principle, cascaded converters employing an equal-number DC source might provide the (2n + 1) level. By selecting an inequitable DC source, the level count rises. Two cascaded H-bridge converters are shown in Figure 1. Tables 1 illustrate the switching strategy for creating multiple multilayer outputs from two cascaded H-bridge converters with different DC voltage levels.

6.1 Five-Level Output

The switching scheme for generating five-level output

S_{1U}	S_{2U}	S_{3U}	S_{4U}	V_1	S_{1L}	S_{2L}	S_{3L}	S_{4L}	V_2	V_0
On	On	-	-	V_{dc}	On	On	-	-	V_{dc}	$2V_{dc}$
On	On	-	-	V_{dc}	On	-	-	-	0	V_{dc}
-	-	-	-	0	-	-	-	-	0	0
-	-	On	On	$-V_{dc}$	-	On	-	On	-	$-V_{dc}$
-	-	On	On	$-V_{dc}$	-	-	On	On	$-V_{dc}$	$-2V_{dc}$

Table1: Five Level Switching Scheme

7. Simulation and Experimental Results

The sine block included in the SIMULINK library browser is used to create the sine wave. The frequency of sine wave is taken 50 Hz. Modulation value (m) is taken as 1 because for less than m=0.8, levels will reduce so we consider m=1. By mathematical equations g value will be 0.5(g=0.5). Generate pulses by pulse generator block. Eliminate negative wave forms in positive signal vice versa by multiplying pulse to positive and negative signals. Resultant signals are combined

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and injected to Cascaded H-Bridge circuit and voltages of dc sources are 1:2 ratio and switching scheme is as shown in table (2).

Levels	S1	S2	S3	S4	S5	S6	S7	S8	VRL
1	ON	OFF	OFF	ON	OFF	ON	OFF	ON	V
2	OFF	ON	OFF	ON	ON	OFF	OFF	ON	2V
3	ON	OFF	OFF	ON	ON	OFF	OFF	ON	3V
4	OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
5	OFF	ON	ON	OFF	OFF	ON	OFF	ON	-V
6	OFF	ON	OFF	ON	OFF	ON	ON	OFF	-2V
7	OFF	ON	ON	OFF	OFF	ON	ON	OFF	-3V

Table2: Seven Level Switching Scheme

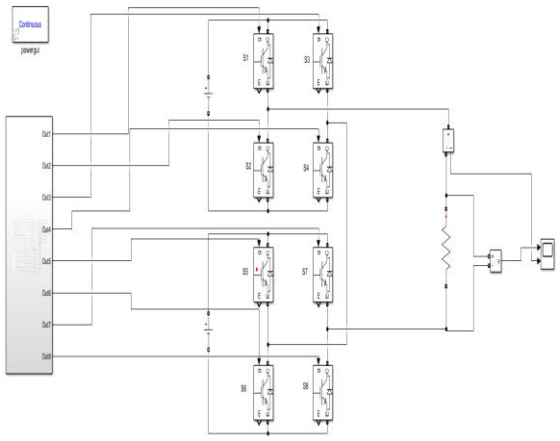

Figure4: Simulation Diagram for Seven level Cascaded MLI with Reduced Switch Count.

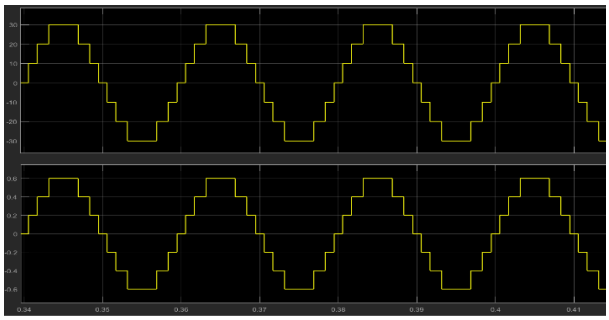

Figure5: Simulation Results

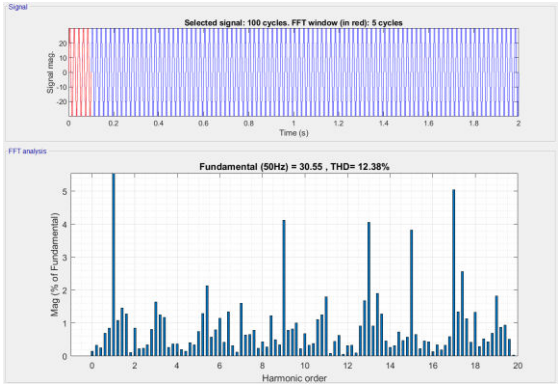

Figure6: THD Analysis

8. Conclusion

This study looked at a different method for generating a cascaded H-bridge multilevel inverter's seven-level output with few switches and sources. A Nearest Level Control (NLC) technique was successfully used to reduce the THD of the output voltage. The outcomes of the experiments have verified the technique.

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