International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

IJIEMR Transactions, online available on 21st June 2020. Link
:http://www.ijiemr.org/downloads.php?vol=Volume-09&issue=ISSUE-06

Title: RANDOM ACCESS SCAN ARCHITECTURE DESIGN FOR MIXED MODE SCAN TEST
Volume 09, Issue 06, Pages: 91-99

Paper Authors

M.SAILAJA, N.VARALAKSHMI

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

RANDOM ACCESS SCAN ARCHITECTURE DESIGN FOR MIXED MODE SCAN TEST

M.SAILAJA[1], N.VARALAKSHMI[2]
[1]PG Scholar, Dept of ECE, SIR C.V. RAMAN Institute of Technology & Science, AP, India
[2] Assistant Professor, Dept of ECE, SIR C.V. RAMAN Institute of Technology & Science, AP, India

Abstract: The ease of testing and high test coverage has made it gain widespread industrial acceptance. However, there are penalties associated with the serial scan design. These penalties include performance degradation, test data volume, test application time, and test power dissipation. The performance overhead of scan design is due to the scan multiplexers added to the inputs of every flip-flop. In today's very high-speed designs with minimum possible combinational depth, the performance degradation caused by the scan multiplexer has become magnified. Hence, to maintain circuit performance, the timing overhead of scan design must be addressed. In this project, we propose a new scan flip-flop design that eliminates the performance overhead of serial scan. The proposed design removes the scan multiplexer from the functional path. The proposed design can help improve the functional frequency of performance critical designs. Furthermore, the proposed design can be used as a common scan flip-flop in the "mixed scan" test wherein it can be used as a serial scan cell as well as a random access scan (RAS) cell. The *mixed scan* test architecture has been implemented using the proposed scan flip-flop

INTRODUCTION

With expanding structure intricacy in present day SoC plan, numerous memory examples with various sizes and types would be incorporated. To test the majority of the memory with generally minimal effort turns into a significant issue. Worked in Self Test, or BIST, is the strategy of planning extra equipment and programming highlights into incorporated circuits to enable them to perform self-testing, i.e., testing of their own activity (practically, parametrically, or both) utilizing their own circuits, in this way lessening reliance on an outer mechanized test hardware (ATE). BIST is a Design-for-Testability (DFT) procedure, since it makes the electrical testing of a chip simpler, quicker, increasingly effective, and less expensive. The idea of BIST is pertinent to pretty much any sort of circuit, so its execution can fluctuate as broadly as the item assorted variety that it takes into account.

Current VLSI circuits, e.g., information way designs, or computerized flag handling chips normally contain number juggling modules [accumulators or number-crunching rationale units (ALUs)]. This has terminated the possibility of number-crunching BIST

(ABIST) . The essential thought of ABIST is to use gatherers for worked in testing (pressure of the CUT reactions, or age of test designs) and has been appeared to result in low equipment overhead and low effect on the circuit ordinary working rate.

The objective of scan design is to achieve full controllability and observability of every flip-flop in the design. In a full scan design, each flip-flop is replaced by a scan flip-flop. A scan flip-flop is nothing but a muxed input master-slave based *D* type flip-flop. The scan multiplexer has two inputs: data input (*D*) and scan input (*SI*). The input selection is performed using a control signal called *test enable* (*TE*). In functional mode, data input is selected and the scan flip-flop function as a regular flip-flop. In test mode, scan input is selected, and all the scan flip-flops connect in a serial fashion to form one or more serial shift register(*s*). The serial shift register(*s*) is popularly known as scan chain(*s*). All flip-flops of the scan chain are loaded with desired data by consecutive application of the clock signal. A full scan design reduces the sequential test problem to combinational test problem.

The serial scan is obviously not free from drawbacks. There are some inherent penalties associated with the serial scan. These penalties include: 1) performance overhead, 2) test data volume, 3) test power consumption, and 4) test application time. The performance overhead of serial scan is due to the scan multiplexer. The scan multiplexer falls into each clocked path and adds performance penalty of approximately two gate-delays. A circuit without scan design and with scan design is shown in Figure 1. As it is observable in Figure 1*a*, the critical path of a sequential circuit without scan insertion is decided by the longest combinational path between two flip-flops. However, in a scan inserted sequential circuit (see Figure 1*b*) the same critical path is elongated by a scan multiplexer at the end of the combinational path. The scan design also adds an extra fanout at the output of a flip-flop. Both of these factors increase the critical path delay, hence reduces functional clock speed by 5% to 10%. This makes it necessary to eliminate the performance overhead of the scan multiplexer. Several solutions have been proposed to alleviate the performance penalty of scan design. One such solution that alleviates the performance overhead, as well as the other penalties associated with the serial scan design is the use of partial scan instead of full scan. In partial scan design, only a subset of all flip-flops in Circuit-Under-Test (*CUT*) are replaced by scan flip-flops to form a scan chain. This subset does not include flip-flops of the critical paths, hence reduces the performance penalty of scan. Additionally, the partial scan design techniques also reduce test data volume and test application time which are directly related to test-cost. However, the partial scan design techniques may lead to lower fault coverage of the *CUT*.

2. FULL SCAN DESIGN

Full scan is a DFT scheme which reduces ATPG complexity by allowing memory elements to be controlled and observed during testing and test generation. A gate level design is converted to a full scan

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

design by replacing all flip-flops (FFs) with scan FFs, and connecting the scan FFs (SFFs) to create a scan chain [1,2]. Mentor Graphics DFTAdvisor tool was used to insert scan chains into both optimized designs for this project. In both designs, 1,346 flip-flops were replaced with scan flip-flops.

2.1 Scan Chains

A typical scan flip-flop is shown in figure 1. Each inserted SFF has two extra inputs, scan_in and scan_enable, and an extra fanout, scan_out. To form a scan chain, the SFFs are linked together as shown in figure 3, and three signals are routed to I/O pins, scan_enable, scan_in, and scan_out. The scan chain can be set to either normal or scan mode by setting the scan_enable primary input. In normal mode, SFFs capture data from their data input. When the circuit is set to scan mode, the scan chain forms a shift register that can be loaded and unloaded serially using scan_in and scan_out I/O pins, allowing memory elements to be both controllable and observable [1,2]. After inserting scan circuitry into both areaOpt and delayOpt designs, two I/O pins were added, a scan in pin and a scan enable pin. The most significant bit of the Memory_Address output is used for scan out in both cases.

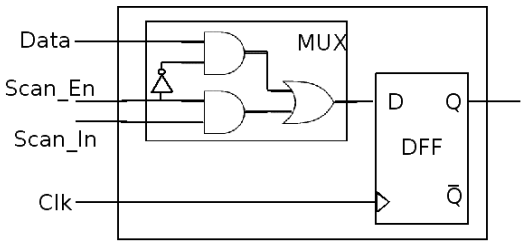


Figure 1: Typical Scan Flip-Flop

3.EXISTING SYSTEM

A conventional scan flip-flop design is shown in Figure 4.1. This scan cell is a master-slave latch based positive edge triggered muxed input D type flip-flop . The transmission gate T1 and the inverter pair connected back to back via transmission gate T2 forms the master latch. The slave latch comprises of transmission gate T3 and the inverter pair connected back to back over transmission gate T4. The multiplexer at the input of master latch selects between functional input (D) and scan input (SI) depending upon the value of test control signal test enable (TE). In test mode, when TE is high (1), SI is selected and is connected to master latch's input. When the clock signal (CP) is low (0), the value of SI propagates to the master latch. In the meanwhile, the

slave latch retains the value from previous clock cycle. The value latched into the master propagates to slave latch when CP turns to high (1), and to the output Q of scan flip-flop. Correspondingly, when the test enable signal (TE) is set to 0, functional input D is selected, and the circuit operates in functional mode.

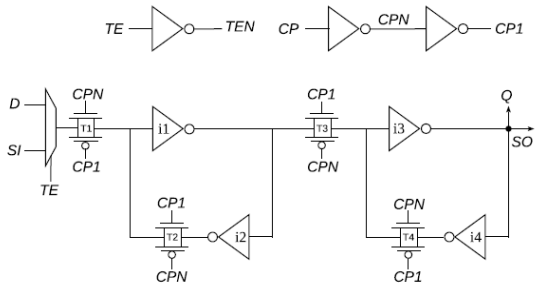


Figure 2. Conventional Scan Flip-Flop Architecture

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

4. PROPOSED SCAN FLIP-FLOP DESIGN

This working of the proposed scan flip-flop in different modes of operation. The proposed scan

flip-flop's schematic design is shown in Figure 3. Instead of a multiplexer at master latch's input, the proposed design uses a separate path for loading test vector values into the master latch. Furthermore, the proposed scan flip-flop uses a low-cost dynamic slave latch for shifting of test vectors in the test mode. In functional mode, functional slave latch's output *Q* drivesthe combinational circuit inputs. The master latch of the proposed scan flip-flop is formed by transmission gate *T*1, and inverter pair (*i*1, *i*2) connected back to back via transmission gate *T*2. Similarly, the slave latch is formed by transmission gate *T*3, and inverter pair (*i*3, *i*4) connected back to back via transmission gate *T*4. The dynamic slave latch comprises transmission gate *T*7 and inverter *i*7. The test mode path is formed by adding transmission gate *T*5, *T*6, buffer *i*5, and inverter *i*6 to the master latch structure. It should be noted that the extra gates added to the master stage to form the test mode input path are not on the functional path. This extra circuitry remains disabled during the functional mode, and the proposed scan flip-flop acts as a regular flip-flop. The master latch and the slave latch are controlled by functional clock signal *CP*. The test mode input path is disabled by the *test_enable* cum scan clock signal *SCK*. Note that, the *SCK* signal in the proposed scan cell is functionally equivalent to the *test_enable* signal *TE*, however, in contrast to the conventional scan design in which *TE* is a purely combinational signal, *SCK* is a low frequency or quasi-sequential signal.

The *SCK* signal is used both as test control as well as a low frequency scan clock signal in the proposed scan design. Since the scan operation is performed at a much lower frequency, typically at 10MHz to 50MHz, compared to the system or functional clock frequency [23], the routing of *SCK* as a slow frequency scan clock signal will not introduce much overhead in terms of area and power. The details of the working of the proposed design in different modes of operation are explained in the following subsections:

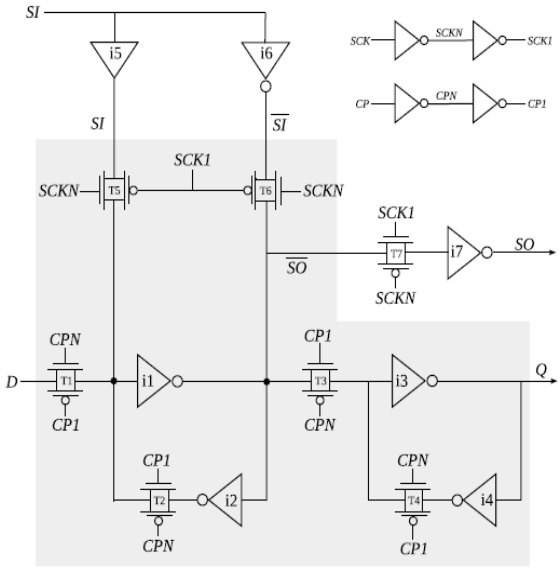


Fig. 3. Proposed scan flip-flop design.

1) Functional Mode: The proposed scan flip-flop works as a regular flip-flop in functional mode. In functional mode, scan clock signal *SCK* is kept at constant logic high (1) level. As long as *SCK* is at constant high (1) level the transmission gate *T*5, and *T*6 remain disabled. This disconnects the test

mode input path from the master structure and the proposed scan flip-flop functions as a regular flip-flop. The scan clock signal (*SCK*) held at constant high (1) level indicates functional mode operation. During the functional mode operation, the transmission gate *T*7 always remains enabled. This keeps the dynamic slave latch always transparent during the functional mode and makes the scan output (*SO*) toggle every time whenever there is a change in master latch's state. However, that is not of any concern as far as the functional mode operation is concerned because the scan output (*SO*) drives only the scan path which feeds the scan input (*SI*) of the successive scan flip-flop. The scan input path remains disconnected from the master structure during the functional mode of operation. The toggling of scan output *SO* will create switching activity in the scan path which also happens in the conventional scan design. Because in case of conventional scan cell the combinational load, as well as the scan path, is driven by the *Q* output of the scan cell. So, in case of conventional scan cell during functional mode, whenever there will be a toggling on the *Q* output, it will propagate in both the combinational logic as well in the scan path. Also, in conventional scan cell, the scan multiplexer which falls in the scan path would dissipate redundant power in both the modes. In functional mode, the master latch of proposed scan cell gets it's input from the functional data input *D*. When clock *CP* is low, the value of functional input *D* propagates into the functional master latch. When *CP* turns to high, the value latched into the master propagates to functional slave latch, and to output *Q* of the scan cell. We verify the said functionality using post-layout simulation.

2) Test Mode: While keeping the functional clock *CP* held at constant high (1) level, consecutive application of scan clock *SCK* makes the proposed scan flip-flop to function in test mode. As the functional clock *CP* is kept high (1), the transmission gate *T*1 always remains disabled in test mode. This disconnects the functional input *D* from the master latch. During test mode, the master latch gets its input from *scan_input SI*. The consecutive application of scan clock *SCK* loads the test values into the scan flip-flops. As it can be observed in Figure 3, when *SCK* gets to logic low (0), *T*5 and *T*6 get enabled, and the value of *SI* is written into the master latch in a similar way to memory write operation.

It should be noted that in test mode since *CP* is always high (1), the feedback path transmission gate *T*2 always remains enabled. This makes the master latch always trying to retain its previous value. However, it can be observed from Figure 3, the test mode input path circuit force writes the *SI* value simultaneously at both input and output nodes of inverter *i*1 via buffer *i*5 and inverter *i*6 respectively. This makes the write operation faster as far as logical fighting is concerned. When the scan clock *SCK* gets high (1), the dynamic slave latch transmission gate *T*7 gets enabled, and the master latch starts driving both dynamic slave latch inverter *i*7, and functional slave latch inverter *i*3. This propagates the test value latched into the master during the negative clock cycle, to dynamic slave latch,

and to *scan_output SO* of the scan cell. When scan clock *SCK* gets to logic low (0), *T*7 gets disabled, and the input parasitic capacitance of inverter *i*7 drives the successive scan cell's *scan_input SI*. Due to the very high impedance of the inverter, the parasitic capacitance does not discharge immediately and takes a long time. The parasitic capacitance discharge time decides the minimum scan clock frequency at which scan shifting can be done. The parasitic capacitance discharge time mainly depends upon two factors: total input capacitance of inverter *i*7, and the charge leakage rate. Hence, for a particular fabrication process technology with well-characterized leakage rate, the discharge time can be optimized by controlling the total input capacitance which in turn depends upon the size of inverter *i*7. The size of inverter *i*7 can be scaled as per the required minimum scan frequency. However, a very low shift frequency is undesirable as it increases the test time, which in turn increases the test cost.

It should be noted that in test mode the transmission gate *T*3 always remains enabled. This keeps the functional slave latch always transparent during test mode and makes the output (*Q*) toggle every time whenever there is a change in master latch's state. Every master latch in scan chain gets its scan input from preceding scan flip-flop's *SO* output, except the very first master latch in the scan chain which gets its test input from a primary input pin. The scan output *SO* of the last flip-flop of the scan chain is connected to a primary output pin. The shifting of test vectors into the scan chain is done using the dynamic slave latch. Once the scan chain is loaded, the test vector is launched via the functional slave latch

5. APPLICATION OF TEST VECTORS

The proposed scan flip-flop allows applying all kind of test vectors that can be applied using a conventional scan flipflop. Before applying any test vectors, scan chain integrity is verified by exercising scan flush test. Scan flush test is applied by propagating an all transition pattern, like 1100, through the scan chain without any response capture cycle in between. The scan clock *SCK* is always kept high during functional mode. When functional clock *CP* is high (1), falling edge on *SCK* switches the circuit from functional mode to test or scan mode. The functional clock *CP* is always kept high (1) during scan shift operation. On arrival of the negative edge of *SCK*, the value of *SI* propagates into master latch via test input path. Next, the rising edge on *SCK* transfers the master latch value to dynamic slave latch and to the scan output node *SO*. By repetitive application of scan clock, the flush patterns are propagated through the scan chain and observed at the primary output pin. The observation of correct input sequence

at primary output pin verifies the integrity of the scan chain or scan path.

Note that for a sequential circuit element like scan cell, the faults are modeled at their inputs and output terminals. In the proposed scan cell, there are separate inputs and outputs for test mode and functional mode which forms the respective scan path and functional path. The scan integrity test covers all possible faults on the scan path which comprises faults of test input *SI*,

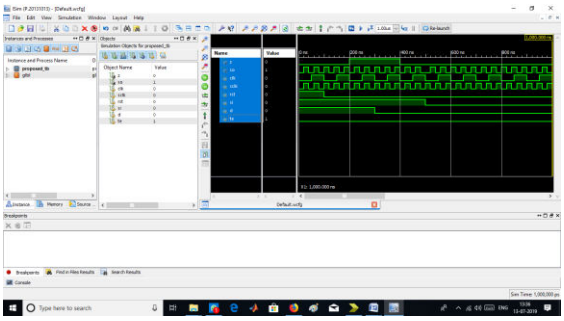
International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

faults of test output *SO*, and faults of the scan path. The scan integrity test does not cover input/output faults of the functional path, i.e., faults of input *D* of the functional master latch and faults of the output *Q* of the functional slave latch. As we will see in the next subsection, these faults are covered during stuck-at fault test application.

A. Stuck-at-Fault Test

When clock *CP* is high (1), falling edge on scan clock *SCK* indicates the start of scan shifting. The *stuck-at-fault* test is applied by first loading the test vector via scan shifting path and then launching the test vector via functional slave latches. As explained earlier the functional slave latch always remains transparent during scan shifting process. So during the last *shift-cum-launch* cycle when negative edge at scan clock *SCK* comes, the test vector is applied via output *Q* of the functional slave latches. It should be noted that the test vector is launched in last shift cycle at the negative edge of the scan clock *SCK*. After the launch of the test vector, the scan clock *SCK* is kept high (1) to disable the scan input path. In order to capture the test response, the functional clock *CP* is clocked once. When the functional clock *CP* gets low, the functional response is latched into the master latch via functional input *D*. On arrival of a positive edge on the functional clock *CP*, the response is propagated to the functional slave latch as well as to the dynamic slave latch. Once the test response is captured, functional clock *CK* is kept at logic high (1) level. This disconnects the functional input *D* from the master latch. Now, falling edge on scan clock *SCK* switches the circuit operation from capture to shift mode. At the same negative edge on *SCK*, functional response stored in the slave latch gets transferred to the functional master latch of next scan cell via the scan input path. The unloading of test response is done with the simultaneous loading of next test vector.

6. SIMULATION RESULT



7. CONCLUSION

We have proposed a scan flip-flop design which eliminates the performance penalty of the serial scan by removing scan multiplexer from the functional path. The new scan flip-flop is capable of applying all conventional tests and fully complies with the conventional industry design and test flow. Furthermore, the proposed scan flip-flop can be used both as a serial scan cell as well as a *RAS* cell, in the mixed mode scan test. The mixed mode scan design implemented with proposed scan flip-flop shows a promising reduction in interconnect wire length, test data volume, and test application time.

BIBLIOGRAPHY

[1] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. New York, NY, USA: Kluwer Acad., 2000.

[2] S. Ahlawat, J. T. Tudu, A. Matrosova, and V. Singh, “A new scan flip flop design to eliminate performance penalty of scan,”

in *Proc. 24th IEEE Asian Test Symp. (ATS)*, Mumbai, India, Nov. 2015, pp. 25–30.

[3] P. Kalla and M. J. Ciesielski, "A comprehensive approach to the partial scan problem using implicit state enumeration," in *Proc. IEEE Int. Test Conf. (ITC)*, Washington, DC, USA, 1998, pp. 651–657.

[4] D. Xiang, S. Venkataraman, W. K. Fuchs, and J. H. Patel, "Partial scan design based on circuit state information," in *Proc. Design Autom. Conf.*, Las Vegas, NV, USA, 1996, pp. 807–812.

[5] V. Boppana and W. K. Fuchs, "Partial scan design based on state transition modeling," in *Proc. Int. Test Conf. (ITC)*, Washington, DC, USA, 1996, pp. 538–547.

[6] D. Xiang and J. H. Patel, "Partial scan design based on circuit state information and functional analysis," *IEEE Trans. Comput.*, vol. 53, no. 3, pp. 276–287, Mar. 2004.

[7] K.-T. Cheng and V. D. Agrawal, "A partial scan method for sequential circuits with feedback," *IEEE Trans. Comput.*, vol. 39, no. 4, pp. 544–548, Apr. 1990.

[8] A. Kunzmann and H.-J. Wunderlich, "An analytical approach to the partial scan problem," *J. Electron. Test. Theory Appl.*, vol. 1, no. 2, pp. 163–174, 1990.

[9] P. Ashar and S. Malik, "Implicit computation of minimum-cost feedback-vertex sets for partial scan and other applications," in *Proc. 31st Design Autom. Conf. (DAC)*, San Diego, CA, USA, 1994, pp. 77–80.

[10] S. T. Chakradhar, A. Balakrishnan, and V. D. Agrawal, "An exact algorithm for selecting partial scan flip-flops," in *Proc. 31st Annu. Design Autom. Conf. (DAC)*, San Diego, CA, USA, 1994, pp. 81–86.

[11] V. D. Agrawal, K.-T. Cheng, D. D. Johnson, and T. S. Lin, "Designing circuits with partial scan," *IEEE Des. Test. Comput.*, vol. 5, no. 2, pp. 8–15, Apr. 1988.

[12] X. Lin, I. Pomeranz, and S. M. Reddy, "Full scan fault coverage with partial scan," in *Proc. Conf. Design Autom. Test Europe (DATE)*, Munich, Germany, 1999, pp. 468–472.

[13] M. S. Hsiao, G. S. Saund, E. M. Rudnick, and J. H. Patel, "Partial scan selection based on dynamic reachability and observability information," in *Proc. 11th Int. Conf. VLSI Design (VLSID)*, Chennai, India, 1998, pp. 174–180.

[14] D. Galbi and L. Basto, "High performance, low power, scannable flip-flop," U.S. Patent 6 348 825, Feb. 19, 2002. [Online]. Available: https://www.google.co.in/patents/US6348825

[15] D. H. Baik, K. K. Saluja, and S. Kajihara, "Random access scan: A solution to test power, test data volume and test time," in *Proc. 17th Int. Conf. VLSI Design*, Mumbai, India, Jan. 2004, pp. 883–888.

[16] D. H. Baik and K. K. Saluja, "Progressive random access scan: A simultaneous solution to test power, test data volume and test time," in *Proc. Int. Test Conf. (ITC)*, Austin, TX, USA, Nov. 2005, p. 10.

[17] D. H. Baik and K. K. Saluja, "Test cost reduction using partitioned grid random access scan," in *Proc. 19th Int. Conf. VLSI Design*, Hyderabad, India, Jan. 2006, pp. 169–174.

[18] A. S. Mudlapur, V. D. Agrawal, and A. D. Singh, "A random access scans

architecture to reduce hardware overhead," in *Proc. Int. Test Conf. (ITC)*, Austin, TX, USA, Nov. 2005, p. 9.