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Paper Authors
K.N.V.R.LAKSHMI, B T MADAV

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DESIGN A CAM ARCHITECTURE BASED ON NOVEL MEMORY ACCESS

[1]K.N.V.R.LAKSHMI, [2]B T MADAV

[1]M.Tech Scholar, Dept of ECE, Malineni Perumallu Educational Society's Group of Institutions, Pulladigunta, Vatticherukur, Prathipadu Road, Guntur, Andhra Pradesh 522017

[2]Associate Professor, Dept of ECE, Malineni Perumallu Educational Society's Group of Institutions, Pulladigunta, Vatticherukur, Prathipadu Road, Guntur, Andhra Pradesh 522017

ABSTRACT: In this paper design a CAM architecture based on novel memory access is implemented. Basically, memory plays very important role in present generation. Earlier instant memory access based on FPGA is introduced. But this will occupy more area and high delay. To overcome this CAM architecture is introduced. Initially, input data is generated from the data generator and address is allotted to that data using address bus. The address bus is divided into two types they are row address and column address. Instruction register is given to the address to perform row and column operation based on instruction command. Both row and column address will transfer data to CAM memory access block to save the data. From this CAM memory access block read and write operations are performed. Hence from proposed system, it can observe that effective results are obtained.

KEY WORDS: CAM (Content Addressable Memory), Address Generation unit, Row Address, Column Address, Instruction Register, Data Generator**.**

I.INTRODUCTION

CAM (Content Addressable Memory)involves a huge segment of a framework on-a-chip (SoC) and has a remarkable commitment to the all out force utilization and region of the SoC. Since region is an Important factor when structuring circuits, memory configuration engineers mean to put however many cells as would be prudent per segment to permit sharing of fringe hardware [1].The regular memory cells are incredibly restricted by their failure to work in longer segments. In most recent couple of years to achieve the superior CMOS gadget, scaling is utilized [2]. Low power circuit operation is a vital metric for the present incorporated circuits.

As compact battery powered electronic devices like small radio devices, cell phones and convenient computers are winding up more mind amazed and common, the interest for expanded battery life requires to search out new innovations and circuit systems that give superior and long operational circumstances. In non-compact applications additionally, lessening power scattering is turning into an important basic issue. Additionally, so as to meet the ongoing execution in computers is complex applications, it is important to have a base event moreover. However, as technology is invariably scaled, spilling currents turn into a noteworthy supporter of the separate power spreading.

A diminishment in power supply voltage is important to lessen dynamic power and stay away from unwavering quality issues in profound sub micron administrations [2]. Voltage scaling goes with supply voltage scaling to keep up the execution, yet it exponentially builds the sub threshold spilling currents. This lessened supply voltage and expanded spilling cause securely and untrustworthy operation of circuits. Thus, in this proposal, an active is made to

outline digital CMOS circuits that have lessened dynamic and spilling power with a worthy deferral and noisy edge. Different power decrease methods are proposed and investigated for their application in three different digital CMOS circuits [3].

The developing interest of compact battery worked frameworks has made strong skilled processors a need. For applications like suitable figuring active productivity takes top generally need. These inserted frameworks need continued charging of their batteries. The issue is gradually extreme in the remote sensor systems which are sent for checking the natural parameters [4].

Memory structures have become inseparable piece of current VLSI frameworks. Semiconductor memory is directly simply remaining solitary memory chip as well as a vital piece of complex VLSI frameworks. The dominating model for streamlining is regularly to press in however much as memory as could reasonably be expected in a given region. This pattern toward compact figuring has prompted power issues in memory .The pattern of scaling of gadget sizes, low limit voltage, and ultra-slim gate oxide have progressively been tested by fluctuation, and along these lines, by dependability related issues [5].

CAM's effect has gotten particularly significant because of the rise of battery fueled convenient gadgets and low force sensor applications. Most CAM plan exertion has been directed to encourage voltage scaling and improving yield. The traditionally actualized six transistor (7T) cell in CAM s permits high thickness, bit-interleaving and quick differential detecting however experiences half-select security, read-upset dependability, and clashing peruse and compose measuring. Past endeavors to unravel these issues have incorporated the usage of help methods, novel cell structure, engineering enhancements, or innovative turns of events Most CAM s are developed using multi VDD biasing to achieve low power consumptions and low delays with the use of Voltage level shifters.

II.LITERATURE SURVEY

"Reducing Power in Content-Addressable Memory by pseudo nMOS Cell" [1]

Content address memory a huge bulk of power is broadly distribute charge and recharging utmost of this game follow on utmost course. That new small power content address memory cell along a individual bit edge architecture act scheduled via break this difference capability of the cam design. This scheduled content address memory cell can break almost half of huge co-actions filling and the ordinarily convert about two reciprocal bus lines follows. The content address memory conversation route architecture is fixed pseudo N metal oxide semiconductor sense framework along a preoccupation way is recycled to forcefully bypass the ordinarily convert in same lines. The content address memory arrangement is situated on complementary metal-oxide semiconductor action among 2.5Volts power supply voltage. The capability utilization of this scheduled content address memory is 16.38mW bottom 300mhz operations.

"Performance Evaluation of Content Addressable Memories" [2]

Content addressable memories are used in high speed searching applications. There are more applications for Ternary Content Addressable Memories (TCAM) than Binary Content Addressable Memories (BiCAM).For higher search speed applications, NOR type match line CAMs

are useful. The NOR type match line CAM requires high power, therefore, the reduction of its power consumption is the subject of many reported designs. Here, comparison of NOR type match line BiCAM and TCAM is done in terms of power and area. The BiCAM power consumption is 20% less than the TCAM. Simulations performed with cadence 45-nm technology.

"Deep and Narrow Binary Content-Addressable Memories using FPGA-based BRAMs" [3]

Binary Content Addressable Memories (BCAM's) are massively parallel search engines capable of searching the entire memory space in a single clock cycle. BCAMs are used in a wide range of applications, such as memory management, networks, data compression, DSP (Digital Signal Processing), and databases. Due to the increasing amount of processed information, modern BCAM applications demand a deep searching space. However, traditional BCAM approaches in FPGAs suffer from storage inefficiency. In this paper, a novel and efficient technique for constructing deep and narrow BCAMs out of standard SRAM (Static Random Access Memory) blocks in FPGAs is proposed. This technique is most efficient for deep and narrow CAMs since the BRAM (Binary Coded Random Access Memory) consumption is exponential to pattern width. Using Altera's Stratix V device, traditional methods achieve up to 64K BCAM, while the proposed technique achieves up to 4M entries. For the 64K test-case, traditional methods consume 43 times more ALMs and achieves only one-third of the Fmax. A fully parameterized Verilog implementation is available. This implementation has been extensively tested using Altera's tools.

"Low Cost Ternary Content Addressable Memory Based on Early Termination Precharge Scheme" [4]

In this paper, early termination matchline (ML) precharge scheme for low power and high speed ternary content addressable memory (TCAM) is given. In the proposed TCAM, by employing the pre-decision based early termination, unnecessary ML precharging has been effectively eliminated while improving the search speed and achieving error-free operation. The reference voltage generator used to implement the proposed early termination approach can be simply designed using dummy row without large area overhead. According to the post-layout simulations with the 65nm CMOS process, the introduced early termination ML precharge scheme shows up to 30.4% of sensing delay improvement and 65.9% of ML power savings compared to the conventional approach. It also shows 8% of FOM (energy/bit/search) improvement compared to state-of-the-art works.

"Low Cost Ternary Content Addressable Memory Using Adaptive Matchline Discharging Scheme" [5]

This paper presents an adaptive Match-Line (ML) discharging scheme for low power and high speed ternary content addressable memory (TCAM). In the proposed TCAM, by employing the gated ML pull down path and ML boosting scheme, the redundant ML discharging and SL (Switch Line) switching are eliminated while improving the search speed. By considering the number of mismatch and ML discharging speed, the ML discharging is adaptively controlled in the proposed TCAM. The simulation results with the 65nm CMOS technology show that the proposed adaptive ML discharging scheme improves up to 19% of sensing delay and saves 81% of ML power compared to the

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conventional approach. When compared with the state-of-the-art work, the post-layout simulations show 10% improvement of FOM (energy/bit/search).

III.PROPOSED SYSTEM

The below figure (1) shows the block diagram of proposed system. Initially, input data is generated from the data generator and address is allotted to that data using address bus. The address bus is divided into two types they are row address and column address. Instruction register is given to the address to perform row and column operation based on instruction command. Both row and column address will transfer data to CMA memory access block to save the data. From this CAM memory access block read and write operations are performed. All these data will be saved in the FPGA memory and it is implemented in Xilinx ISE software tool.

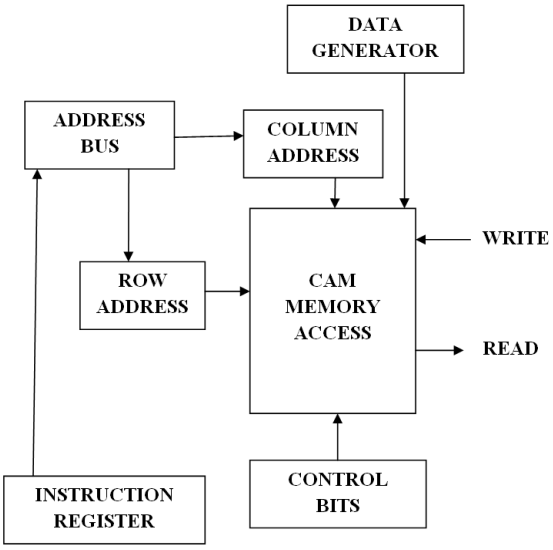

Fig. 1: BLOCK DIAGRAM OF PROPOSED SYSTEM

Instruction register (IR) or current instruction register (CIR) is the part of a CPU's control unit that holds the instruction currently being executed or decoded. Modern processors can even do some of the steps out of order as decoding on several instructions is done in parallel.

An instruction register holds a machine instruction that is currently being executed. A variety of registers serve different functions in a central processing unit (CPU) – the function of the instruction register is to hold that currently queued instruction for use.

The address generation unit (AGU), sometimes also called address computation unit (ACU), is an execution unit inside central processing units (CPUs) that calculates addresses used by the CPU to access main memory. By having address calculations handled by separate circuitry that operates in parallel with the rest of the CPU, the number of CPU cycles required for executing various machine instructions can be reduced, bringing performance improvements.

Some of the complicated processors use a pipeline of instruction registers where each stage of the pipeline does part of the decoding, preparation or execution and then passes it to the next stage for its step. Modern processors can even do some of the steps out of order as decoding on several instructions is done in parallel.

Decoding the op-code in the instruction register includes determining the instruction, determining where its operands are in memory, retrieving the operands from memory, allocating processor resources to execute the command (in super scalar processors), etc.

The output of the IR is available to control circuits, which generate the timing signals that control the various processing elements involved in executing the instruction. In the instruction cycle, the instruction is

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loaded into the instruction register after the processor fetches it from the memory location pointed to by the program counter.

IV. RESULTS

The below figure (2) shows the RTL schematic of proposed system.

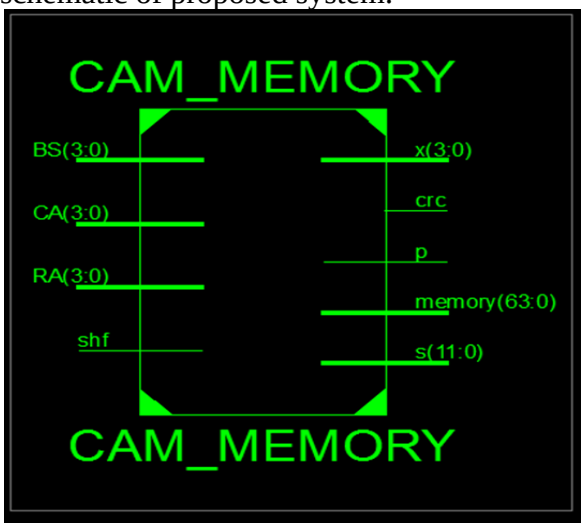

Fig. 2: RTL SCHEMATIC

The below figure (3) shows the technology schematic of proposed system. It is the combination of look up tables, truth tables and K-Map.

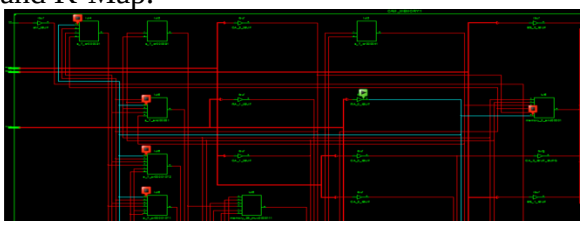

Fig. 3: TECHNOLOGY SCHEMATIC

The below figure (4) shows the output waveform of proposed system.

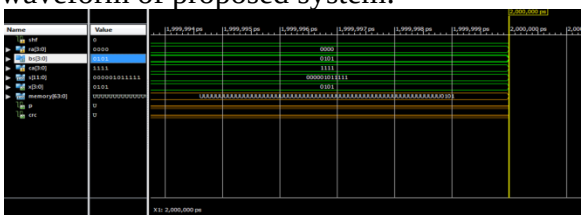

Fig. 4: OUTPUT WAVEFORM

V. CONCLUSION

In this paper design a CAM architecture based on novel memory access is implemented. The main intent of this system is to reduce the delay and area. Address generation unit will generate the row address and column address. According to this row accelerators and column accelerators are generated from blocks. All these data will be saved in the FPGA memory and it is implemented in Xilinx ISE software tool. From results, it can observe that this project gives effective output in terms of delay and memory.

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K.N.V.R.LAKSHMI completed B.Tech from B.V.C. Engineering College and pursuing M.Tech from Malineni Perumallu Educational Society's Group of Institutions, Pulladigunta, Vatticherukur, Prathipadu Road, Guntur, and Andhra Pradesh 522017. Her M.Tech specialization is VLSI.

B T MADAV completed B.Tech from IETE and M.Tech from JNTUK. At present he is working as associate professor at Malineni Perumallu Educational Society's Group of Institutions, Pulladigunta, Vatticherukur, Prathipadu Road, Guntur, and Andhra Pradesh 522017. His area of interest is computer vision and VLSI design. .