International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

ELSEVIER SSRN

IJIEMR Transactions, online available on 8th Apr 2020. Link
:http://www.ijiemr.org/downloads.php?vol=Volume-09&issue=ISSUE-04

Title: A LOW POWER DUAL MODE DATA CONVERTER FOR MIXED SIGNAL CIRCUIT TESTING
Volume 09, Issue 04, Pages: 41-46.

Paper Authors

P. RAMAKRISHNA, C. PRANITHA, M. SWATHI

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

A LOW POWER DUAL MODE DATA CONVERTER FOR MIXED SIGNAL CIRCUIT TESTING

P. RAMAKRISHNA[1], C. PRANITHA[2], M. SWATHI[3]

[1]Associate professor, Department of Electronics and Communication Engineering, Anurag Group of Institutions, Hyderabad, India.

[2]P.G. Scholar, Department of Electronics and Communication Engineering, Anurag Group of Institutions, Hyderabad, India.

[3]Assistant professor, Department of Electronics and Communication Engineering, Vignan Bharathi Institute of Technology, Hyderabad, India.

[1]prk.cvsr@gmail.com.

Abstract

The design of a low power 12-bit 100MS/s Dual-Mode Data Converter (DMDC) is presented in this paper. DMDC can be contained analog-digital and digital-analog converters with different resolutions and speeds for testing mixed type of signal circuits. It has been used in built-in self-test or mixed signal boundary scans. This work is implemented in 0.18um using Verilog-A with a 1V power supply. It ranges from 10kHz to 50MHz. It evinces 72.39 SNR and consuming power 56.62uW with a 10MHz input signal, at 100MS/s.

Keywords—Pipelined ADC; R-2R DAC; MDAC; Verilog-A

I. Introduction

Recently, system-on-chip (SOC) packaging system allows integrating several components on a single chip for different kind of applications. These components can be memory, CPU, analog, digital and mixed etc. However, SOC packaging system faced different challenges with mixed signal processing at production stage. A major concern is mixed-signal testing, but not the only one. It is also important to achieve great accuracy in the modeling of mixed-signal designs. In addition, another key issue is to integrate analog and digital components into one program, with better performance as the prominent objective. Therefore, it is essential to speed up the system with accurate model and design simulations.

Latterly, multiple design-for-test (DFT) techniques have been proposed for mixed signal systems [1]. The key component of the system is having a high-speed, resolution. Pipelined ADC is the ideal choice between speed and resolution. The pipeline ADCs have been able to achieve a resolution of 8-10 bits and a speed of 60-80MS /s in recent years.In this paper, we demonstrated DMDC of a 12-bit 100MS/s for low power applications. A Dual-Mode Data Converter can be used to convert both analog-to-digital converter (ADC) and digital-to-analog converter (DAC). To reduce the power consumption and size of chip, MDAC has been used. However, mixed-signal systems may contain either ADCs or DACs but not both. Moreover, for high-speed and better accuracy

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

applications, the conversion rate and accuracy of the ADCs and DACs must be high. Therefore, Dual-mode Data Converter with high-speed DFT building block is used in this paper. One of the best features of the DMDC is allow the user to select either ADC or DAC combinations for their desired utility.

The following article is organized. The Data Converter architecture is outlined in Section II. The design features of the data converter are defined in Section III. In section IV, the results calculated are summarized. Section V concludes this paper.

II. Data Converter

Figure 1, shows the general structure of the proposed dual-mode data converter (DMDC). It consists of a series of similar conversion stages (CSs) and an ICN network interconnection. Each CS in the amplifier stage containing a k-bit flash ADCs and DACs. The input of amplifier and ADC can be controlled by the multiplexer operated by S. The role of CS is specified by the signal Fi. The CS is configured as a pipelined stage of the ADC when Fi is set to 1 and the conversion stage (CS) is configured as a digital-to-analog converter (DAC) stage when Fi is set to 0.

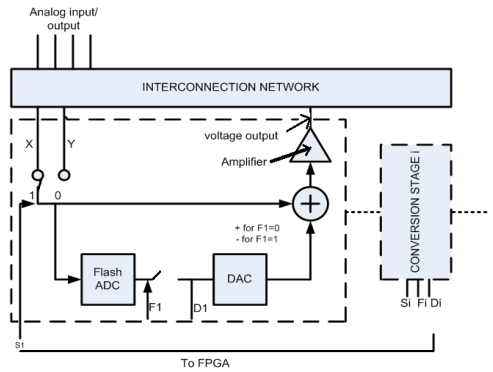


Figure 1: Block Diagram of Data Converter

Figure 2 demonstrates the configuration of an ICN for an ADC with 10 CSs. The ICN makes it possible to link the CSs to various groups. It also allows the CSs outputs to be fed to other CSs as inputs. Different data converters with different resolutions may be reconfigured using different ICN links. The delay between css is reduced significantly, as the number of switches between the two terminals is equal to one and it is possible to achieve high-speed operations. The ICN's area requirement is usually very small as there are just a few paths to link a cable.

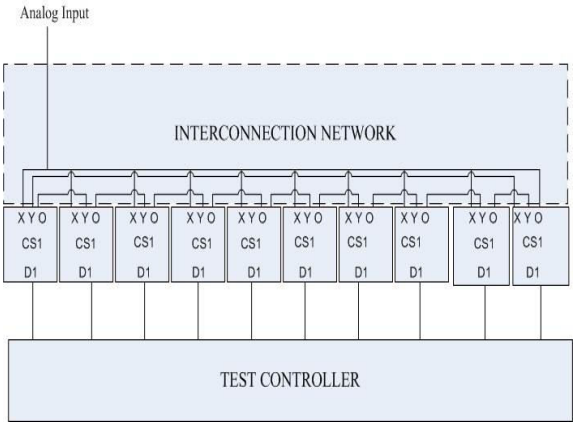


Figure 2: An ADC of 12 bits attained in a DC with 10 CSs

The first stage of the conversion stage serves as a sample and hold circuit and all remaining stages will be configured as ADC stages. The analog input is provided to the A terminal and o is connected to the B terminal in the next stage. By using the pipelined structure, if there are m clock periods, only 1 sample/clock period will be required to complete one sample

III. Design details of the DMDC

The analog input is given to the first stage of the ADC. In the 1-bit ADC, the operation is performed by the sub-blocks. The sample and hold output is given to the comparator and compares with the reference signal and delivers the output.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

The comparator output is considered to be the digital output. In the MDAC circuit, another input signal is used and another input from the comparator output. The output is either DAC or ADC based on the switching network. If Fi is 1, the output is configured as Pipelined ADC and if Fi is 0 then the output is configured as R-2R DAC.

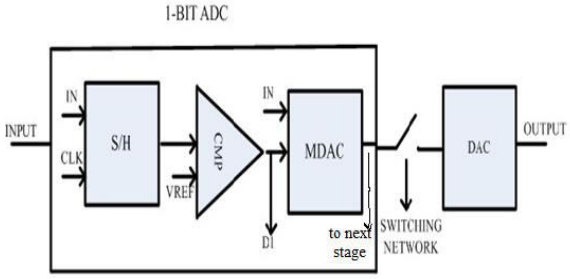


Figure 3: Proposed design of DMDC

In this Pipelined ADC, we only use sample and hold (s &h), comparator and MDAC as shown in figure 3. The threshold voltage Vth is 0.5V. We write Verilog-A code for each block, from which we create schematic and execute and test simulation results. A sample and hold (S&H) circuit is a simple framework used to get the voltage of an always-changing analog signal and to hold its incentive at a steady level for a while.

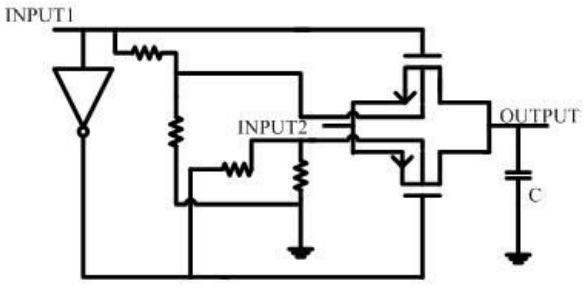


Figure 4: Switch diagram

The transmission gate can be used as a switch. Here a low-power technique called Dynamic Threshold Metal Oxide Semiconductor Logic (DTMOS) is applied to the switch in order to reduce the power consumption. The threshold voltage is dynamically altered in dynamic threshold CMOS (DTMOS) to match the circuit's operating state. Dynamic threshold CMOS can be achieved by tying the gate and body together.

Approach to Verilog-A, analog simulation environment, and Verilog-AMS (Wreal) approach with System Verilog.

A. Verilog-A

The basic idea behind to use Verilog-A is a standard language modeling of analog circuits. This solution is a Verilog-AMS constant-time sub-set [6]. Verilog-A helps to SPICE simulator users to build analog modules for their simulations. However, the simulation of SPICE is slower compared to Verilog-A. Within Verilog-A, nodes and branches are used to assemble components. The node-branch relationship is defined by the laws of Kirchhoff. A linear resistor with two-terminals example is illustrated using double nodes (also known as pins or ports).

```
module resistor (node1,node2);
electrical node1,node2;
parameter real r=1;
branch (node1,node2) res;
analog V(res)<+ r*i(res);
endmodule
```

B. Verilog-AMS with Wreal

Verilog-AMS has a versatile capability to import both analog and mixed-signal modeling. It helps to understand the behavior of analog and mixed-signal circuit (AMS). It also includes continuous time modeling and even driven concepts for making ideal behavior of both analog and mixed signal devices. In Verilog-AMS, all interactive sphere procedures and statements function like in Verilog.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

Also, all the analog domain components work as in Verilog-A. An example of a sample and hold is illustrated below.

```
module sh(out,in,clk);
input in,clk;
output out;
electrical in;
wreal out;
real sampled;
always @(posedge clk)
out=V(in);
assign out=sampled;
endmodule
```

A comparator delivers voltage based output signal when one signal level to another or predefined reference voltage (V_{ref}). An MDAC is connected to a pipeline ADC through a comparator. It samples an input signal in the sampling phase and performs subtraction or multiplication operations in the amplification phase based on the reference voltage. The MDAC output is connected as an input to the next stage pipeline ADC. 2-bit flash ADC is used at the last stage of the ADC pipeline. Flash type ADC is based on the principle of comparing the analog input voltage with the reference voltage set. It is the fastest type of ADC because the conversion is carried out simultaneously via a set of comparators.

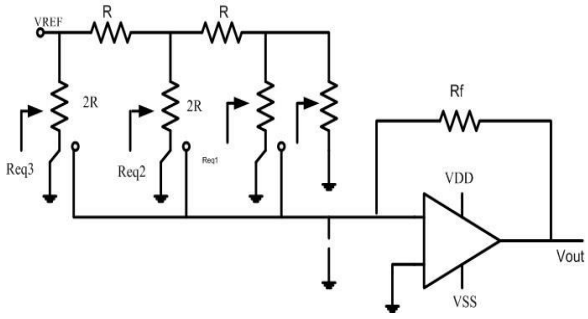
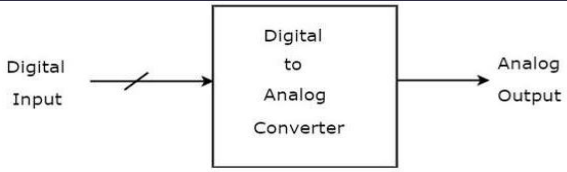


Figure 4: (a) Block diagram of R-2R Ladder DAC



(b) Block diagram of DAC

An important element of any mixed-signal circuit is the digital to analog converters (DACs). A fast, accurate and relatively inexpensive way to create analog voltages from digital values is the DAC-based R-2R ladder. DAC changes to analog voltage via a parallel digital input. Only two resistor values R and 2R are required. Resolution is the output voltage variation for each LSB change in the digital input. The DAC performance estimation is achieved by various error types. They are DNL, INL, Gain error, Offset error, and Non-Monotonicity.

- DNL is the difference between the actual height of the step and the ideal 1LSB value. Therefore, if a DAC's step height is 1LSB, then DNL is zero. If DNL exceeds 1 LSB, the converter may not be monotonic.
- Gain error is the difference between the ideal curve slope and the real DAC performance.
- INL is the divergence of the actual transfer function from an ideal transfer function.
- Offset error is the constant difference in voltage between the actual output and the ideal DAC output.

Table I: 1-bit conversion stage configurations

Fi	Configuration
1	ADC stage
0	DAC stage

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

IV. Measured results

The DMDC prototype was fabricated in a mixed-signal CMOS process of 0.18um. The total power consumption is 56.62uW with a power supply of 1V. Cadence Virtuoso tool is used to simulate pipelined ADC and R-2R DAC. The simulation results are shown in figure 5, 6.

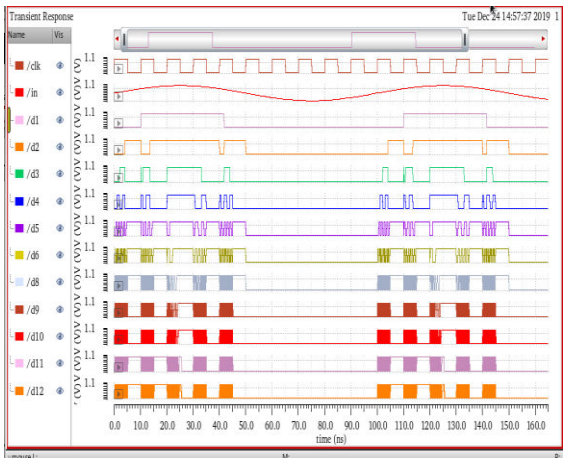


Figure 5: Simulation result of 12-bit Pipelined Analog-to-digital Converter

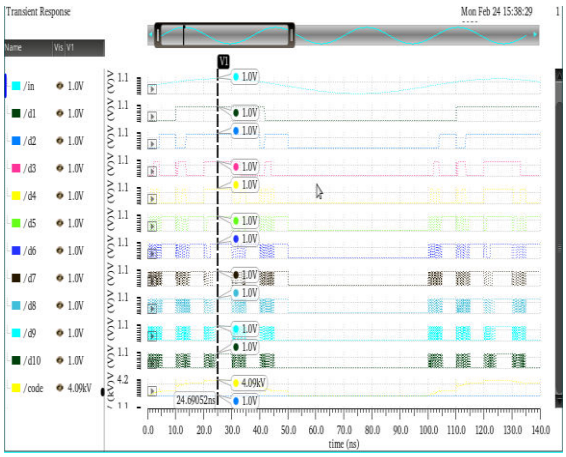


Figure 6: Simulation result of 12-bit R-2R ladder Digital-to-analog Converter

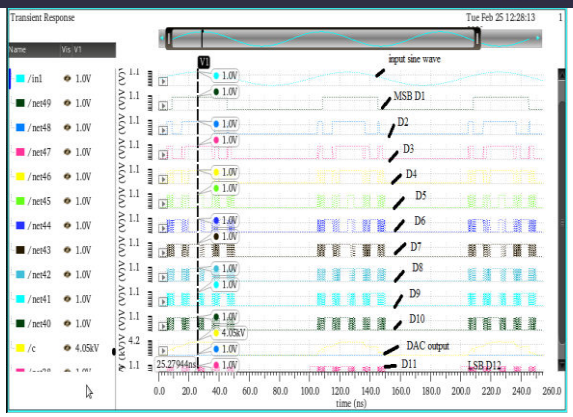


Figure 7: Simulation result of overall proposed design of DMDC

The DAC's differential nonlinearity (DNL) and integral nonlinearity (INL) were computed using the code density test method. The measured SNR is 72.39dB with an effective bit number (ENOB) of 11.73.

Table II: Comparison of measured performance with the existing paper.

	Base paper	**In this work**
Supply voltage(V)	1.8	1
Resolution(bits)	8	12
SNR(dB)	74.4	72.39
Sampling rate	80MS/s	100MS/s
Power consumption(W)	75u	56.62u

V. Conclusion

This paper introduces a 12-bit 100MS/s dual-mode data converter with low power dissipation. Through applying the DTMOS technique to the design, we achieved low power consumption. The results measured shows that ADC's ENOB reaches 11.73bits. The area overhead is also reduced.

References

[1]Ramana Aisola et al., "Verilog-A Language Reference Manual", Open Verilog International, 1996.

[2] Edward K.F.Lee, "Reconfigurable Data Converter as a Building Block for Mixed-Signal Test", March-17 1997 IEEE.

[3]Ron Vogelsong, Ahmed Hussein Osman, Moustafa Mohamed, "Practical RNM with SystemVerilog", CDNLive 2015, 2015.

[4] Long Yang, Zongmin Wang, Liang Zhou, Wenxiao Feng, "A Low Power Pipelined ADC with Improved MDAC", CoDIT'16-April6-8, 2016.

[5] Cadence Design Systems, "Verilog-AMS Real Valued Modeling Guide", 2015

[6] Kenneth S. Cundert and Olaf Zinke, "The Designer's Guide to Verilog AMS", Kluwer Academic Publishers, 2004.

[7] Van den Bosch, A. et al, A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter , IEEE Journal of Solid State Circuits, Vol. 36, pp. 315-324, 2001.

[8] Nikolaos Georgoulopoulos, Alkiviadis Hatzopoulos, "Real Number Modeling of a Flash-ADC using SystemVerilog", PACET 2017.

[9] Payal Jangra, Rekha Yadav, "Design of 12-bit DAC using CMOS Technology", Volume 5 issue VI, June 2017.

[10] M.Ohletz. "Hybrid Built-In Self Test (HBIST) for Mixed Analog/Digital Integrated Circuits". European Test Conf.,p.22.4.1-4, 89.

[11] Razavi, B., Principles of Data Conversion System Design, IEEE Press, 1995.

[12] Digital to Analog Conversion The R-2R DAC, Alan Wolke, May 2013.

[13] D.Johns and Ken Martin- Analog Integrated Circuit Design, Wiley India Pvt.Ltd, 1997.

[14] A. M. Abo, P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipelined analog-to-digital converter," *IEEE J. Solid State Circuits*, vol. 34, no. 5,
pp. 599-606, May 1999.

[15] A. Van den Bosch and M. Borremans et al., "A 12-bit 200-MHz low glitch CMOS D/A converter," in IEEE 1998 Custom Integrated Circuits Conf (CICC), May 1998, pp. 249–252.

[16] S. Chin and C. Wu, "A 10-b 125-MHz CMOS digital-to-analog converter with threshold-voltage compensated current sources," IEEE J. Solid-State Circuits, vol. 29, pp. 1374–1380, Nov. 1994.