International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

ELSEVIER
SSRN

IJIEMR Transactions, online available on 5th Feb 2020. Link
:http://www.ijiemr.org/downloads.php?vol=Volume-09&issue=ISSUE-02

Title: AN APPROACH TO PHYSICAL DESIGN OF 28NM TECHNOLOGY BASED PROCESSOR CHIP USING IC COMPLIER TOOL
Volume 09, Issue 02, Pages: 1-5.

Paper Authors

T GANGADHAR, Dr V ADINARAYANA REDDY
SVIST, Ramarajupalli, Kadapa, AP, India

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

AN APPROACH TO PHYSICAL DESIGN OF 28NM TECHNOLOGY BASED PROCESSOR CHIP USING IC COMPLIER TOOL

T GANGADHAR[1], Dr V ADINARAYANA REDDY[2]

[1]MTech student, Dept of ECE, SVIST, Ramarajupalli, Kadapa, AP, India.

[2]Professor, Dept of ECE, SVIST, Ramarajupalli, Kadapa, AP, India.

ABSTRACT:

With the advancement of modern technology the world has come into System-On-Chip (SOC) based automation systems. Modern technology has abandoned analog bulky system occupying large areas. Based on CMOS logic, technology is growing but at the same time area, cost, power and efficiency trade-off of the system has become more concerned matter. In 2008, when transistor based processor become commercially available, it has become more commonplace for semiconductor fabrication through generation of 65nm processes. Each and every system has limitations. Now-a-days works are progressing on 5 nm technology. The sheer purpose of this project is to develop a design of chip using 28nm library of MOSFET semiconductors using physical design flow technique. Here 28nm refers to channel-length of gate of MOSFET. All the physical design has been simulated on IC Compiler tool, founded by Synopsys. The project has been demonstrated as a single voltage and single row with double spacing of macros. But it can also be demonstrated as Multi Voltage with double row single spacing, which can deem as cost beneficiary. Large fabrication companies use Si02 dies for fabrication. Physical design uses technology library such as 60nm, 45nm, 28nm etc which are actually provided by most fabrication houses according to their requirement.

***Keywords*: MOSFET, Semiconductor devices, Sio2, 28nm, multi voltage.**

1. INTRODUCTION:

Semiconductor is usually a chemical compound element conducts electricity for few rules, thus making it for controlling of current. There is a difference in substances between conductors and insulators. Semiconductors has intermediate sized band gap that actually acts as insulators in absolute temperature (-273 K). Obviously, Insulators are materials which have large band gap. Conductors are having the overlapped, the valence and conduction bands, so they may not have a band gap. Semiconductors have band gap of 1. Elements of group IV, as – Silicon (Si), Germanium (Ge), and Gallium Arsenide (GaAs) are used as semiconductors. Some compounds of these are also used as semiconductors. Semiconductors are made up of covalent bonds. Making crystalline structure, semiconductors need 4 valence

electrons for each valence electron. This bond called covalent bond. This document is a template. An electronic copy can be downloaded from the conference website. For questions on paper guidelines, please contact the conference publications committee as indicated on the conference website. Information about final paper submission is available from the conference website. The thesis here is a study on the ASIC flow and we worked on the physical design aspect of the flow and hence a comprehensive work on the physical designing of the subsystem torpedo. This thesis basically studies the physical design implementation of torpedo processor which incorporates 32 macros in overall and 43000 cell instances .We had 5 clocks ,3 propagated and 2 generated clock in a die size of 5.9 mm square which operated at a frequency of 400 megahertz having a supply voltage of 1.8 volts. Manuscript received February 2014. Tauseef Amin Azmi. VLSI Research Academy, RV-VLSI Design Centre Jayanagar 4th block Bangalore, Karnataka, India. The technology which we worked was 180 nm technology and working on the IC Compiler tool from synopsys and then moving on to static timing analysis part on the Prime time tool from synopsys and then further moving on to drc/lvs checking on the tool Calibre from mentor graphics. The foundry which supplied us the 180 nm technology documents was Jazz semiconductors INC. The earlier work on this project that were carried out were at different scenarios and hence the results were with different optimization, here in our study we had made a comprehensive and mature step to achieve the maximum optimization of the placement of the standard cells and therefore in our effort we had chosen the three scenarios for our thesis which were three operating conditions: function minimum, function maximum, CTS maximum. The temperature that we worked on the physical design implementation of this block level subsystem were -40 degree celcius , 25 degree celcius ,125 degree celcius. The three scenarios supply voltages were 1.65 volts, 1.8 volts and 1.9 volts respectively and the power dissipation was 300 milli watts with pre cts derate of 15 % and post cts derate of also 15% respectively.

2. RELATED STUDY:

In the designing of integrated circuits, Physical Design Flow is mostly used tools. It is a step which comes after circuit design in the cycle of standard circuit design. Divine goal of physical design flow is to create a correct geometric representation of circuit component such as devices, logic gates, inverter, multiplexer, interconnects in a shape according to specified requirements and become ready for manufacturing in corresponding layers of materials. After manufacturing it should make sure the working of the component. It is often termed as layout. Physical design has steps and sub-steps. Some steps include designing, some steps work for verification of designing and rest are used for affirmation of layout design. It has three (03) major categories namely: Front-End designing using

Hardware Description Language, Physical Verification and Back-End Design. After proper plan of circuit layout next step is or manufacturing which is conducted by some photo-lithographic process and sometimes in hand with very care in wafer fabrication houses.

3. METHODOLOGY:

"At the 28nm node, static power is a very significant portion of the total power dissipation of a device and in some cases is the dominate factor. To achieve maximal power efficiency, the choice of process technology is paramount because the key to enabling greater useable system performance and capabilities is controlling power consumption," said Victor Peng, senior vice president, Programmable Platforms Development as Xilinx. "We chose the high-k metal gate (HKMG) high-performance, low-power process at TSMC and Samsung Foundry for next-generation FPGAs to significantly minimize static power consumption so we wouldn't lose the performance and functional advantages we get at 28nm." Power consumption was a global concern and a driven factor within past decades for integrated circuits industry. IC's power consumption is a series factor in the IC design and the operating system. Eliminating access heat, created by ICs and other semiconductors components, directly impacting the entire system's cost due to the usage of cooling fans, heat sinks and other overall temperature regulators. Power has to be carefully designed for device operation and cooling purposes. One of the most critical issues rose due to access heat was the system's reliability. Systems suffered from overheat downtime and high maintenance cost. The great success of semiconductor industry has been driven by the advancement in transistor technology. The industry could improve the performance of their products by shrinking the transistor dimension, integrating more transistors, significantly reducing manufacturing cost. However, static power consumption has unavoidably offset the cost savings with each manufacturing process reduction. This phenomenon is particularly effects the FPGAs world where modern processes are used in orders to provide high performance at low cost. Systems designed with FPGAs benefit from significant improvements over ASICS, such as rapid-process technology scaling and design innovation, which permit the use of FPGAs in high availability, high-reliability, and safety-critical systems. Yet, IC's designers can't take complete advantage of deep nano meter processes due to the limitations of static power consumption. In very low processes static power actually exceeds dynamic power in some cases. The solution especially in 28nm node and below is to efficiently manage dynamic power within the entire chip's power budget. Reducing static power consumption allocates more of the power budget for dynamic power, resulting in more functional performance. This method facilitates higher bandwidth interfaces and greater resources for advanced functionality circuits like memories, DSPs and other logic IPs on FPGAs. Efficient management of

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

both dynamic power (Active) and the growing static power (Leakage) is a key factor to a successful design's in 28nm node and below. Wiser utilization of the IC's power budget results higher performance and maintaining the process low cost benefit.

4. EXPERIMENTAL ANALYSIS:

Check net list

It shows results for certain problems such as input ports unloaded or un-driven output ports, nets free of loads or drivers or having multiple drivers, cells or designs that does not have any inputs or outputs, pin counts that are not matched between its reference and an instances, hierarchical wire loops and so forth.

Check library Syntax:

Check library It provides information of consistency between physical and logical libraries. Other important sanity checks are

• I/O Placement,

• report qor

This command reports:

♣ Timing path group

♣ Count details of cell

♣ Combinational and non-combinational statistics of current design

♣ Total area

♣ Static power report

♣ DRV- Design Rule Violation

♣ Timing details of compilation.

After so many iterations of VT Swapping, Cell Sizing and so many buffers adding, I haven't got any Setup and Hold Violation in my design as well as I'm successful to meet and fix all the DRC Violations.

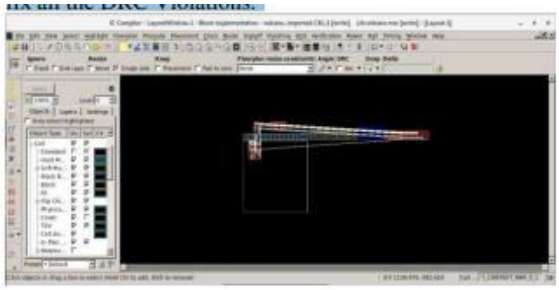

Fig.4.1. Started Dragging Macros For Macros Placement After Setting Colors.

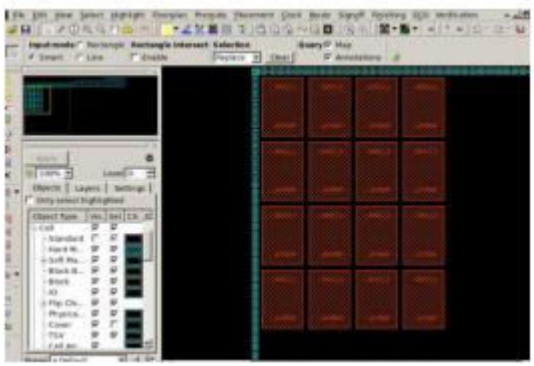

Fig.4.2. Macros Placement.

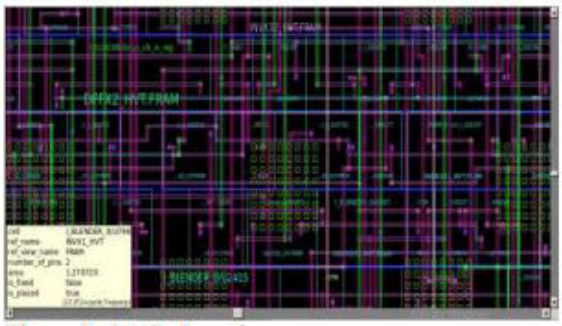

Fig.4.3. Detailed routing.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

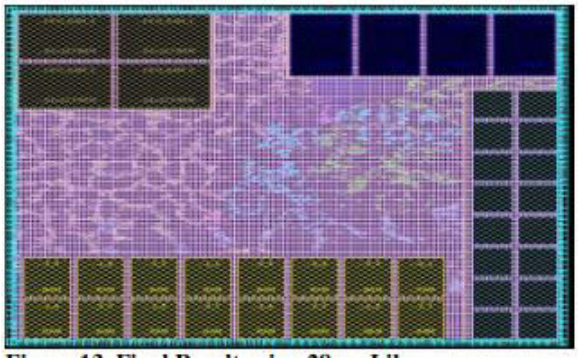

Fig.4.4. Final Result using 28nm Library.

5. CONCLUSION:

As VLSI, especially PD (Physical Design) domain is a great Research and Development field and as my design hasn't any DRC Violations as well as hasn't any Setup and Hold Violations so this design can be great in future.

REFERENCES:

1) Naveed sherwani ,a dissertation submitted at the summit of open silicon December1999 .

2) Venkatesh Prasad and Srinath b k a design for the issues in the torpedo processor ,RV VLSI design centre Bangalore year 2007 bangalore India .

3) S.Chien, S.Ma and L.Chen, "Efficient Moving Object Segmentation Algorithm Using Background Registration Technique", IEEE transcript on circuits and systems, July 2002.

4) J.Moon, D.Kim and R.Park, "Video Matting Based on Background Estimation", Enformatic Transactions on Engineering, December 2004.

5) R.C. Gonzalea and R.E. Woods, Digital Image Processing (2nd Edition), Prentice Hall, 2002.

6) Andreas Koschan and Mongi Abidi, "Comparison of Median Filter Techniques for Noise Removal in Color Images", Imaging Robotics and Intelligent Systems Laboratory, The University of Tennessee, Knoxville.

7) Abdessamad Ben Hamza, "Removing Noise and Preserving Details with Relaxed Median Filters", Dept. de Fiscia Aplicada, Universidad de Granada, Spain, 2009.

8) Pawan Patidar, Manoj Gupta and Sumit Srivastava, "Image De – Noising by Various Filters for Different Noise", International Journal of Computer Application, November 2010.

9) D.Maheswari and Dr. V.Radha, "Noise Removal in Compound Image Using Median Filter", International Journal on Computer Science and Engineering, 2010.