International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

IJIEMR Transactions, online available on 11th Dec 2019. Link :http://www.ijiemr.org/downloads.php?vol=Volume-08&issue=ISSUE-11

Title **MAKING USE OF ADDITION PLANS FOR THE RENOVATION OF MAXIMIZED RADIX-2 AND RADIX-4 FFT BUTTERFLIES**

Volume 08, Issue 12, Pages: 58–63.

Paper Authors

T.R. KAMESWARA RAO , MR. P. NAGARAJA KUMAR , MR. K. NIRANJAN REDDY

CMR Institute of Technology, Kondlakoya , Hyderabad , Telangana , India

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
www.ijiemr.org

MAKING USE OF ADDITION PLANS FOR THE RENOVATION OF MAXIMIZED RADIX-2 AND RADIX-4 FFT BUTTERFLIES

[1]T.R. KAMESWARA RAO , [2]MR. P. NAGARAJA KUMAR , [3]MR. K. NIRANJAN REDDY

[1]PG Scholar, Department of ECE, CMR Institute of Technology, Kondlakoya , Hyderabad , Telangana , India

[2]Assistant Professor, Department of ECE, CMR Institute of Technology, Kondlakoya , Hyderabad , Telangana , India

[3]Professor, Department of ECE, CMR Institute of Technology, Kondlakoya , Hyderabad , Telangana , India.

ABSTRACT:

Optimized butterflies used to calculate the complex terms, Power reduction in FFT architecture. In this paper we exploit different addition schemes in order to improve the efficiency of 16 bit width radix-2 and radix-4 FFT butterflies. Combinations of simultaneous addition of three and seven operands are inserted in the structures of the butterflies in order to produce power efficient structures. It involves additions schemes like Carry Save Adder (CSA), adder compressors. The radix-2, radix-4 butterflies are implemented in HDL, Synthesized 45 nm Nan gate Using Cadence RTL Complier. The main results show that both radix-2 and radix-4 butterflies, with CSA, are more efficient when compared with the same structures with other adder circuits.

Keywords: CSA, Radix-2, Radix-4, FFT architecture, Area, Efficiency, RTL complier.

1. INTRODUCTION

A fast Fourier transform (FFT) is an algorithm that samples a signal over a period of time (or space) and divides it into its frequency components. These components are single sinusoidal oscillations at distinct frequencies each with their own amplitude and phase. An FFT algorithm computes the discrete Fourier transform (DFT) of a sequence, or its inverse (IFFT). Fourier analysis converts a signal from its original domain to a representation in the frequency domain and viceversa. An FFT rapidly computes such transformations by factorizing the DFT matrix into a product of sparse (mostly zero) factors. As a result, it manages to reduce the complexity of computing the DFT from O (n 2) to O(n log n), n is data size. The discrete Fourier transform finds limitless applications in many areas of signal processing. In the era of fast computing it has become increasingly important to enhance the existing FFT algorithms to meet the ever increasing applications in the field of digital signal processing. DFTs have also been extensively used in multi-carrier transmission systems like orthogonal frequency domain multiplexing as FFT processors. In multi-carrier modulation,

such as OFDM and discrete multitone (DMT), data symbols are transmitted in parallel on multiple sub-carriers. Multi-carrier modulation-based transceivers involve real-time DFT computations. FFT based channel estimation method is derived from the maximum likelihood criterion, which is originally proposed for OFDM systems with pilot preambles. In order to save bandwidth and improve system performance, decision-feedback (DF) data symbols are usually exploited to track channel variations in subsequent OFDM data symbols, and this method is called DF DFT-based channel estimation [8]. DFT is extensively used in sonar and radar systems. These systems use millions of multiplications per second. Seismic processing requires extensive processing of seismic data [9]. Computerized tomography is widely used to synthetically form images of internal organs of the human body wherein massive amounts of signal processing are required. Remote sensing is another field employing huge amount of processing. Satellite photographs can be processed digitally to merge several images or enhance features or combine information received on different wavelengths.

The criteria that need to be considered when choosing between alternate FFT algorithm implementations in an FPGA are execution speed, programming effort, hardware design effort, system cost, flexibility and precision. However, for systems for real time signal processing system the primary criteria is latency. There are different FFT algorithms which have been developed to reduce the number of computations. Different special purpose architectures have been developed for these FFT algorithms to reduce the execution speed, thereby increasing throughput and reducing latency. There are other factors which also cause latency to reduce like the use of MMSE MIMO detector shortens processing latency. As discussed in the first chapter, in the last three to four decades several FFT architectures, namely

(i) single-memory architecture
(ii) dual-memory architecture
(iii)Cached memory architecture
(iv)array architecture
(v) Pipelined architecture
(vi)Parallel architecture has been used.

2. RELATED STUDY

Most of the low power implementations of FFT from the literature try to optimize the entire architecture by using techniques such as pipelining, reusing the butterflies in sequential and semi-parallel architectures, or even reordering the twiddle factors such as in fig. However, neither mentioned work proposed to reduce the number of multipliers in the butterfly operator from the FFT architecture. The reduction of the number of multipliers in the radix-2 butterfly was presented, where only two multipliers are used in the butterfly. However, the butterfly was operated at two clock cycles, i.e., the multiplier was reused for the butterfly calculation. In the radix-2 and radix-4 butterflies operate at one clock cycle, but they do not exploit different addition scheme in order to improve the power efficiency of the butterflies, as in this work.

The FFT X (k) of a signal x (n) can be computed using (1), where WN is named twiddle factor, i is the imaginary component and N is the number of points of the FFT. The FFT has a hierarchical computation and

International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
www.ijiemr.org

the butterfly plays a central role in this computation. In this work, radix-2 and radix-4 butterflies are exploited.

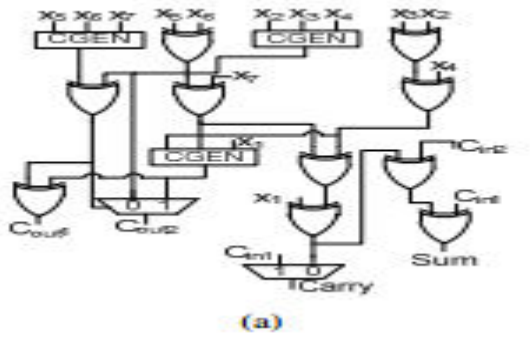


Fig.2.1. 5-2 and 4-2 adder compressors.

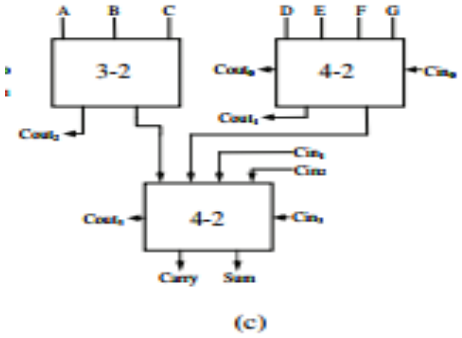


Fig.2.2. 3-2 and 4-2 adder compressors.

Radix-2 Butterfly:

For the DIT radix-2 FFT algorithm, the butterfly allows the calculation of complex terms according to Fig. 1. The butterfly is composed of addition, subtraction and multiplication of complex numbers. In this work, different addition schemes are used in order to improve the implementation of this structure.

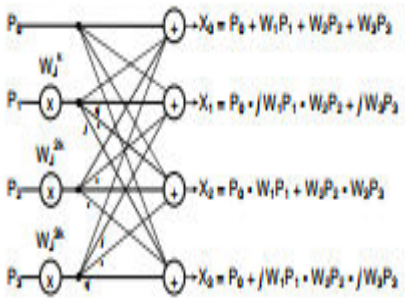
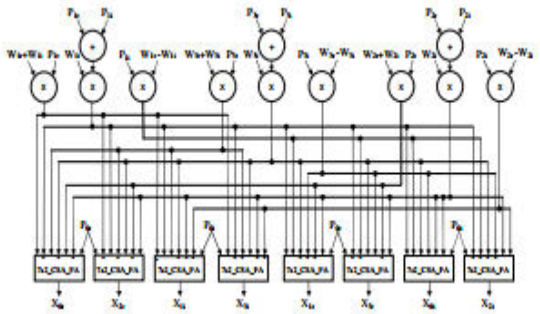


Fig.2.3. Structure of DIT radix-4 butterfly.

The best results for the addition of three operands, in terms of number of cells and cell area, is the structure named 3-2/RCA_3-2, and the best results for power is the structure named CSA_FA/RCA_3-2. In fact, although the CSA structure presents more area, and consequently more leakage power, the aspect of presenting less dynamic power contributes for the slightly reduction in total power in this structure. From now, we will be using in the radix-2 butterfly, the CSA_FA/RCA_3-2 instance.

Table III shows the synthesis results of the 16-bit width addition of seven operands, where five structures were used with 7-2 adder compressor: 1- with the structure of, and shown in Fig. 5(a) (named 7-2_); 2- with one 5-2 and one 4-2 adder compressor (named 7-2_5-2,4-2); 3- with two 4-2 and one 3-2 adder compressor (named 7-2_4-2,3-2); 4- with CSA using 3-2 adder compressors (named 7-2_CSA_3-2), and finally 5- with CSA using FA (named 7-2_CSA_FA). For all structures, the delay was set to 1100ps.

According to this structure, seven operands can be simultaneously added after the multipliers. This observation resulted in the structure with 7-2 adder compressors presented in Fig. We used the architecture named 7-2_CSA_FA that demonstrated the lowest power value in the analysis of the previous section.



International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
www.ijiemr.org

3. OVERVIEW OF PROPOSED SYSTEM

To implement an N -bit CSA, or an N - bit adder compressor, we have to use a recombination of partial Carry and Sum terms. This recombination is made from a cascade of half and full -adders circuits in a RCA form. The line of recombination is a bottleneck in the compressor performance, since the partial carries produced by the actual block are propagated to the next blocks. For the RCA recombination line, four structures were used: 1 - RCA composed of Half Adder (HA) and Full Adder (FA), 2 - RCA composed of HA and 3-2 adder compressor, 3 - RCA based on Carry Look Ahead adder, and finally 4 - RCA based on Kogge -Stone adder.

Radix-2 Butterfly Using the Addition of Three Operands:

The structure presented in Fig corresponds to the optimized structure. By observing this optimized structure, was possible to note that three operands can be simultaneously added after the multipliers, what leads to the structure of Fig. This structure, named CSA_FA/RCA_3- 2.

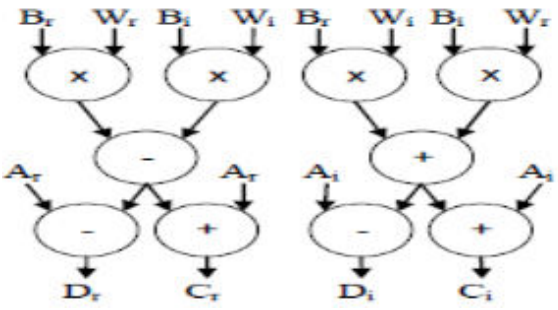


Fig.3.1. Radix 2 butterfly structure with four multipliers.

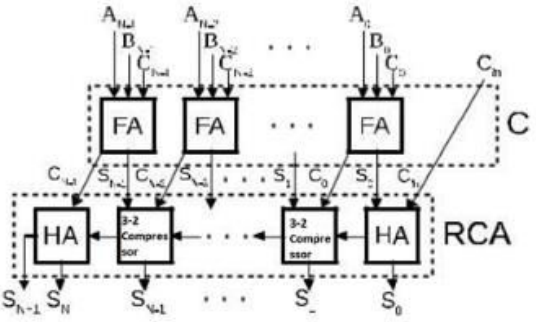


Fig.3.2. CSA_FA/RCA_3-2.

Radix-4 Butterflies Using the Addition of Seven Operands:

The radix -4 butterfly is shown in Fig. According to this structure, seven operands can be simultaneously added after the multipliers. This observation resulted in the structure with 3- 2 adder compressors presented in Fig. We used the architecture named 3 -2_CSA_FA.

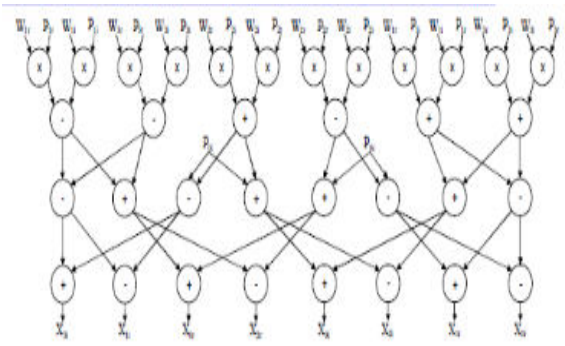
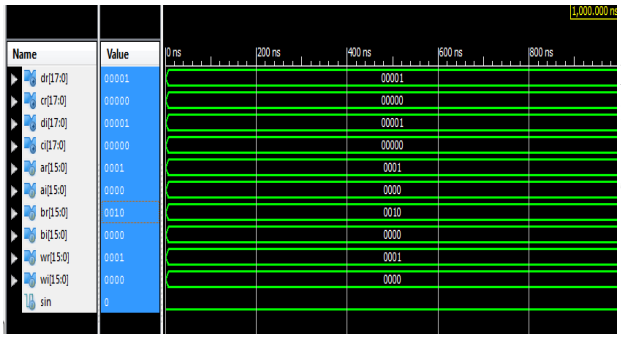


Fig.3.3. Radix-4 butterfly structure.

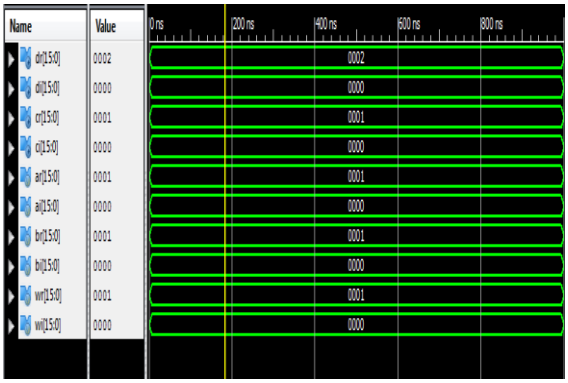
Optimized Radix 4

Radix2 using 3_2 compressor:

International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
www.ijiemr.org



Optimized radix 2




```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 8.832ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

--------------------------------------------------------------------------
```

4. CONCLUSION

This paper presented different addition schemes for radix-2 and radix-4 butterflies. The main results showed that the best adder scheme for the recombination line of CSA and adder compressors are that uses internally HA and 3-2 adder compressor. This efficient recombination line was used in the CSA and adder compressors for three and seven operands additions. As could be presented, the radix-2 and radix-4 butterflies from the literature were improved by using a CSA with FA, and one line of pipeline. These results prove the efficiency of the CSA for both butterflies.

REFERENCES

[1] Chen-Fong Hsian, Yaun Chen, Chen-Yi Lee, "A Generalized Mixed- Radix Algorithm For Memory Based FFT Processer", IEEE Trans. Circuit System II, express briefs, Volume 57 no.1, PP. 26-30, January 2010.

[2] Wen-Chang Yeh, Chein-Wei Jen, "High-Speed and Low-Power Split-Radix FFT ", IEEE Transactions On Signal Processing, Volume 51, NO. 3, PP. 866-874, March 2003.

[3] V. Venkata Lakshmi Dadala,CH. Satya Naresh, R. Anil Kumar "Butterfly Design for Radix-4k DIT FFT", Volume 3, Issue 10, PP. 1348-1353 October - 2014.

[4] K. Sarath Chandra Varma, Ch. Kranthi Kumar, K. Sravan kumar, D. Sharat Chandra varma, N. Rajasekha , " Design and Simulation of 64-Point FFT Using Radix-4 Algorithm for OFDM Applications " ,Volume 10, Issue 2, PP. 35-40, Mar - Apr. 2015.

[5] K. Sreekanth Yadav, V. Charishma, Neelima koppal, "Design And Simulation Of 64 Point FFT Using Radix- 4 Algorithm For FPGA Implementation", Volume4 Issue2 pp.109- 113, 2013.

[6] K. Sowjanya, B. Leele Kumari "Design And Performance Analysis Of 32 And 64 Point FFT Using Radix-2 Algorithm", AECE-IRAJ International Conference", PP. 55-58, 14th July 2013.

[7] Siva Kumar Palaniappan, Tun Zainal Azni Zulkifli "Design of 16-point Radix-4

Fast Fourier Transform in 0.18μm CMOS Technology" Volume 4 Issue8 PP. 570-575, 2007.

[8]Asmita Haveliya "Design and Simulation of 32-Point FFT Using Radix-2 Algorithm for FPGA Implementation"Second International Conference on Advanced Computing & Communication Technologies PP. 168-171, 2012.

[9] Kasina Madhusudhana Rao, V. Ravi Tejesvi, AnanthaRao," Verilog Implementation of 32 Point FFT Using Radix-2 Algorithm on FPGA Technology", (IOSR-JECE) Volume 9, Issue 1, Ver. II, PP. 40-43, Jan. 2014.

[10] Soda Karan G, Brundavani P, "FPGA Implementation of 256-Bit, 64-Point DIT-FFT Using Radix-4 Algorithm" Volume 3, Issue 9, PP. 127-133, September 2013.