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Volume 08, Issue 11, Pages: 228–233.

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EFFICIENT AND HYBRID DESIGN OF QSD BASED ADDER AND MULTIPLIER USING VEDIC MULTIPLIER

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ABSTRACT:

This paper provides a high-speed Vedic multiplier based on the Urdhva Tiryagbhyam sutra of Vedic maths that includes a unique adder based on Quaternary Signed digit number system. Three procedures are inherent in multiplication: partial items generation, partial items reduction and also addition. Rapid adder architecture therefore significantly improves the speed of the general process. Quaternary logic adder architecture is recommended that services a crossbreed of binary as well as quaternary number systems. A given binary string is first divided into quaternary figures of 2 little bits each complied with by parallel addition lowering the lug breeding delay. The style does not need a radix conversion module as the amount is straight produced in binary making use of the unique principle of an adjusting bit. The suggested multiplier design is compared with a Vedic multiplier based on multi voltage or multi worth logic [MVL], Vedic Multiplier that includes a QSD adder with a conversion component for quaternary to binary conversion, Vedic multiplier that utilizes Carry Select Adder and a generally used rapid multiplication system such as Cubicle multiplier. All these designs have been created utilizing Verilog HDL and synthesized by Synopsys Layout Compiler. This paper is devoted to make a high-speed Arithmetic Logic Device. All of us know that, ALU is a module which can do arithmetic as well as reasoning operations. The rate of ALU considerably depends upon the speed of the Multiplier. This paper offers a technique called, "Vedic Maths" for making the multiplier that is quick as contrasted to various other multipliers based on mathematical techniques that have remained in method for a very long time. Right here, a high-speed 32x32 little bit multiplier, division is created and also assessed which is based on the Vedic mathematics mechanism. The proposed technique is effective and also quick, in which the processing involves the upright and also went across multiplication of precedent Vedic maths. The interior multiplier is implemented using Vedic-Wallace structure for high-speed application. The backer of the result is gotten by using Brent-Kung adder for quick computations with much less area utilization. The projected Vedic multiplier is coded in a Verilog complied with by synthesization using an EDA tool, XilinxISE14.2. The proposed ALU has the ability to perform 3 different math as well as eight different rational procedures at broadband. The main objective of this paper is to boost the rate of the multiplier and to decrease the delay, and location of the hardware.

Keywords: FPGA, 32x32 bit multiplier, ALU, EDA, Verilog, vedic.

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1. INTRODUCTION

One of the primary features that help us determine the computational power of a processor is the speed of its arithmetic unit. An important function of an arithmetic block is multiplication because, in most mathematical computations, it forms the bulk of the execution time. Thus, the development of a fast multiplier has been a key research area for a long time. Some of the important algorithms proposed for fast multiplication in literature are Array, Booth and Wallace multipliers. Vedic Mathematics is a methodology of arithmetic rules that allows for more efficient implementations regarding speed. Multiplication in this methodology consists of three steps: generation of partial products, reduction of partial products, and finally carry propagate addition. Multiplier design based on Vedic mathematics has many advantages as the partial products and sums are generated in one step, which reduces the carry propagation from LSB to MSB. This feature helps in scaling the design for larger inputs without proportionally increasing the propagation delay as all smaller blocks of the design work concurrently. References and compared Vedic Multiplier with other multiplier architectures namely Booth, Array and Wallace on the basis of delay and power consumption. Vedic multiplier showed improvements in both the parameters over other architectures. Thus, many implementations of multiplication algorithms based on Vedic sutras have been reported in literature. Vedic multiplier schemes proposed in literature are based on Urdhva Tiryagbhyam and Nikhilam sutras of Vedic Mathematics. As Nikhilam sutra is only efficient for inputs that are close to the power of 10, in this paper a design to perform high-speed multiplication based on the Urdhva Tiryagbhyam sutra of Vedic Mathematics which is generalized method for all numbers, has been presented. Multiplier implementation in the gate level (FPGA) using Vedic Mathematics has already been reported but to the best of our knowledge till date there is no report on transistor level (ASIC) implementation of such complex multiplier. By employing the Vedic mathematics, an N bit complex number multiplication was transformed into four multiplications for real and imaginary terms of the final product. "Nikhilam. Navatascaramam Dasatah" sutra is used for the multiplication purpose, with less number of partial products generation, in comparison with array based multiplication. When compared with existing methods such as the direct method or the strength reduction technique, our approach resulted not only in simplified arithmetic operations, but also in a regular array like structure. The multiplier is fully parameterized, so any configuration of input and output word-lengths could be elaborated.

2. RELATED STUDY

The system speediness of the movement is the critical necessities within organizing Digital signal processor. The unemployment related through checked digits of the numbers offer the probability of the pass on free of charge extension. The main overabundance gave during the checked number depiction considers brisk extension and subtraction in light of the way that the total or qualification and a digit is nothing but a segment of the simply and the two digits bordering digit number spots the main operands used for a radix number more conspicuous than the two, and three neighbouring digit number position used for a radix number of two. Thusly, main

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incorporate time intended for two let go stamped the digit numbers are a relentless self-ruling of the main length of the word operands, in the best approach to quick count. The main benefit of pass on liberated development obtainable by adders of QSD numbers can be used in abused in arranging a quick snake circuit. In addition of snake organized with the adders of QSD number structure has a standard plan which is sensible for VLSI utilization which is the exceptional good position over the RBSD wind. An Algorithm for plan of Quaternary Signed digit number adders wind is projected. Twofold checked digits of the numbers are known to allow compelled pass on spread with a reasonably continuously complex extension process requiring tremendous circuit for utilization. An uncommon upper radix number based (quaternary) depiction of the matched stamped digit of the numbers are not simply allow the pass on free of charge development as well as get free of charge elimination yet what's more offers other fundamental central focuses, for instance, ease in reason and higher amassing thickness.

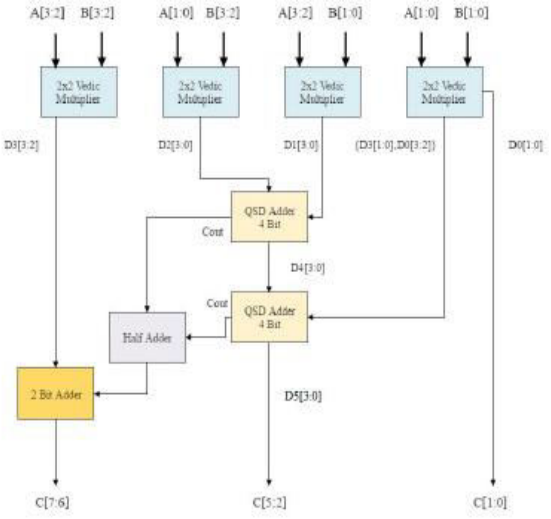

Fig.2.1. 4x4 Multiplier.

3. AN OVERVIEW OF PROPOSED SYSTEM

When the critical path is compared between the critical path in 4 bit conventional and Vedic multiplier, for a 4-bit multiplier, 4 partial products will be generated, as shown in Figure 2 and are named as p0 to p3. For Wallace tree multiplier, a 3:2 reduction is used, so that the partial products are reduced from 4 to 3. The Delay in critical path is given by the addition of 3 full adder sums, 2 full adder carry, and half adder carry. The critical path for Vedic mathematics as shown in Figure 3, is given by 2FAS is reduced by 3HAS and in terms of XOR gates, Vedic-Wallace uses 3XOR gates instead of 4XOR i.e., less carry propagation delay than the conventional method. Hence, Vedic-Wallace has a variable improvement over design ware depending upon the number of bits in multiplication.

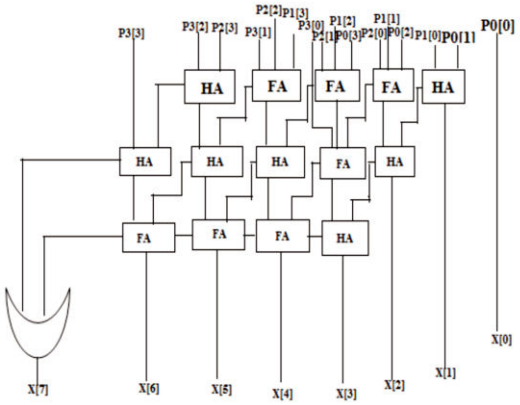

Fig.3.1. 4x4 Multiplier using Wallace Tree.

One of the primary features that help us determine the computational power of a processor is the speed of its arithmetic unit. An important function of an arithmetic block is multiplication because, in most mathematical computations, it forms the bulk of the execution time. Thus, the development of a fast multiplier has been a key research area for a long time. Some of the important algorithms proposed for fast

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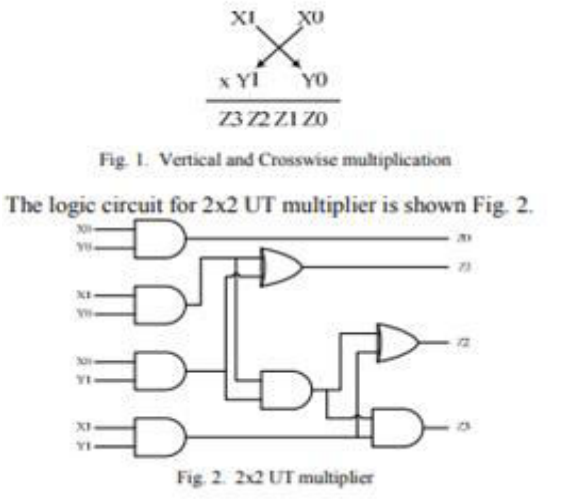

Fig.3.2. 2X2 UT multiplier

The QSD is a radix-4 number system that provides the benefit of faster arithmetic calculations over binary computation, as it eliminates rippling of carry during addition. Every number in QSD can be represented using digits from the set {-3,-2,-1, 0, 1, 2, 3}. Being a higher radix number system it utilizes less number of gates and hence saves on time and reduces circuit complexity. The stages involved in addition of two numbers in QSD are: Stage1: Generation of intermediate carry and sum: When two digits are added in QSD number system, the resulting sum ranges between -6 to +6. Numbers with magnitude higher than 3 are represented by multiple digits with least significant digit representing sum and the next digit corresponds to carry. Also, every number in QSD can have multiple representations.

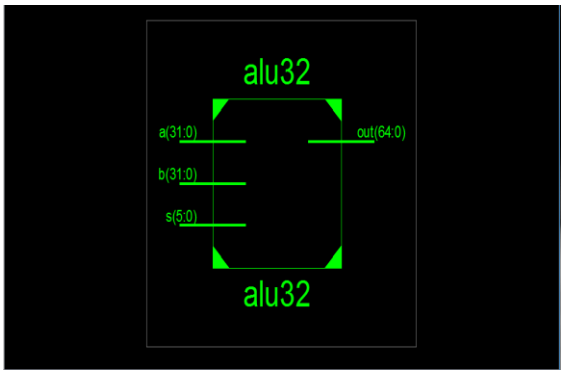

Fig.3.3. RTL model.

For designing of the logical unit, the performance of logic circuits has been analyzed by employing the commonly used logic gates and a multiplexer. A Logic unit does the

Various operations such as Logical AND, OR, XOR, NOT, NAND, NOR, XNOR, and data buffer. In addition to this arithmetic unit and logical unit, they have been combined into the arithmetic logic units. The schematic block diagram of an arithmetic logic unit is shown in Figure that is self-explanatory in itself. The output of the ALU and Logical Unit is 64 bits.

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Fig.3.4. ALU Simulation circuit.

Lowest path delay for various multipliers. This section also deals with the quantitative and comparative result analysis of the different approach to Vedic mathematics through various multipliers and adder design and implementation. Additionally, to validate the proposed Vedic mathematics based various multipliers and adder designs and their implementation, the synthesis and the simulated results have been compared with some other trendy multiplier structures which are designed based on the different multiplication algorithms.

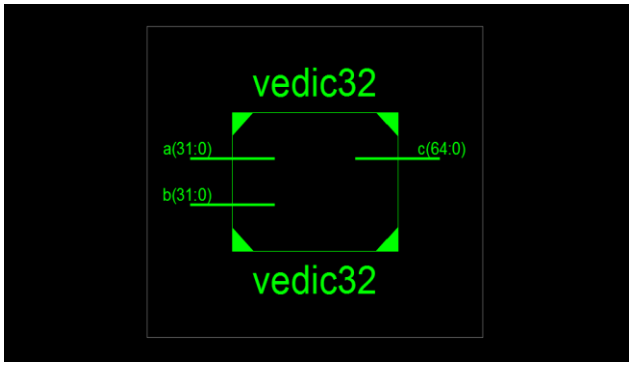

Fig.3.5. VEDIC WALLACE MULTIPLIER 32x32 RTL OUTPUT.

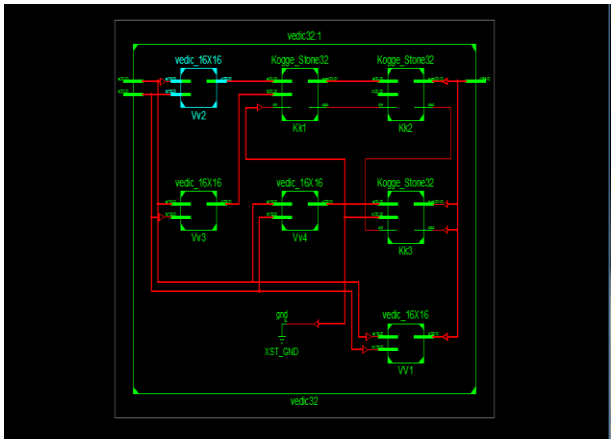

Fig.3.6. Model.

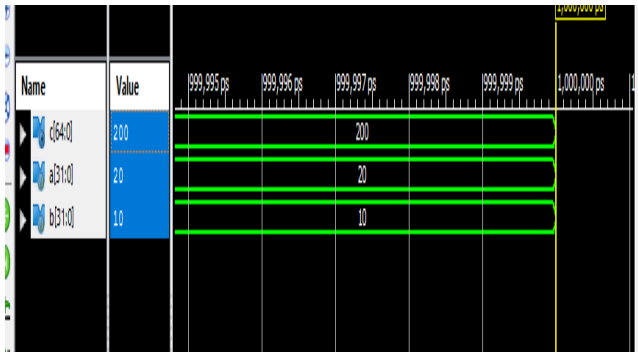

Fig.3.7. Simulation results.

4. CONCLUSION

Through this paper, the authors have presented an extremely effective method of multiplication, i.e. Urdhva- Tiryakbhyam Sutra based on Vedic mathematics. With this method, the multiplier of any number of bits can be designed, and show the computational benefits given by Vedic methods. It is a method for hierarchical multiplier design which clearly indicates the computational advantages offered by Vedic methods. Since the objective was to reduce the delay, the computational path delay for the proposed 32x32 bit Vedic Wallace multiplier is found to be 54.004ns. The Vedic Wallace multiplier is much more efficient than Vedic multiplier and Array multiplier in terms of execution time (speed) and Area Delay Product. So we can say Vedic mathematics can be included in the education systems and help students learn mathematics fast and perform better in less time. In future, all the research centers are to promote research works in Vedic mathematics.

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