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IMPLEMENTATION OF HIGH EFFICIENT PARTIAL PRODUCT REDUCTION BASED APPROXIMATE MULTIPLIERS USING VERILOG

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ABSTARCT:

Approximate computing can decrease the design complexity with an increase in performance and power efficiency for error resilient applications. This brief deals with a new design approach for approximation of multipliers. The partial products of the multiplier are altered to introduce varying probability terms. Logic complexity of approximation is varied for the accumulation of altered partial products based on their probability.

The proposed approximation is utilized in two variants of 16-bit multipliers. Synthesis results reveal that two proposed multipliers achieve power savings of 72% and 38%, respectively, compared to an exact multiplier. They have better precision when compared to existing approximate multipliers. Mean relative error figures are as low as 7.6% and 0.02% for the proposed approximate multipliers, which are better than the previous works. Performance of the proposed multipliers is evaluated with an image processing application, where one of the proposed models achieves the highest peak signal to noise ratio.

Keywords Approximate Carry Adder, Three Dimensional Reduction method, Approximate Multiplier

I. INTRODUCTION:

Exact and precise models and algorithms are not always appropriate for proficient use in multimedia and image processing operations. The model of approximate calculation relies on entirely relaxing fully exact and completely deterministic building blocks while, designing energy-efficient systems. In digital designs, integer multiplication is one of the fundamental building blocks, which deeply affects the microprocessor and DSP performance. A faster digital circuit is obtained by implementing a speculative (prediction) approach. Speculative digital circuits are based on faster operation by employing a speculative functional unit, which is an arithmetic unit that employs a predictor for

the carry signal, without actually waiting for the carry propagation. The speculative unit predicts the carry of the one or more cells used in the digital circuit without waiting for the actual carry propagation to take place. This is similar to a predictor in the microprocessor. Here we have considered a speculative multiplier which consists of a predictive carry-save reduction tree using three steps: partial products recoding, partial product partitioning and speculative compression. The speculative tree utilize (m: 2) counters, and are faster than traditional compressors based on half adders and full adders. The tree is further comprised of a fast carry-propagate adder and an error rectification circuit. Speculative multipliers have higher speed compared to their conventional counterparts.

II. PREVIOUS WORKS

[10] Shows that approximate circuits have higher performance as compared to precise logic circuits. Many inexact multipliers have been proposed in the literature [4] [6] [7] [13]. These designs employ a truncated multiplication method. In [6], an inexact array multiplier is used, by ignoring selected least significant bits in partial products. A inexact multiplier with correction constant has been proposed in [13]. A variable correction constant inexact multiplier is proposed in [4].This method modifies the correction term according to column n-k-1. If partial products in column n-k-1 are one, then correction factor is increased and, if all partial products in the above column are zero, the correction factor is decreased. In [7], a basic 2x2 multiplier block is suggested for constructing larger multiplier arrays. In all these designs the area was found to be very high. In [11] another approximate multiplier with two approximate [4:2] compressor has been proposed. This multiplier requires lesser area as compared to multipliers using truncation technique however the error percentage was found to be very high.

[12] Describes another approximate multiplier design which utilizes prediction units for the carry signal and also has lesser error percentage as compared to [11]. SFUs (Speculative Functional Units) are prediction circuits that can be considered as black box entities which are faster than their non -speculative counterparts, independently of the particular implementation [8]. Hence approximate multipliers using SFUs also aim to achieve delay improvements, at the same time introducing less power and area overheads. This multiplier utilises Carry Save Adder (CSA) tree [14] for partial product reduction, wherein the carry outputs are propagated rather than being preserved thereby reduces the delay. Popular CSA schemes include Wallace tree and Dadda multiplier. Wallace tree [1] [9] result in long and irregular wires along the columns to connect to the CSA. The wire capacitance in turn increases the delay and energy of the multiplier and the wires are difficult to layout. Dadda refined Wallace's method by introducing a counter placement strategy that requires few numbers of counters in the reduction stage but at the cost of larger Carry propagate Adder (CPA) [2] [9]. The delay from an input to an output in a full adder is not the same. This delay is dependent on a particular transition (0-to-1,

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1-to-0). Therefore it is also possible to come up with different realizations of a full adder wherein a specific signal path is favored with respect to the others and has been designed in such a way that a signal propagation of this path takes a minimal amount of time [3]. The CSA scheme which takes care of this delay in transition is Three Dimensional Scheme (TDM) [3], where partial product array is represented in space and time. This is followed by a speculative adder [5].

III. EXISTING DESIGN MODEL FOR APPROXIMATE MULTIPLIERS

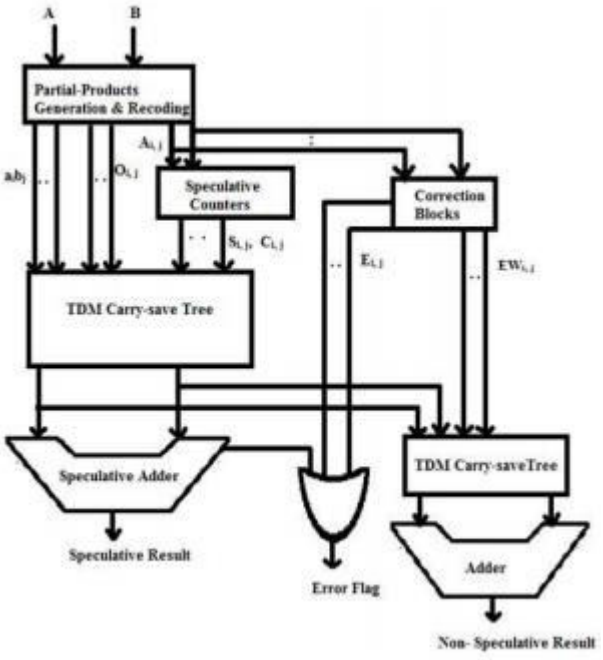

Fig. 1. Architecture of Approximate Multiplier

3.1 Partial Product Recoding

Consider two partial products aibj and ajbi of the i+j-th column of the PPM. Now we will define two modified partial products:

Ai, j = aibj AND ajbi (1)

Oi, j = aibj OR ajbi (2)

Thus couple of partial products aibj and ajbi can be replaced with modified partial products Ai, j and Oi, j. The advantage of introducing such a recoding technique is the introduction of lower probability terms in the PPM. The probability of Ai, j is given by (.25)2 = 0.0625, much lower than the probability of the original partial product (i.e. 0.25). Alternatively the probability of Oi, j is 7/16. From the above two observations it can be concluded that speculative carry tree utilizes lower probability terms, to minimize the probability of misprediction. The introduction of recoded terms does not modify the total number of partial products, but introduces an additional very small delay for the recoded partial products. The figure below shows a 16 X 16 Partial Product Matrix (PPM) after being recoded.

3.2 Partial Product Partitioning Only the lower probability terms Ai, j is has been added in the speculation carry-save tree. Partial products that belong to the largest columns of PPM are singly recoded. In the figure given below the partial products in the columns 11, 12……22 are recoded.

3.3 Speculative Compression Although the probability Ai, j has been decreased with respect to the actual partial products, simple removal of Ai, j terms would bring about a large misprediction error probability. Thus, instead of omitting these terms we sum them in an approximate manner by using speculative compressors. A (m: 2) speculative counter has m inputs (x0….xm-1) and only two outputs Sum (S) and Carry (C). The speculation compressor counts the

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number of input bits and determines the output bits, on the supposition that not than more than three inputs are high. Analogously to full adders and half adders, the output C has a doubled weight with respect to S, so that 2C + S = x0 +x1……..+.xm-1 for: x0 +x1……..+.xm-1 3, it is not possible to represent sum x0 +x1……..+.xm-1, by using only C and S signals for all likely input configurations. The speculation counter computes the outputs based on the supposition that not more than three inputs are high: If this criterion is not met, an error occurs; the multiplication result is wrong and must be corrected.

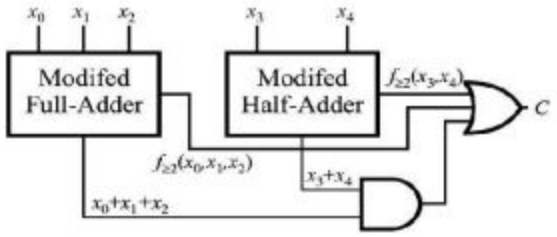


Fig. 2.Speculative Compressor

IV. PROPOSED MODEL FOR APPROXIMATE MULTIPLIER FOR DSP APPLICATIONS:

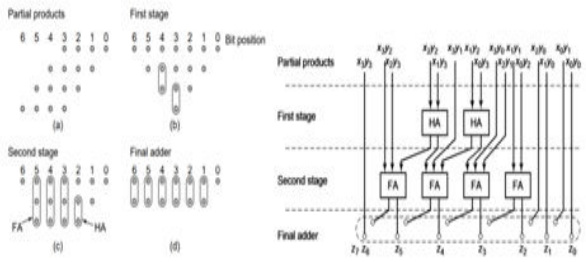
CONCEPT:

As the demand of high computational speed along with compact area and low power consumption is becoming indispensable, it‟s very important for the most fundamental components to be highly efficient. Hybrid adder is the combination of two different adders or implementing a new logic style in the conventionally existing adders. In hybrid adders, the addition is performed using two adders. The addition of Least Significant Bit (LSB) is carried out by one adder and the Most Significant Byte (MSB) is carried out by another adder. The main objective to design hybrid adder is to take up the advantages of the adders connected to make it more efficient than individual adder.

An N bit adder for designed multiplier has N rows in first stage and remaining rows are calculated as: $r_i = \left\lfloor \frac{2r_{i-1}}{3} \right\rfloor + r_{i-1} \bmod 3.$ (1)

Here we have proposed Normalized Hybrid Adder which utilizes MSB bits via Kogge stone adder and for LSB we use Wallace prefix tree. For, the partial products in multiplier and adder which are readjusted in a reverse pyramid style which makes it easy to analyze the tree for efficient reduction. The number of stages for RCW multiplier remains the same as that of TW multiplier. RCW tries to reduce the partial product tree using only full adders. Half adders are used only where they are necessary to satisfy the number of rows in a stage according to (1). This approach allows RCW multiplier to reduce the area of the reduction process. However, RCW multiplier uses a much larger final adder as compared to TW multiplier. The size of the final adder for an N bit Multiplier as (2*N-2).Note: RCW: - Reduced Complexity Wallace

4.1 Wallance tree multiplier:



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shown in KSA, Here each Partial product for each stage are calculated based on the mathematical equation section. This section of multiplier with each design stage based on kogee stone partial product in all the stage mention in the above figure

4.2 Kogge stone adder:

The Kogge-Stone adder is a parallel prefix form of carry look-ahead adder. It generates the carry signals in O (log2N) time, and is widely considered as the fastest adder design possible. It is the most common architecture for high-performance adders in industry. The Kogge-Stone adder concept was first developed by Peter M. Kogge and Harold S. Stone. In Kogge-stone adder, carries are generated fast by computing them in parallel at the cost of increased area.TheKogge Stone Adder (KSA) has regular layout which makes them favored adder in the electronic technology. Another reason the KSA is the favored adder is because of its minimum fan-out or minimum logic depth. As a result of that, the KSA becomes a fast adder but has a large area .The delay of KSA is equal to log2n which is the number of stages for the "o" operator. The KSA has the area (number of "o" operators) of (n*log2n)-n+1 where n is the number of input bits.The complete functioning of KSA can be easily comprehended by analyzing it in terms of three

distinct parts :

1. Pre processing

This step involves computation of generate and propagate signals corresponding too each

pair of bits in A and B. These signals are given by the logic equations below:

pi = Ai *xor*Bi

gi = Ai *and* Bi

2. Carry look ahead network

This block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the logic equations below:

Pi:j = Pi:k+1 *and Pk:j*

Gi:j = Gi:k+1 *or* (Pi:k+1 *andGk:j*)

3. Post processing

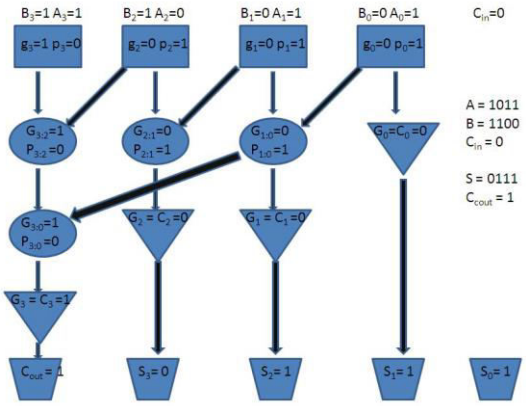
This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits. Sum bits are computed by the logic given below:

Si = pi xor Ci-

4. Illustration

The working of KSA can be understood by the following Fig. 1 which corresponds to 4-bit

KSA. 4-bit KSA is shown for simplicity.



5. Implementation

The schematic of KSA is implemented by using following building blocks :

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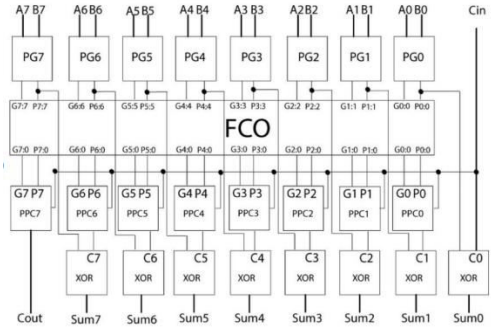
1. Bit propagate and generate This block implements the following logic:

Gi= Ai **AND** Bi

Pi = Ai **XOR** Bi

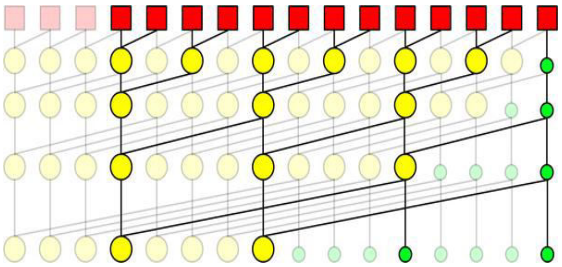
4.2 8 bit Proposed Kogge-stone Adder:



The kogge-stone adder operation is shown for 8 bit. From LSB to MSB we can observe that in each stage the black nodes are reducing or shifted to 2^{l-1}, (where l = stage number) horizontally and the reduced black nodes are inserted with white nodes. The nodes are either propagation or generation units which are utilized for parallel additions of each Full and half adder structure.Implementation of 8-bit and 16 and 32 multiplication using reduced complexity Wallace tree multiplier and (kogge-stone) parallel prefix adder has been simulated.

Enhancements

Enhancements to the original implementation include increasing the radix and sparsity of the adder. The *radix* of the adder refers to how many results from the previous level of computation are used to generate the next one. The original implementation uses radix-2, although it's possible to create radix-4 and higher. Doing so increases the power and delay of each stage, but reduces the number of required stages. In the so called **sparse Kogge–Stone adder** (**SKA**) the *sparsity* of the adder refers to how many carry bits are generated by the carry-tree. Generating every carry bit is called sparsity-1, whereas generating every other is sparsity-2 and every fourth is sparsity-4. The resulting carries are then used as the carry-in inputs for much shorter ripple carry adders or some other adder design, which generates the final sum bits. Increasing sparsity reduces the total needed computation and can reduce the amount of routing congestion.



Above is an example of a Kogge–Stone adder with sparsity-4. Elements eliminated by sparsity shown marked with transparency. As shown, power and area of the carry generation is improved significantly, and routing congestion is substantially reduced. Each generated carry feeds a multiplexer for a carry select adder or the carry-in of a ripple carry adder.

Expansion

This example is a carry look ahead - In a 4 bit adder like the one shown in the introductory image of this article, there are 5 outputs. Below is the expansion:

S0 = (A0 XOR B0) XOR Cin

S1 = (A1 XOR B1) XOR ((A0 AND B0) OR (A0 XOR B0) ANDCin)

S2 = (A2 XOR B2) XOR (((A1 XOR B1) AND ((A0 AND B0) OR (A0 XOR B0) AND Cin)) OR (A1 AND B1))

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S3 = (A3 XOR B3) XOR ((((A2 XOR B2) AND (A1 XOR B1)) AND ((A0 AND B0) OR (A0 XOR B0) AND Cin)) OR (((A2 XOR B2) AND (A1 AND B1)) OR (A2 AND B2)))

S4 = (A3 AND B3) OR (A3 XOR B3) AND ((((A2 XOR B2) AND (A1 XOR B1)) AND ((A0 AND B0) OR (A0 XOR B0) AND Cin)) OR (((A2 XOR B2) AND (A1 AND B1)) OR (A2 AND B2)))

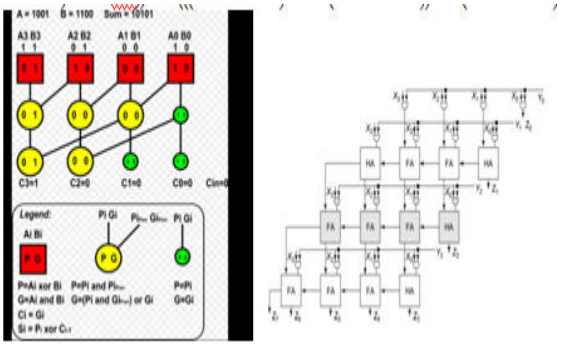

Figure 4.4 : Representing Parallel Array Multiplier structure. {Kogee and Wallace}

Half Adder : Approximate Half adder using 4:2 compressor

Full Adder: Approximate Full adder Using 7:4 compressor.

4.5 Operation:

Execution of multiplier contains three phases:

- Generation of partial things,
- Partial things diminish tree, ultimately,
- a vector mix development to make last thing from the aggregate and pass on segments created from the diminishing tree.

Second step uses more power. In this short, estimation is associated in diminish tree organize. A 8-bit unsigned1 multiplier is used for layout to portray the proposed system in gauge of multipliers. Consider two 8-bitunsigned input operands α = _7m=0 αm2m and β = _7n=0 βn2n.

The deficient thing am,n = αm · βn in Fig. 1 is the outcome of AND assignment between the bits of αm and βn.The proposed inaccurate methodology can be associated with checked duplication including Booth multipliers as well, except for it isn't associated with sign extension bits.

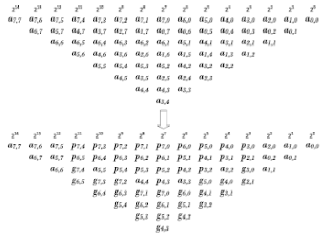

Fig. 4.6. Transformation of generated partial products into altered partial products.

4.7 PROBABILITY STATISTICS OF GENERATE SIGNALS:

TABLE I :Probability of the generate elements.

m	Probability of the *generate* elements being				P_{err}
	all zero	one 1	two 1's	three 1's and more	
2	0.8789	0.1172	0.0039	-	0.00390
3	0.8240	0.1648	0.0110	0.00024	0.01124
4	0.7725	0.2060	0.0206	0.00093	0.02153

From correct viewpoint, the insufficient factor am, n has a opportunity of one/four of being 1. In the portions containing more than three midway things, the insufficient things am, n and an, m are united to define propagate and make moves as given in (1). The ensuing propagates and make indicators

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define changed inadequate matters pm, n and gm, n. From location 3 with weight 23 to phase eleven with weight 211, the partial things am, n and an, m are supplanted by means of changed inadequate things pm, n and gm, n. The first and modified fragmentary aspect structures are confirmed up in Fig. 1

pm,n = am,n + an,m

gm,n = am,n ⋅ an,m. (1)

The probability of the changed fragmented component gm,n being one is 1/sixteen, that is out and out decrease than 1/four of am,n. The probability of changed fragmentary aspect pm,n being one is 1/sixteen + 3/sixteen + 3/sixteen = 7/16, that is higher than gm,n. These elements are considered, whilst applying supposition to the changed fragmentary issue go segment.

Approximation of Other Partial Products:

The storing up of other midway matters with opportunity ¼ for am,n and seven/sixteen for pm,n uses deduced circuits. Assessed half-snake, full-snake, and 4-2 blower are proposed for their social occasion. Carr y and Sum are two yields of those assessed circuits. Since Carr y has higher weight of matched piece, bungle in Carry bit will contribute more by making botch qualification of two in the yield. Figure is managed with the purpose that the combination difference between real yield and prompted yield is usually saved up as one. In this manner Carr y yields are approximated best for the cases, where Sum is approximated. In adders and blowers, XOR entryways generally tend to feature to excessive district and postpone. For approximating 1/2-wind, XOR passage of Sum is supplanted with OR entryway as given in (2). This outcomes in a solitary bumble in the Sum figuring as located as a preferred rule desk of expected half-snake in Table II. A tick test implies that inferred yield suits with rethink yield and pass stamp implies jumble

Entire = x1 + x2

Carr y = x1 ⋅ x2. (2)

In t hegauge of full-snake, one of the two XOR gateways is supplanted with OR entryway in Sum calculation. This outcomes in botch in ultimate two instances out of eight instances. Carr y is balanced as in (3) displaying one goof. This offers greater revisions, whilst preserving up the qualification among exceptional and evaluated a motivator as one. Reality table of harsh full-wind is given in Table III

W = (x1 + x2)

Total = W ⊕ x3

Carry = W ⋅ x3. (3)

Two construed four-2 blowers in [5] carry nonzero yield regardless of for the instances in which all facts assets are zero. This consequences in high ED and unusual kingdom of precision incident mainly in examples of zeros in all bits or in maximum crucial elements of the lessening tree. The

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proposed 4-2 blower vanquishes this drawback. In 4-2 blower, three bits are required for the yield precisely while all of the 4 wellsprings of records are 1, which occurs handiest as soon as out of 16 cases. This assets is taken to forgo one of the three yield bits in four-2 blower.

To keep up inappropriate screw up differentiate as one, the yield "100" (the estimation of 4) for 4 statistics resources being one desires to b supplanted with yields "11" (the estimation of 3). For Sum figuring, one out of 3 XOR entryways is supplanted with OR door. In like way, to make the Sum identifying with the circumstance wherein all records sources are ones as one, a further circuit x1 · x2 · x3 · x4 is brought to the Sum verbalization. This results in goof in 5 out of 16 instances. Carr y is unraveled as in (four). The searching at truth table is given in Table IV

TABLE II TRUTH TABLE OF APPROXIMATE HALF ADDER

Inputs		Exact Outputs		Approximate Outputs		Absolute Difference
x1	x2	Carry	Sum	Carry	Sum	
0	0	0	0	0 ✔	0 ✔	0
0	1	0	1	0 ✔	1 ✔	0
1	0	0	1	0 ✔	1 ✔	0
1	1	1	0	1 ✔	1 ✗	1

TABLE III TRUTH TABLE OF APPROXIMATE FULL ADDER

Inputs			Exact Outputs		Approximate Outputs		Absolute Difference
x1	x2	x3	Carry	Sum	Carry	Sum	
0	0	0	0	0	0 ✔	0 ✔	0
0	0	1	0	1	0 ✔	1 ✔	0
0	1	0	0	1	0 ✔	1 ✔	0
0	1	1	1	0	1 ✔	0 ✔	0
1	0	0	0	1	0 ✔	1 ✔	0
1	0	1	1	0	1 ✔	0 ✔	0
1	1	0	1	0	0 ✗	1 ✗	1
1	1	1	1	1	1 ✔	0 ✗	1

W1 = x1 · x2

W2 = x3 · x4 Sum = (x1 ⊕ x2) + (x3 ⊕ x4) + W1 · W2

Carr y = W1 + W2. (4)

This indicates the diminishing of changed midway aspect device of eight*eight harsh multiplier. It calls for ranges to make sum and pass on yields for vector blend development step. Four 2-facts OR gateways, four three-information OR entryways, and one 4-data OR entryways are required for the lessening of create indicators from areas 3 to eleven. The resultant indications of OR entryways are set apart as Gi contrasting with the component I with weight 2i .

For diminishing other fragmentary matters, three faulty half of-adders, 3 harsh full-adders, and 3 inferred blowers are required within the primary stage to make Sum and Carr y symptoms, Si and Ci figuring out with section I . The components inside the 2d degree are diminished the usage of 1 erroneous 1/2-snake and eleven evaluated complete-adders making final operands xi and yi to be sustained to swell skip on snake for the closing figuring of the end result.

TABLE IV TRUTH TABLE OF APPROXIMATE 4-2 COMPRESSOR

Inputs				Approximate outputs		Absolute Difference
x1	x2	x3	x4	Carry	Sum	
0	0	0	0	0 ✔	0 ✔	0
0	0	0	1	0 ✔	1 ✔	0
0	0	1	0	0 ✔	1 ✔	0
0	0	1	1	1 ✔	0 ✔	0
0	1	0	0	0 ✔	1 ✔	0
0	1	0	1	0 ✗	1 ✗	1
0	1	1	0	0 ✗	1 ✗	1
0	1	1	1	1 ✔	1 ✔	0
1	0	0	0	0 ✔	1 ✔	0
1	0	0	1	0 ✗	1 ✗	1
1	0	1	0	0 ✗	1 ✗	1
1	0	1	1	1 ✔	1 ✔	0
1	1	0	0	1 ✔	0 ✔	0
1	1	0	1	1 ✔	1 ✔	0
1	1	1	0	1 ✔	1 ✔	0
1	1	1	1	1 ✗	1 ✗	1

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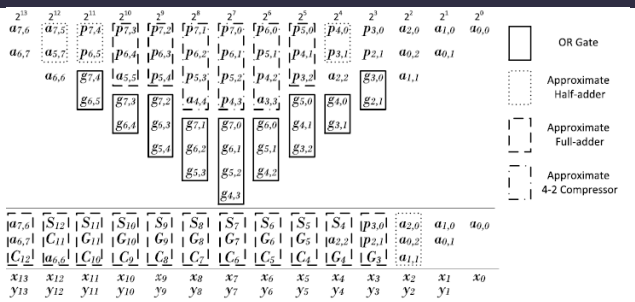

Fig. 4.8. Reduction of altered partial products.

Two Variants of Multipliers

Two varieties of multipliers are proposed. In the essential case (Multiplier1), estimation is associated in all fragments of partial aftereffects of n-bit multiplier, however in Multiplier2, vague circuits are used in n − 1 smallest enormous segment

V. SIMULATION RESULTS

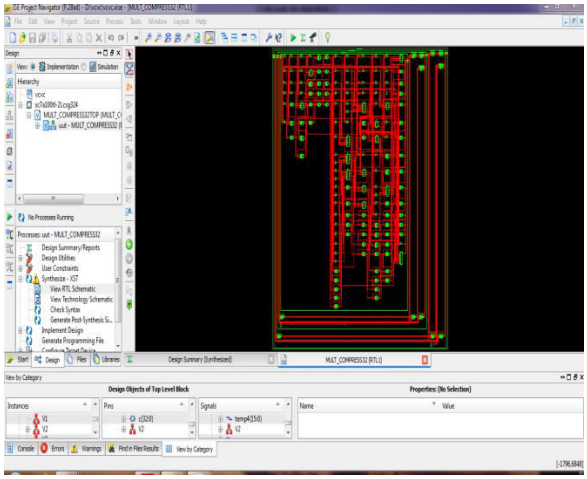

Fig. 7.1.RTL Schematic

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	88	960	9%
Number of 4 input LUTs	155	1920	8%
Number of bonded IOBs	32	108	29%

Fig. 7.2.Design Summary

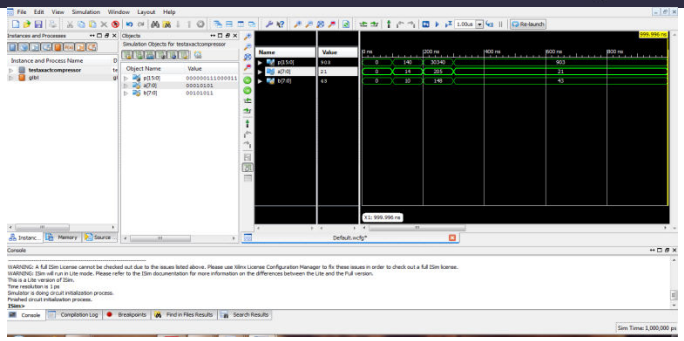

Fig. 7.3.a Approximate Multiplier(16 bit) output

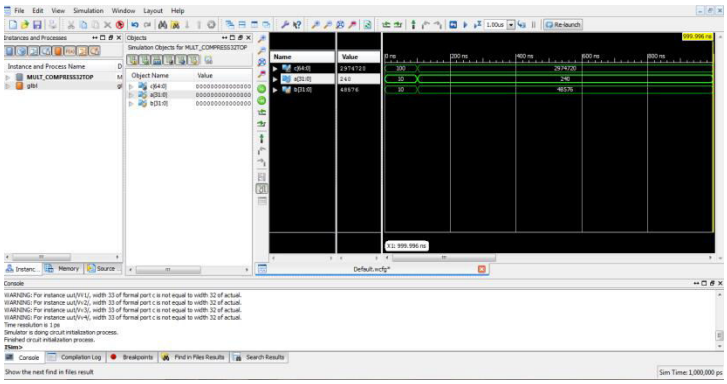

Fig. 7.3.a Approximate Multiplier(32 bit) output

TABULATED RESULTS:

DEVICE: LOW POWER ARTIX 7

SN0	MULTIPLIER(n)	ADDER(N)	AREA(%)		POWER		DELAY	
	EXISITING (8)	EXISITING (8)	7.8		4.89W		7.4 ns	9.3 ns
	PROPOSED (16)	PROPOSED (16)	11 (Adder)	14 (MUL)	0.65W(Adder)	2.268W (MUL)	5.2 ns(Adder)	16.17 ns(MUL)
	PROPOSED (32)	PROPOSED (32)	21 (Adder)	14 (MUL)	1.347W(Adder)	2.268W (MUL)	8.2 ns(Adder)	30.34 ns (MUL)

1. We are design 16bit&32bit hybrid adder.instead of Full adders we use compressors (here we use 4:2 compressor,6:4 compressor And 7:4 compressors).
2. Two types of delays are there 1).Logic delay

2).Route delay

3. Here the existing design was proposed on Low power Artix -7 for 8 bit adder and 8 bit multiplier, also the proposed scenario is extended via its adder and multiplier implementation for real time applications
4. These changes in Adder and multiplier for proposed design has provided extensive changes when compared individually but as a whole multiplier we have only changes observed
5. As per the proposed design we have reduced the adder delay about 9.6 ns improvement specially when compared to twice of 8 bit existing design.
6. Similarly when compared to 32 bit we have reduced about 21.4 ns improved stats, resulting higher speed accuracy.

CONCLUSION

In this brief, to propose proficient inexact multipliers, halfway results of the multiplier are altered utilizing produce and spread signs. Estimate is connected utilizing basic OR entryway for adjusted create fractional items. Inexact half-adder, full-adder, and 4-2 compressor are proposed to diminish staying fractional items. We have proposed a hybrid Adder scenario for the existing model to establish specific functional problems observed. To improvise such problems we have modelled a Wallace prefix and kogee stone prefix to analyze the design parametric aspects such as power, area and delay by reducing prefix tree structure and accompanying with different stages partial product which leads to accomplish critical decrease in area and power utilization contrasted and correct design scenario. Hence, the proposal for hybrid adder have an additionally found to have better accuracy when contrasted with existing surmised multiplier outlines. The proposed multiplier scheme can be utilized in applications with negligible errors in output quality while sparing huge influence on design structures.

FUTURE SCOPE

Redundant basis (RB) multipliers over Galois Field have gained huge popularity in elliptic curve cryptography (ECC) mainly because of their negligible hardware cost for squaring and modular reduction. In this paper, we have proposed a novel recursive decomposition algorithm for RB multiplication to obtain high-throughput digit-serial implementation. Through efficient projection of signal-flow graph (SFG) of the proposed algorithm, a highly regular processor-space flow-graph (PSFG) is derived. By identifying suitable cut-sets, we have modified the PSFG suitably and performed efficient feed-forward cut-set retiming to derive three novel multipliers which not only involve significantly less time-complexity than the existing ones but also require less area and less power consumption compared with the others. Both theoretical analysis and synthesis results confirm the efficiency of proposed multipliers over the existing ones.

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