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POWER EFFICIENT MULTI BIT GATE DRIVEN ANALYSIS FOR FLIP FLOPS USING VERILOG

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ABSTRACT:

Power reduction has become a vital design goal for sophisticated design applications, whether mobile or not. Researchers have shown that multi-bit flip-flop is an effective method for clock power consumption reduction. The underlying idea behind multi-bit flip-flop method is to eliminate total inverter number by sharing the inverters in the flip-flops. Since the ring counter is made up of an array of D-type flip-flops (DFFs) triggered by a global clock signal it is possible to disable the clock signal to most DFFs. Such a gated-clock ring counter is implemented to compose a low-power first-in first-out (FIFO) memory. In this paper, we will review multi-bit flip-flop concepts, and introduce the benefits of using multi-bit flip-flops in our design. We proposed to use double-edge-triggered (DET) flip-flops instead of traditional DFFs in the ring counter to halve the operating clock frequency. A novel approach using the C-elements instead of the R-S flip-flops in the control logic for generating the clock-gating signals is adopted to avoid increasing the loading of the global clock signal. The technique will greatly decrease the loading on distribution network of the clock signal for the ring counter and thus the overall power consumption. The same technique is applied to the input driver and output driver of the memory part in the delay buffer. Then, we will show how to implement multi-bit flip-flop methodology using gated drive tree by Microwind Design Compiler. Experimental results indicate that multi-bit flip-flop using gated drive tree is very effective and efficient method in lower -power designs.

INTRODUCTION:

Optimizations in VLSI have been done on three factors: Area, Power and Timing (Speed). Area optimization means reducing the space of logic which occupy on the die. This is done in both front-end and back-end of design. In front-end design, proper description of simplified Boolean expression and removing unused states will lead to minimize the gate/transistor utilization.

Partition, Floor planning, Placement, and routing are perform in back-end of the design which is done by CAD tool .The CAD tool have a specific algorithm for each process to produce an area efficient design similar to Power optimization. Power optimization is to reduce the power dissipation of the design which suffers by operating voltage, operating frequency, and

switching activity. The first two factors are merely specified in design constraints but switching activity is a parameter which varies dynamically, based on the way which designs the logic and input vectors. Timing optimization refers to meeting the user constraints in efficient manner without any violation otherwise, improving performance of the design. High performance designs are achieved by proper placement, routing and sizing the element. The word optimization is approached in different ways by merging, instead of sizing the memory element. Some of the basic ideas of timing optimization approach are (a) Circuit re- synthesis.

MOTIVATION

The idea of designing the multi-bit flip flop arises for power considerations and placement rout-ability effectiveness. Some of them are discussed here: Minimization of dynamic clock power leads the way to merge the single-bit flip flops and constructed Multi-Bit Flip-Flops. This merging process also has to satisfy the certain area constraint which decreases the total flipflop area in synchronous design the clock power by congested constraints of unallocated bins and the length of constraints of the input and output signals of all the 1-bit flip-flop. Here redundant inverters in merging of single-bit flip-flop are eliminated. The multi-bit flip-flops are mostly viewed as low power design technique, MBFFs with larger bit numbers as possible to gain more clock power saving but larger bit number may lead to severe crosstalk's due to close interconnecting wires .To address this problem step by step procedure those are creating crosstalk model of MBFF, next coupling Capacitance

Generation from these derive Flip-Flop and Intersection Graph are considered. A clustering and Placement is done by reducing the interconnect wire length. Merging of Flip-Flop is done through library that perform a coordinate transformation to identify those flip-flops that can be merged and their legal regions. This approach reduces the wire length considerably. The Digital design uses the single-bit Flip Flop for memory applications and controller design. D flip flops are implemented in two ways which are Master-Slave latch pair and pulse-triggered latches. Most of the design involving standard cell follows Master-Slave approach because of the restricted timing constraints of pulse triggered latches. In master-slave approach, two latches are connected in serial manner with complementary clock signal in serial manner with complementary clock signal.

LITERATURE SURVEY:

Gollapudi. Venkateswarlu —Power has become a burning issue in modern VLSI design. In modern integrated circuits, the power consumed by clocking gradually takes a dominant part. Given a design, we can reduce its power consumption by replacing some flip-flops with fewer multi-bit flip-flops. However, this procedure may affect the performance of the original circuit. Hence, the flipflop replacement without timing and placement capacity constraints violation becomes a quite complex problem. To deal with the difficulty efficiently, we have proposed several techniques. First, we perform a coordinate transformation to identify those flip flops that can be merged and their legal regions. Besides, we show how to build a



combination table to enumerate possible combinations of flip-flops provided by a library. Finally, we use a hierarchical way to merge flip-flops. Besides power reduction, the objective of minimizing the total wire length is also considered. The time complexity of our algorithm is $O(n^{1.12})$ less than the empirical complexity of $O(n^2)$. According to the experimental results, our algorithm significantly reduces clock power by 20–30% and the running time is very short. In the largest test case, which contains 1 700 000 flip-flops, our algorithm only takes about 5 min to replace flip-flops and the power reduction can achieve 21%.

1CHALLA SANKARAMMA,
2K.D.MOHANA SUNDHARAM, 3M.
JASMINE, As technology advances, a systems-on-chip (SOC) design can contain more and more components that lead to a higher power density. Timing Optimization is also one of the most important objectives of the designer in the Modern VLSI world. Power consumed by clocking has taken a major part of the whole design. Reducing the power consumption not only can enhance battery life but also can avoid the overheating problem. The basic memory elements of designer considerations are Latch and flip flop. Multi-bit flip-flop is an effective method for clock power consumption reduction proven by the researchers. For improving Flip flop performance one of the promising way is to merge the clock pulse. The Multi-bit Flip-flop is designed by single clock pulse and achieves same functionality like two single-bit Flipflop. In this paper, we analyze the design of Single-bit Flip-flop (SBFF) and performance comparison over

the Multi-bit Flip-flop (MBFF). We can extend over Parameterized flip flops. A shift register is designed using both Single-Bit FlipFlop (SBFF) and Multi-Bit Flip-Flop (MBFF). We implemented an adder by using the Multi bit flip flop technology. It consumes less power than normal adder. This paper analyzes the timing performance of both SBFF and MBFF in Xilinx Spartan 3E family (XC3s 500 E). These results in favor of Multi-Bit Flip-Flop as reduction of Clock network such as clock buffer and gate delay.

PARUCHURI RAVITEJA 2 L. SRINIVAS
Power decrease has turned into an imperative plan objective for complex outline applications, regardless of whether versatile or not. Specialists have demonstrated that multi-bit flip-flop is a compelling strategy for clock control utilization decrease. The fundamental thought behind multi-bit flip-flop strategy is to kill add up to inverter number by sharing the inverters in the flip-flops. Since the ring counter is comprised of a variety of D-type flip-flops (DFFs) activated by a worldwide clock flag it is conceivable to incapacitate the clock flag to generally DFFs. Such a gated-clock ring counter is actualized to create a low-control first-in first-out (FIFO) memory. In this paper, we will audit multi-bit flip-flop ideas, and present the advantages of utilizing multi-bit flip-flops in our plan. We proposed to utilize twofold edge-activated (DET) flipflops rather than conventional DFFs in the ring counter to split the working clock recurrence. A novel methodology utilizing the Elements rather than the R-S flip-flops in the control rationale for creating

the clock-gating signals is embraced to abstain from expanding the stacking of the worldwide clock flag. The system will extraordinarily diminish the stacking on conveyance system of the clock motion for the ring counter and therefore the general power utilization. A similar system is connected to the source driver and destination driver of the memory part in the postpone support. At that point, we will demonstrate to execute multi-bit flip-tumble approach utilizing gated drive tree by XILINX Design Compiler. Trial results demonstrate that multi-bit flip-slump utilizing gated drive tree is extremely compelling and effective strategy in bring down - control outlines.

U. Soma Naidu¹ , K.Venkateswarlu², Power reduction has become a vital design goal for sophisticated design applications, whether mobile or not. Researchers have shown that multi-bit flip-flop is an effective method for clock power consumption reduction. The underlying idea behind multi-bit flip-flop method is to eliminate total inverter number by sharing the inverters in the flip-flops. Since the ring counter is made up of an array of D-type flip-flops (DFFs) triggered by a global clock signal it is possible to disable the clock signal to most DFFs. Such a gated-clock ring counter is implemented to compose a low-power first-in first-out (FIFO) memory. In this paper, we will review multi-bit flip-flop concepts, and introduce the benefits of using multi-bit flip-flops in our design. we proposed to use double-edge-triggered (DET) flipflops instead of traditional DFFs in the ring counter to halve the operating clock frequency. A novel approach using the C-

elements instead of the R-S flip-flops in the control logic for generating the clock-gating signals is adopted to avoid increasing the loading of the global clock signal. The technique will greatly decrease the loading on distribution network of the clock signal for the ring counter and thus the overall power consumption. The same technique is applied to the input driver and output driver of the memory part in the delay buffer. Then, we will show how to implement multi-bit flip-flop methodology using gated drive tree by XILINX Design Compiler. Experimental results indicate that multi-bit flip-flop using gated drive tree is very effective and efficient method in lower-power designs.

Yarramsetti Ramya Lakshmi¹ , Dr. I. Santi Prabha² , R.Niranjan³, In today's VLSI technology, power is the major issue with shrinking technology. Clock will play important role in the integrated circuits. In this paper, Multi-bit flip flop technique has been introduced to reduce clock power. The idea behind this technique is that clock power savings can be achieved by using multi-bit flip flop cell with optimized design. Recent works have been proposing methods using multi-bit flip flops in standard cell based designs, where single-bit flip flops are replaced by multi bit flip flop cells during logic & physical synthesis. In this paper a comprehensive comparison between conventional flip flop and MBFF implementations of an industrial 90nm design has been done. Sequential circuits has been designed using single-bit flip flop and multi-bit flip flop.

EXISTING MODEL FOR MULTI-BIT FLIP FLOP:

Multi-bit flip-flop structure

In a basic circuit structure, the clock signal is fed into all the flip-flops of anSoC. So improving the clock network (say, reducing the total number of clock buffers used) will improve the overall QoR of the design. To improve the flip-flop clock network, circuit designers have designed the multi-bit flip-flops.

A multi-bit flip-flop is either a 2-input or 4-input flip-flop (**Figure 1**) with same number of outputs. A multi-bit flip-flop consists of more than one flip-flop custom designed to optimize area and power.

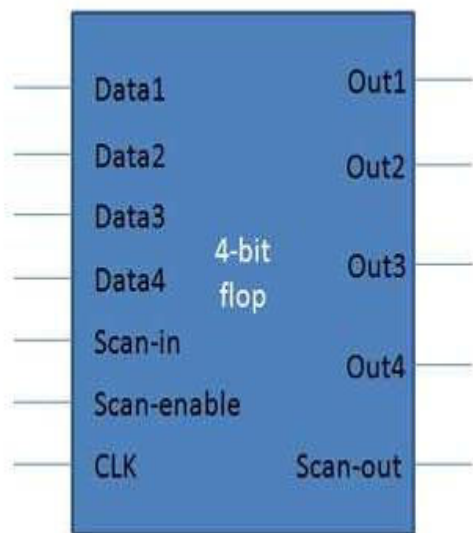


Figure 1. A 4-bit flop

The major structural difference is the shared clock network between all the single-bit flip-flops of a multi-bit flip-flop. Due to this kind of implementation, all the single-bit elements are physically placed nearby, which resolves many physical design implementation challenges.

Figure 1 shows the block diagram of a 4-bit flop and **Figure 2** shows the internal

structure of a 4-bit flop. The in-built 4 flops share a common clock and scan enable. Also, the 4 flip-flops form an internal scan chain of 4 flops and can be plugged as it is forming a bigger scan chain. All these connections are made by hand and are near optimal in terms of use of resources.

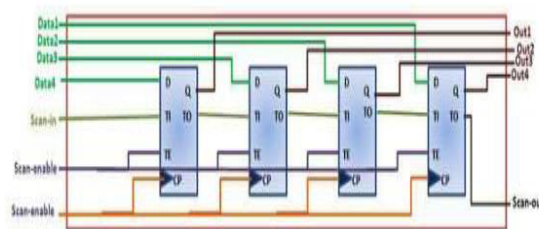


Figure 2: Internal structure of multi-bit flip-flop

Advantages of using multi-bit flop

As stated above, multi-bit flip-flops are a step closer to optimal use of resources and offer many advantages over single-bit flip-flops:

- The SoC implementation using multi-bit cell results in lesser number of clock sinks as seen by the clock-tree synthesis tool. Hence, their usage should result in less power consumption by the clock in all the flip-flops as the overall capacitance driven by a clock net gets reduced.
- This should also reduce clock skew in sequential gates as the clock paths are balanced internally in a whole multi-bit cell.
- The SoC implementation using multi-bit flip-flops should result in smaller SoC area as the total number of clock buffers should reduce, resulting in lesser congestion.
- The multi-bit usage should improve the timing numbers, due to shared logic (in clock gating or set-reset

logic) and an optimized multi-bit circuit and layout from library team.

Comparison of results

We experimented with a small block and ran two experiments, one allowing multi-bit flops and other without using multi-bit flops, at different frequencies in order to compare the pros and cons of using these in our design.

Table 1 shows flop count in the two runs. As is evident from the table, the number of flops is almost half if we allow the usage of multi-bit flops. This approach is not size limited and scales well. When larger numbers of multi-bit flops are used the resulting optimization is even more pronounced.

	Total flop count	MULTIBIT FLOP COUNT	Relative number of sinks
Base library (w/ multibit flops)	15.4K	6.6K	1
Base library (w/ single bit flops)	30.7K	0	2

Table 1: Number of flops/clock sinks with and without multi-bit flops usage

Table 2 shows the timing and power statistics after clock tree synthesis for three different frequencies: 80 MHz, 120 MHz, and 160 MHz. The first row in every category shows the statistics when multi-bit flops were allowed. The lower row shows the statistics of the run without allowing multi-bit flip-flops to be used. We analyzed the design both in terms of timing and power.

The timing was analyzed in terms of Worst Negative Slack (WNS), Total Negative Slack (TNS) and total number of violation paths. Similarly, power was analyzed in terms of internal, switching, leakage, and clock power. The table shows the total number of flip-flops; it also shows total number of multi-bit flip-flops in each case.

Target frequency		Total number of sinks	Number of multi-bit flops	Timing statistics			Power statistics				
				WNS (ps)	TNS (ns)	No of violating paths	INTERNAL	SWITCHING	LEAKAGE	CLOCK	TOTAL
80 MHz	With Multi-bit	15.4K	6.6K	115	0.278	143	21.57	22.85	19.55	14.98	63.97
	W/o Multi-bit	30.7K	0	89	0.125	60	23.44	24.45	19.29	15.64	67.18
120 MHz	With Multi-bit	15.5K	6.7K	178	0.674	350	23.52	25.82	20.97	16.4	70.32
	W/o Multi-bit	30.9K	0	118	0.504	100	26.21	28.92	20.44	17.25	75.57
160 MHz	With Multi-bit	15.5K	6.6K	256	34.98	628	27.42	32.8	18.17	16.82	78.39
	W/o Multi-bit	30.9K	0	427	24.78	319	25.74	28.92	18.56	17.53	73.22

Table 2: Timing and power statistics after clock tree synthesis

PROPOSED CIRCUIT MODEL FOR DESIGN OF MULTI BIT FLIP FLOP:

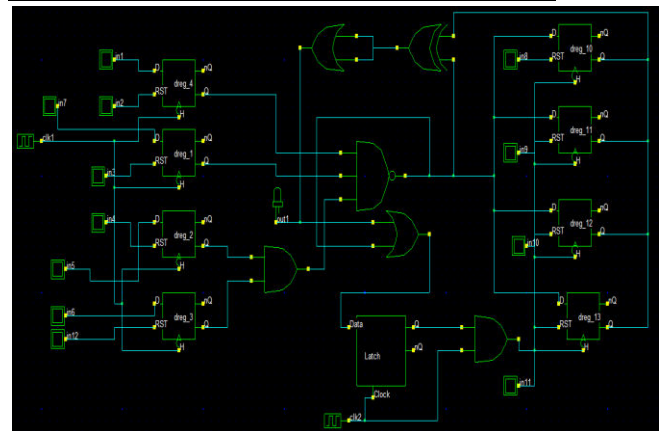


Figure: Representing the Circuit model for MULTI-BIT FLIP FLOP

We consider the present model of the p-spice model for implementation of multi-bit FF design where each output for each register unit is applied to specific input

which would estimate and simplify the correct values from the design circuit model. Now using this model we have proposed a sequential circuit and combinational circuits for implementing the practical application of the desired MBFF for commercial use.

To emphasize the correct power related works utilizing the estimation of the design and its futuristic approach, a novel power optimization method has been applied by incrementing larger MBFFs at the as mention circuit model stage to gain more clock power saving while considering the placement density and timing slack constraints, and simultaneously minimizing interconnecting wire length. By formulating the flip-flop grouping problem as the *m*-clique finding and maximum-independent-set problems, a progressive window based optimization approach is proposed to improve the deficiency.

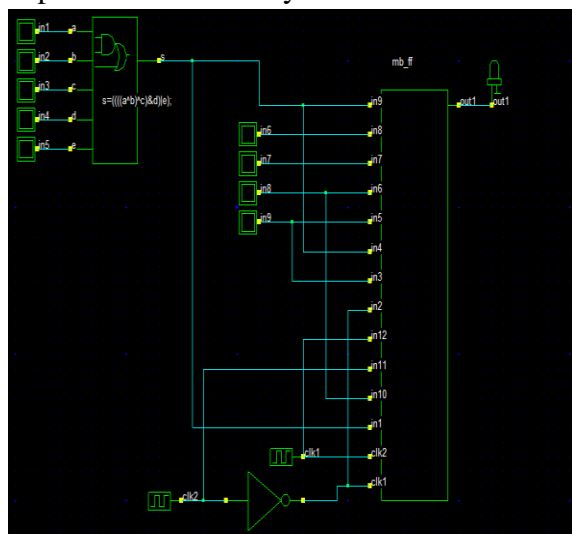


Figure Representing the Combination model for MBFF

Now this model depicts us the particular analysis of the multi bit flip-flop variation of based on the changes in the input combitory logic model. Each analysis is explained and factorized depending upon the input

conditions. The variation of the clock would affect output only if the circuit values for the clock and input condition are set to specific values as shown below:

$F = (a \text{ xor } b \text{ xor } c) \& (d \text{ or } e)$, which is combitory logic output created from K-MAP for SOP or POS.

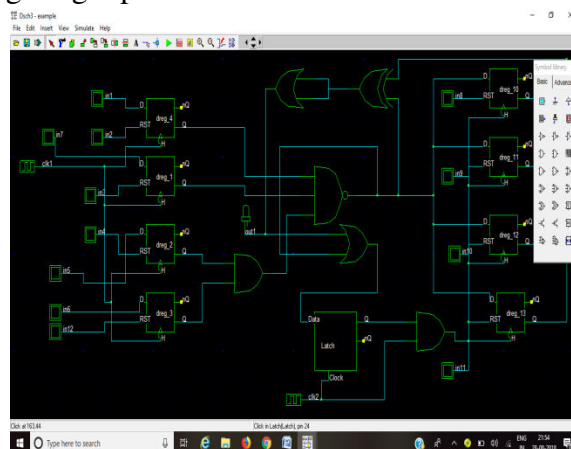
RESULTS AND DISCUSSION:

Simulate for backend:

In the back end design process, we initially design MBFF schematic for DSCH by using micro wind DSCH3 application then observe results are simulated . The desing of MBFF schematic design generated or makes the verilog file and saves as mbff.v file. Observe the size of the MBFF size reduced to still achieve the figure of MBFF.

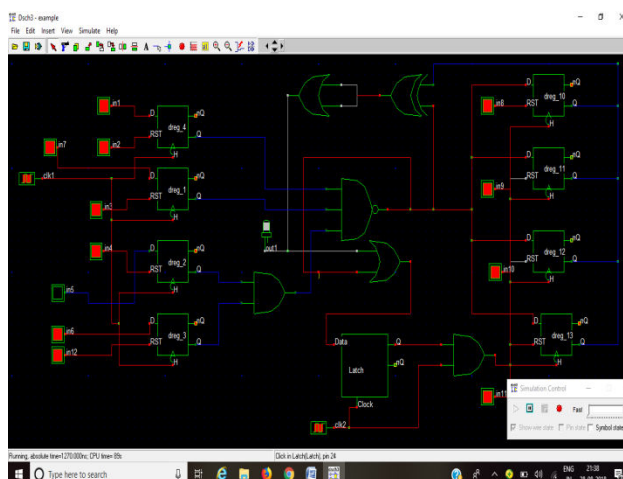
MBFF SCHEMATIC FOR MULTIPLE INPUTS OF THE MULTI BIT FLIP FLOP:

In their initially consider two input 8 d-register ,1 LED,2 input NAND gates,2 input or nor gates ,LATCH,12 input switches and outputs are LED'S. Inputs are read line and outputs are bit line .The below figures multiple inputs of multibit flipflop without giving inputs.



1. Figure for simulation of multiple inputs of multibit flipflop without inputs

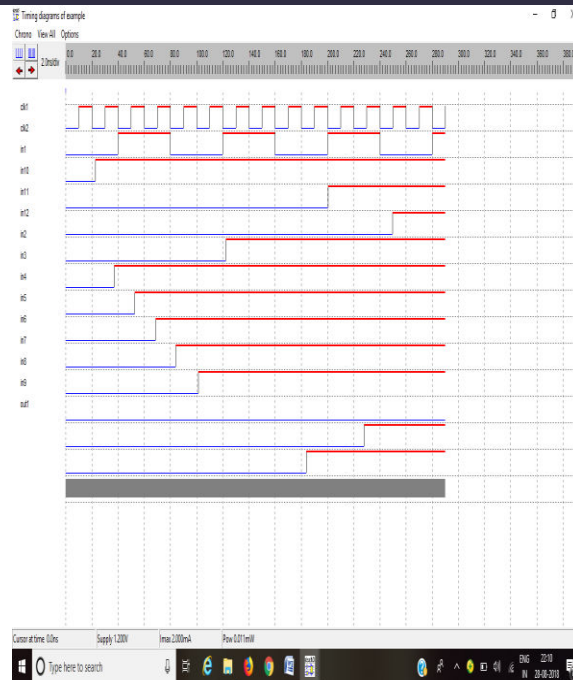
In the above D-registers which are connected in back to back and it act as latches. In this circuit input is wordline(input 1-12)high, then bit line (output 1)high. The Bitline~bitline in the wordline is high.so it performs the read and write operations circuit.



2. Figure for the simulation of read and write operation outputs.

TIMING RESULTS FOR MULTIPLE INPUTS MULTIBIT FLIPFLOP:

In the fig 3 we can see the inputs and output results of RTL schematic design for the multibit flipflop. In there inputs 1 is 0 or low at the time no operation will be operated in the circuit.It,s just hold the data initially in the d-registers and the inverters acts as inputs. Input line is 1 or high then output bit line also high, input is 01 then output is high ,then input is 0 or low then bit line(out 1) is also low. So circuit is fully activate state. The bit line is high so this performed write operation, the bit line is also read operation ,and word line is high or 1 then circuit is performed Read_Write operation .As shown in the timing diagram of the multiple inputs of the MBFF.



3. Figure for simulation of timing diagram for multiple MBFF

In analog simulation of multiple MBFF:

In these mbff we are using 12 inputs and LED output, these simulations

$I_{dd} \max = 1.519mA$,
 $I_{dd} \text{avg} = 0.424Ma$, $V_{dd} = 12.01 \text{ volt}$, $((N18 \times 2) = 0.000Ma)$

Power=0.509mw

Figure for simulation of MBFF of capacitance outputs

Bit # of Flip-Flop	Power	Area
1	100	172
2	172	192
4	312	285

COMPARITION TABLE FOR 4 BIT FLIP-FLOP

Parameters	Existing system	Proposed system
Area	285mm ²	105mm ²
Power	0.285mw	0.155 mw
Delay	5.87 ns	1.45 ns
V _{th} (Threshold Voltage)	1.1V	0.6V

CONCLUSIONS

Current, we have introduced a new problem formulation of post-placement power optimization with multi-bit flip-flops. We have also proposed our algorithms to solve the addressed problem based on the progressive window based optimization with the considerations of both placement density and interconnecting wire length. Experimental results based on the industry benchmark circuits have shown that our approach is very effective and efficient, which is capable of incrementally merging existing MBFFs in the design to gain more power saving.

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