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FAULT DETECTION ANALYSIS USING PSEUDO EXHAUSTIVE PATTEREN GENERATION IN TESTING

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ABSTRACT:
This project presents a new method for pseudo exhaustive testing of standard array multipliers using a novel approach of data-controlled segmentation of the circuit. The method covers both combinational and sequential fault classes. Differently from previous papers, the proposed separate cell testing approach targets multiple faults in different cells and avoids fault masking. The method is also applicable to other multiplier architectures like Booth and Mini MIPS with high stuck-at fault (SAF) coverage. The regular structure of the test allows efficient implementation of the method as both software based self-test (SBST) and hardware-based BIST.

I. INTRODUCTION
BIST is a course of action for-testability structure that spots past what many would consider conceivable physically with the circuit under test (CUT). The basic BIST building requires the improvement of three mechanical assembly squares to an automated circuit: a test structure generator, a reaction analyzer, and a test controller. The test plan generator makes the test structures for the CUT. Wide and pseudo concentrated test plan generators outfit high issue thought with least number of test structures and without turning reenactment. Pseudo wide testing disposes of the need of deterministic test system age. For this condition, the pseudo raised the target can be reformulated is such way that the nbit space is ensured if for all n – k+ 1 flanking k-bit subspaces, most by a long shot of the 2k models happens at any rate once. Pseudo clearing testing is demonstrated to be gainful by iterative point of confinement packs (ILAs). ILAs are structures including not especially delineated framework for theory cells, related in standard way. These days present day VLSI circuits, containing an enormous number of transistors by utilizing a relative BIST plan generator to test past what one module would separation have the choice to down the contraption cost. A standard pseudo veritable two-plan generator makes a (n,k) – pseudo genuine two-structure test for any estimation of k, by drawing in an information signal P[k], $1 \leq k \leq n$. The nonexclusive pseudo wide two-plan generator can be summed up into dynamic two-structure generator that makes all (n,k)-pseudo wary two-structure test vectors for

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all estimations of k. This system is called as recursive pseudo wide two-structure age. In recursive pseudo cautious testing, (n,k)-PETS are made for all k= 1,2,3,… ..,n. By the usage of a mix of XOR portals and enabled counter we can recursively make all (n,k) pseudo complete test structures for k ≤ n in unimportant time. Progressively observable bit of Built-In Self-Test systems go for combinational deficiencies, i.e., blemishes that can be dependably watched utilizing a particular test plan. Testing for deferral and consecutive blames requires two - plan tests. The test structure generator in proposed BIST circuit makes two models.

Existing Method:

Augmentation is the most standard errand utilized in enduring figurings. Multipliers are displayed in information way models of standard microchips, DSPs or SOC. In chip, Software-Based Self-Test (SBST) approaches are completely utilized. Regardless, the test endeavors should be outfitted with beneficial information (operands) for testing the multipliers. In conditions where the multipliers are brought into always basic complex circuits, are less controllable and recognizable, capable Built-In Self-Test (BIST) plans are required.

Proposed Method:

In this paper, we build up another methodology for testing pack multipliers, which joins PET with deterministic test to accomplish standard test structures, draw in synchronous and parallel testing of highlight cells, and to cover wonderfully sweeping classes of issues including dynamic flaw types like CMOS stuck-opens (SOP) and yield issues.

II. TEST PATTERN GENERATOR

Two test structure generators like Generic Pseudo Exhaustive Two Pattern Generator (GPET) and Recursive Pseudo Exhaustive Two Pattern Generator (RPET) are enveloped with lesser mechanical get-together use.

1. PSEUDO EXHAUSTIVE TWO PATTERN GENERATOR

A standard pseudo-wide two-structure generator is a module with 7 bit information (PE[7:1]) and 7 bit yield (A[7:1]) that can pass on a two-plan (7,k)- pseudo-raised test set for any estimation of k , (k ≤ 7). The nonexclusive pseudo-broad two-structure generator is appeared in Figure 1. It unites a 7-engineer gatherer, containing a snake and a register (the pass on in sign of the snake is driven by the yield of a module named pass on generator, or c_gen for short), a 7-sort out nonexclusive counter, and a control module..

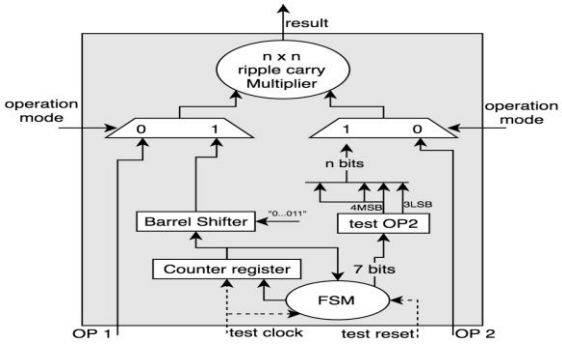

FIGURE 1: Generic pseudo-exhaustive two pattern testing

At each time most exceptional one of the PE[i] sign is affirmed. Legitimately when PE[i] 1≤ I ≤ 7 is checked, by then a (7, k-1)–pseudo-clearing two-structure test is passed on. For instance, for n=7, Table 1 demonstrates the pseudo-complete test set passed on for each estimation of the PE[i]

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signals. In Table 1, in the focal zone the estimation of the PE[k] sign are appeared; in the second area the made pseudo-sweeping tests are exhibited, while in the third part the level of the mindful subspaces are appeared.. For instancein the fourth bit of Table 1, where PE[4] is confirmed, a (7,3)- pseudo-clearing test set is passed on and 3-bit cautious test set is related with the 2 packs A[3:1] , A[6:4] and a singular piece test set is passed on at A[7] . In case the size of the pseudo-extended test set does in no way, shape or form at all, in any way shape or form, using all techniques, at all most fantastic by 7, by then the degree of bits is dissipated into [7/k] get-togethers of k bits, that take close properties and the remainder of the (7 mod k) over the top intrigue bits have in each supportive sense hazy traits with the (7 mod k) low-demand bits of the low-demand parties. For example, for k=4, the A [7:5] bits of the yield of the generator have close qualities with the A [3:1] bits. As necessities be, if a wide k-bit two-plan test is passed on at the low-demand bits of the yield of the generator, by then a (7,k)–pseudo-concentrated two-structure test is made at the yields of the generator.

Fig. 1 shows the implementation of the proposed method as BIST. The circuit consists of a Finite State Machine (FSM) with 11 states (according to 11 A-patterns) which controls the test process. The extended version of FSM for testing sequential faults consists of 15 states. The A-atterns are loaded directly from the FSM, replicating the 4-bit groups (a2,a3, a4,..., a5)for all of the next higher 4-bit groups, while a barrel shifter which is shifting predefined values loads the B patterns.

An ”operation mode” signal can switch the multiplier from normal mode to test mode by utilizing two multiplexers. is well suitable for BIST. Added 1 extra input and (n-1) OR gates into the multiplier (PET + DFT) allows to achieve 100% SAF coverage. A hybrid test using PET with additional ATPG generated deterministic test patterns (PET + DET) guarantees as well 100% SAF coverage, but without any change in the multiplier, and therefore is well usable for SBST.

III. RESULTS AND DISCUSSIONS

The yield waveform of all the individual modules and the waveform of Generic and Recursive pseudo wide two model generator

The Generic Pseudo-Exhaustive two-pattern generator modules:

The responsibility of the 7-engineer nonexclusive counter can't swear off being counter reset (C_reset), 7 bit sign PE[7:1] and counter disable(C_clk_disable).If the sign PE[1] is imparted, by then the standard counter fills in as a 7-sort out twofold counter. Right when PE[4] is checked, by then the standard counter fills in as two 3-bit subcounter and a 1-bit sub counter from LSB. In like manner, the standard counter makes all 2k-1 × (2k-1 - 1) mixes to each and every get-together of k-1 neighboring bits. Unequivocally when the sign C_reset is affirmed in, the nonexclusive counter checks from the key worth. The sign C_clk_disable is used to keep the counter moderate. The C_gen is used to give the Cin commitment concerning the snake. The commitments of C_gen module are PE[7:1] and Cout[7:1]. If the sign PE[4] is checked in, the Cout[4] is given as a Cin. In light of the sign PE[7:1] the estimation of Cin changes

The control module is used to find that a k–structure two-structure test is made at the k low-demand bits of the generator. The information indication of the control module are reset, ACC[7:1], C[7:1], PE[7:3], and makes the sign C_clk_disable, C_reset, A_reset0 and end_k_bit_test.

The obligations of snake are cin, A[7:1], C[7:1] and its yields are C_out[7:1], A[7:1]. It joins 7 full adders, the pass on yield of the full adders are caused to the going with full adders as pass on data. On the off chance that the estimation of k is viewed as 3, by then very far as two 3-plan sub master and one 1-make gatherer.

The pass on yield of each sub gatherer is given to the pass on duty of next sub ace. On the off chance that there is any pass on in the third piece, by then it is added to the most diminished referencing bit of the snake yield.

IV CONCLUSION

Clearing and pseudo attentive test plan generators give high issue thought least number of test structures and without need increase. Pseudo wide testing killings the need of deterministic test game-plan age. In current VLSI circuits, containing inconceivable transistors, the utilization of an adjoining BIST structure generator for testing past what one module can drive down the gadget overhead, developing the fittingness of the BIST thought. Modules whose information sources are driven (during BIST) from a relative model generator may have unequivocal cone sizes. Recursive pseudo wide testing has been proposed as a reaction for this issue; in recursive and nonexclusive pseudo concentrated generators for the zone of stuck-at issues have been proposed. In this paper we have shown a two-structure age plot that can make both nonexclusive and recursive pseudo sweeping tests; with this course of action, more than one circuit under test, maybe having unmistakable cone sizes (k) can be tried in parallel. Associations of the proposed course of action with plans proposed as of now to recursively make pseudo genuine one-structure tests fittingly extended to pass on two-structure tests, reveal that the proposed blueprint makes the recursive pseudo complete two-structure tests with lower gear overhead.

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