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Design of Low Power Optimizing Chien Search Usage in the BCH Decoder

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Abstract:
In this a new power-saving chien search (CS) structure is proposed for parallel Bose-Chaudhuri-Hocquenghem (BCH) decoder .The CS plays an important role in identifying the areas of error in syndrome-based decoding, but incurs a huge waste of exhaustive computation power consumption. In this proposed architecture, the process of searching for the binary representation of the matrix is decomposed in two steps. The first step is accessed every cycle, but the second step is activated only when the first step is successful, this will result in remarkable power saving. Here an effective construction is presented in a two stage process to avoid an increase in the delay of the critical path. Experimental results of the proposed two-step structure for the BCH (8752, 8192, 40) code that saves 50% power consumption compared to a conventional building of the show.

Keywords:
Bose–Chaudhuri – Hocquenghem (BCH) codes, Chien search (CS), low power, two-step approach.

INTRODUCTION:

Communications and storage systems for various error correction codes are used to recover the corrupted code words, Bose-chaudhuri-Hocquenghem (BCH) code [1], [2] is the most widely used due to its powerful error correction performance and affordable hardware complexity is one of the algebraic signs. Binary BCH code is a solid-state storage such forward [3], [4] and optical fiber communication systems [5], most of the applications and the never-ending demand for high through put decoding has been running ever larger error- correction capability of different systems.Satisfying the huge computational capacity of high through put and strong error correction is inevitable, therefore, becomes more and more important power saving structure of the BCH decoding. In general, a BCH decoder to correct the bits T at the peak of the three main blocks, namely, the syndrome calculation (SC), the key-equation solving (KES) has, and Chien search (CS) [1], [2]. Receiving a code word for a given R (x) Compute syndromes SC 2T and KES (X) using the syndromes of the error locator polynomial Λ. Finally, the error is E (X) Λ sources (X) CS determined by the algorithm is based on the finding. In a parallel BCH decoder, CS main cause of power consumption and total electricity consumption [6] and can take up to a half. Numerous studies have demonstrated the ability to reduce the power consumption of CS proposed structures. Early termination of the methods presented in [6] and [7] After finding an error in the past to eliminate redundant computations. An additional error counter is incremented when an error is found, and the counter KES down sides found in the CS is turned off matches. BCH decoder dealing with a small number of errors early in the implementation of the common and effective drug, though, when the power saving small insignificant error

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correction capability. [8], is a more effective method in order polynomial reduction (POR) when the error was found in the error locator polynomial of the proposed reform. Locator polynomial order one at a time, errors are detected by the decline and eventually becomes zero. POR [8] at a time, gradually power down circuitry associated with a polynomial factor makes it impossible for the CS. POR for serial BCH decoders are successful, however, because it is difficult to apply the technique of complex polynomial update parallel architecture. Further more, all of the previous power saving algorithms, including early termination, [6], [7] and the POR [8], depending on the position of the errors. For example, if faults at the end of the term of the code, as in the case of power savings is significant that in the beginning of errors. In this brief, we have a new approach, which is parallel to the CS proposed two stages of decomposition. In order to have access to each of the first step, but the first step to access the second stage will be activated only when a less successful result. The proposed two-step method [9] that is conceptually similar. The two-step approach, in general, lead to an increase in the critical path delay and delay, the losses can be solved simply by employing an efficient pipelined architecture. Unlike previous architectures [6] - [8], regardless of the error, the location of the proposed construction of the power consumption can be saved. Digital communication system for carrying the signal from the source to the destination user via a communication channel is used to transfer data. All the code words encoded, encoder, which generates a set of code word. When it becomes a code for the actual set of data encoded. Memories of errors and data corruption is a significant problem in the channels. Disorders that affect one or more of the memory cells of radiation-induced soft errors, for example, have been known to change their values. Other types of failures cause permanent damage, such as the device will no longer provide the correct data. In the event of failure to ensure that the data is not corrupted, error correction codes (ECCs) are widely used in memories [1]. To add some extra parity bits to check every memory ECCs word in such a way that errors are detected and corrected. The proposed system is basically sound channel .Parity describes the additional bits of memory for its ability to reduce data corruption. There are other costs introduced by the ECC encoding and decoding circuitry. More than one channel to transfer the data to be encoded and decoded as read from it also affects the circuit delay. In many cases, because many of the steps of the encoding, decoding speed is much more complex and ECC [1] .Traditionally single error, double error detection (SEC-DED) codes used to protect memories are limited [3]. But the data signal error was found and corrected in the proposed system for multi-byte. This point of view as well as the delay in the performance of RS code symbols in the number of bits of memory modules and devices when the matches will be very attractive for the channel, a device that can be corrected failures. In fact, the main reason is usually used to protect the RS codes A code word for a certain polynomial coefficient of the polynomial, the generator polynomial g (x). Reed- Solomon error correcting codes (RS codes) to transmit a wide array of possible errors arising from error to restore data from a disk and data communication systems used for storage. There are two types of errors when the bits flowing from one point to another, they are subject to change because of the unpredictable interference. Change the shape of the interference signal. from 1 to 0

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or 0 to more bits of data per unit of linear 1.Reed Solomon code means that the cycle has turned into a regular non-binary block code. Redundant encoder signals and message signs are included in the product using the generator polynomial. Decoder error location and intensity are calculated using the same generator polynomial. Then the correction is applied to the received code. Reed- Solomon coding, plus data storage and retrieval systems (noise channel harm) forward error correction of a type used for data transmission.

LITERATURE SURVEY:

A large number of errors, because they have the ability to correct the error correction described in this paper basically memory devices, the memory is used for the applications important to the majority logic decodable codes. However, the performance of the memory they need to have a big influence the decoding time. Technical standards, in memory devices become larger and more powerful error correction codes are needed. Euclidean geometry to overcome the problems in this paper as they use more modern codes. These codes can correct a number of errors, but usually requires complex decoders. Serially with the majority logic decoding circuitry can be implemented in a very simple, but it requires long periods of decoding. Memory, this is an important parameter for the access to the system can increase the time. Increase the size of the code, so the majority of the increase in the time of decoding the decoding logic (implemented serially), N iterations required. EG-LDPC code, the code word is used in this method (Euclidean geometry -Low Density Parity Check), there is a majority One Step Logic Decodable code. It uses the algorithm to check the code. There is nothing to check the algorithm, but code word is associated with a numerical value to be transmitted. The receiver then receives the code word at the end of the numerical values associated with the error identification is a comparison of some numerical value.There. The method is easy to implement using existing hardware. This method is more time for decoding. As well as the power consumption and the need for the region are high. One step is to identify the shortcomings of the majority of serially MLDD serial technique uses Logic decoder. [2] In this article, the author of the noisy channel (Additive White Gaussian Noise) in the presence of PSK and FSK modulation techniques Reed Solomon code (RSC) of the bit error rate (BER) on performance analysis explains. In this paper, 32- FSK (frequency shift keying), PSK (phase shift keying) modulation coded communication system is used for the simulation. In addition to the use of Monte Carlo simulation and calculation of the rate of BER MATLAB / SIMULINK is done using the tool. The results are shown using BERTOOL. In order to compare the performance of the block length is fixed, we have taken a different code rates. After getting familiarized with the classification and characteristics of forward error correction codes, error detection and correction codes described in this section are compared to some. Hamming code - a Hamming encoder bits of parity bits are inserted into the message. The parity bits and parity bits of data to determine the different combinations to impose a fixed parity. The combinations are fixed parity check decoder. The parity bits are set according to the decoder. The combination of the binary equivalent of the error location is determined. OK, that particular bit of data that is being flipped. Hamming code in the same error code. If any of the attempted correction of double errors can be detected.

• Berger code - Unidirectional Berger code error detection code. It can only detect an error in either '1' flipped '0' or '0' flipped '1', but it means the same code. '1' are designed to detect errors with a "0", the binary equivalent of the message, then the message is sent by the number of 0s and flipped over. The invention of the '0' design '1', an error message, the binary equivalent of the number of 1s and sent along with the message, as well as when it flipped. According to the decoder to receive the binary 0s or 1s compares the number of the same design. Imbalance between the two indicates an error. It is expected to be used where the error is unidirectional.

• a valid code word in the code has always been a constant weight, constant weight code. It means that a valid code word of a fixed number of 1s. Therefore, any variation indicates an error. Multiple errors can cancel each other out as a simple but effective way of encoding it.

• Code of Ann M - An encoder message out in an M-M number of 1s in an n bit code is mapped to a word. An M-1s in the code message bits which are used to adjust the number of bits added to the number of additional M. It consists of all the M bits of the message in any 1s '1' will. It is also effective in terms of the code of coding rate.

• Erase Code - to erase the error means that you know in advance from the previous experience of its location. Erasure code is to be able to correct such errors. It is already known that this type of code is not required in the decoder circuit fault locator. Only to correct an error in the decoder is calculated by measuring the eraser.

• low-density parity check code - the low density parity check code is a linear block code. The message block is transformed into a code block by multiplying the transformation matrix. The name refers to the low density and low density transform matrix. This means that the number of 1s in the transformation matrix less. It's a lot of coding gain, but the encoder and decoder design is concerned, the best code is complicated. Mainly used for Digital Video Broadcasting.

• Turbo code - it is a convolutional code. Convolutional encoding, encoding normal. It is defined by the (n, k, l) n the number of bits input to the Turbo code, k and l is the number of output bits is the memory of the encoder. Decoding takes place in two stages. The first stage will be a hard and soft decoding step decoding. This is a very good error correcting capability, which means that there is no coding gain. The main drawback is that it has a low coding rate and high latency. Hence it is not suitable for many applications. Satellite communication latency due to distance, but also the lowest in the extra latency is too high. Hence it is mainly used in satellite communication.

• Reed Solomon code - Reed Solomon code of a nonbinary block linear cyclic code sequence. Redundant encoder signals and message signs are included in the product using the generator polynomial. Decoder error location and intensity are calculated using the same generator polynomial. Then the correction is applied to the received code. Reed Solomon code and turbo codes, LDPC coding gain is relatively low. But it is a very high rate and low complexity of coding. Hence it is suitable for many applications, including storage and transmission.

REED-SOLOMON CODES:

A Reed-Solomon (RS) code described in a paper in 1960, Reed Solomon error-correcting code is a rst [9]. Since that time they are CD-ROM, wireless communications, space communications, DSL, DVD, digital TV application. RS encoding of the data is relatively

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straightforward, but the decoding of the 1960s and other major e ciency improved by Berlekamp, time consuming [2, 5, 6, 8]. RS only in the last few years, it has become possible by using the high-bandwidth data to count. Groups of bits instead of one bit at a time, that it is a gesture from the Hamming code of RS ERS. We are the groups of digits \ Call "(the \ icons" or \ Co cients ") is. If a digit is error-free in all of its bits are error-free only. For example, if an 8-bit character in a number, and the same error in three bits of impersonation we are number one is damaged. the following example is damaged two digits (but not more than two corrupted bits) that count

Original : 10110001 11011111 01001011
0101110
0

Received
: 10110101 11011111 01110001
0101110
0

Corrupted
? yes no yes no

If we want to send a k digit plaintext message, RS will send n = k + 2s digits, and guarantee that the correct message can be reconstructed at the other end if there are fewer than s corrupted digits. An example of commonly used parameters: k = 223, s = 16, n = k+2s = 255, giving the ability to correct 16 corrupted digits out of every 255 digit packet. In general, the number of bits in a digit and the parameters n and s are tuned to optimize for your application. A CD-ROM can correct a burst of up to 4000 consecutive errors.

PROPOSED TWO-STEP CS ARCHITECTURE:

In the proposed architecture paraell CS is decomposed int two steps.The p-parallel CS examines p error positions at the same time, each of which generates a binary matrix of 1 x m representing a Galois field (GF) element by computing

$$Y(\alpha^{wp+i}) = \sum_{j=1}^{t} \mathrm{FFM}_{ij} = \sum_{j=1}^{t} \Omega_j A_{ij} = [\Omega_1\ \Omega_2 \cdots \Omega_t] \begin{bmatrix} A_{i1} \\ A_{i2} \\ \vdots \\ A_{it} \end{bmatrix} \quad (5)$$

Where i ranging from 1 to p. The CS will examines and determines the presence of an error when Y (αwp+i) is 1, where αwp+i is a root of the error locator polynomial.The main idea comes from the fact that the absence of errors is guaranteed if some bits ofY (αwp+i) are not equal to those of 0(m−1:1)1(0).In the GF of dimension m, the multiplicative identity element, α0 or α2m−1, is defined as 1, i.e., 0(m−1:1)1(0), more precisely In the case of GF(24), for example, no presence of errors is guaranteed if Y (αwp+i)(3:2) _= 0. Like this two-step approach is employed for early detection.This wil results in remarkable power saving.

SIMULATION RESULTS:

CS low power, depending on the size of the field of construction of the proposed two step different configurations, and error-correction capability of the horizontal factor compared to traditional construction. At the operating frequency of 200 MHz for all the CS blocks with a 130-nm CMOS technology is, and equally probable error model [7], [8] adopted simulations power consumption. More precisely, V errors BCH (n, k, t) signals, the average bit of a distance between two adjacent errors n / V model, every bit of the code word received is from the same error occurs when the reference is corrupted.

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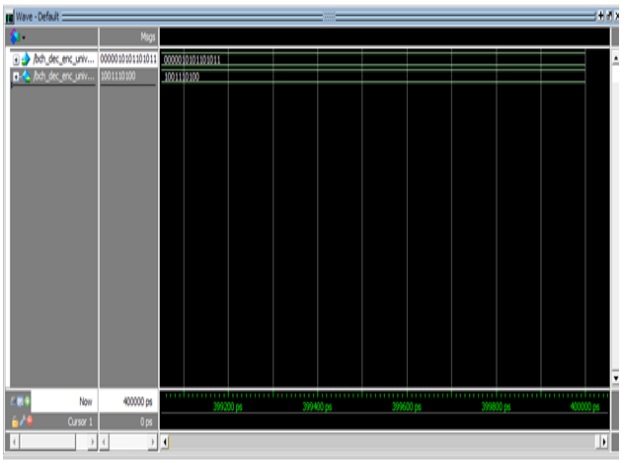

Fig: Chien search based BCH codes

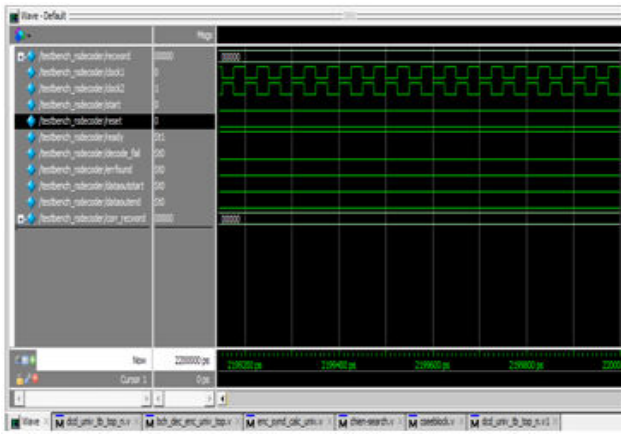

Fig: Chien search for RS decoder

SEC-RS code testbench waveforms shown in below two figures

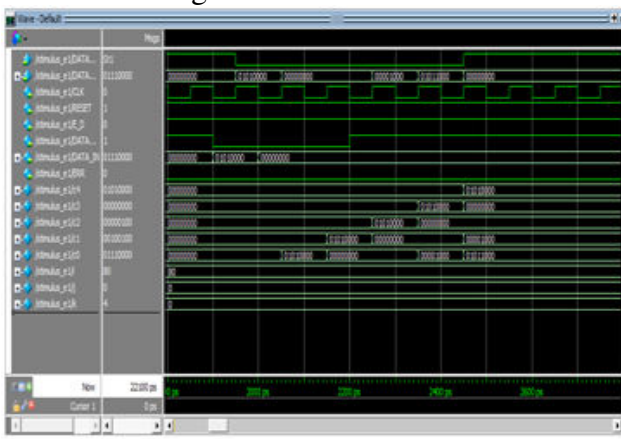

Fig. The size of the field in the first step of the bit width of 4 and shows the effect of energy saving ratio.

For fair comparison, all of the BCH codes to model the rate of 0.93 is designed and shown in Fig 8. Set the horizontal element. 4, the proposed increase in the size of the field of development becomes even more important as a result of the construction, and a small number of bits are sufficient in electricity savings increase. For example, BCH for the proposed two-step structure (8752, 8192, 40) GF (214) 49.3% power, savings over the code FFM partial opening of the first four MSBs will be processed. Moreover, Figs. 5 and 6 horizontal error correction factor and illustrate how it affects the efficiency of power saving. The horizontal element increases, the energy savings and the horizontal aspect ratio closer to 50% than the energy saving ratio of 8. It is error correction capability is almost independently shown to be saturated when. In figs. 3-6, we estimate an offset between energy savings and in spite of the simulation, a simplified energy model (9) can be used as a good
estimate. Due to the additional buffers are addressed in Section III, the proposed construction of an approximately 10% increase in hardware complexity.

CONCLUSION:

By reducing access to the second stage of the conventional CS to achieve significant power savings is decomposed in two steps. Error operate under the same ownership, the less energy the size of the CS in the construction sector in different configurations, and error-correction capability of the horizontal factor compared to traditional construction. From the experimental results, the proposed construction of a 50% reduction in power consumption compared to the conventional horizontal CS show. Power saving horizontal factor or increase the size of the field will become more and more important.

Reed- Solomon codes, such as the proposed two-step CS also applies to other linear block codes.

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