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A NEW PROBABILISTIC ERROR MODELING FOR APPROXIMATE ADDERS

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ABSTRACT
Approximate adders are widely being advocated as a means to achieve performance gain in error resilient applications. In this paper, a generic methodology for analytical modeling of probability of occurrence of error and the Probability Mass Function (PMF) of error value in a selected class of approximate adders is presented, which can serve as performance metrics for the comparative analysis of various adders and their configurations. The proposed model is applicable to approximate adders that comprise of sub-adder units of uniform as well as non-uniform lengths. Using a systematic methodology, we derive closed form expressions for the probability of error for a number of state-of-the-art high-performance approximate adders. The probabilistic analysis is carried out for arbitrary input distributions. It can be used to study the dependence of error statistics in an adder's output on its configuration and input distribution. Moreover, it is shown that by building upon the proposed error model, we can estimate the probability of error in circuits with multiple approximate adders. We also demonstrate that, using the proposed analysis, the comparative performance of different approximate adders can be correctly predicted in practical applications of image processing.

Index Terms—Approximate computing, Adders, Probability of error, Probability Mass Function (PMF), Image smoothing, Modeling, Arithmetic, Analysis.

I. INTRODUCTION
Optimizations in VLSI have been done on three factors: Area, Power and Timing (Speed).Area optimization means reducing the space of logic which occupy on the die. This is done in both front-end and back-end of design. In front-end design, proper description of simplified Boolean expression and removing unused states will lead to minimize the gate/transistor utilization. Partition, Floor planning, Placement, and routing are perform in back-end of the design which is done by CAD tool .The CAD tool have a specific algorithm for each process to produce an area efficient design similar to Power optimization. Power optimization is to reduce the power dissipation of the design which suffers by operating voltage, operating frequency, and switching activity. The first two factors are merely specified in design constraints but switching activity is a parameter which varies dynamically, based on the way which designs the logic and input vectors. Timing optimization refers to meeting the user

constraints in efficient manner without any violation otherwise, improving performance of the design.Quantum-dot cellular automata (QCA) are an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. Quantum-dot cellular automata (QCA) which employs array of coupled quantum dots to implement Boolean logic function. The advantage of QCA lies in the extremely high packing densities possible due to the small size of the dots, the simplified interconnection, and the extremely low power delay product. A basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. If two excess electrons are placed in the cell, Coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations can be labeled logic "0"and "1".The basic building blocks of the QCA architecture are AND,OR and NOT. By using the Majority gate we can reduce the amount of delay.i.e by calculating the propagation and generational carries.

2. EXISTING METHOD:

As the computing systems, involving high complexity arithmetic, become increasingly embedded and mobile, the concern for energy efficiency, size and speed of these systems also accrues. Approximate computing is an emerging trend in hardware and software design that exploits this inherent tolerance for inaccuracy for efficiency gain in terms of required hardware, speed and/or power. Unlike the low-power approximate adders, most of these these high-speed, low latency approximate adders exploit the fact that the carry propagation chain for most input combinations is shorter than that for the worst case. Traditionally, the error performance evaluation and comparison presented for these adders relies on computer simulations, which can only be executed exhaustively for small-sized adders.As the processing frameworks, including high unpredictability math, turn out to be progressively installed and portable, the worry for vitality effectiveness, size and speed of these frameworks additionally collects. An expansive number of such applications include media handling, for example, picture, video and sound based applications intended for human interface. Other such computationally escalated applications incorporate information mining and machine learning. A typical element in these applications is that they don't require the result to be completely exact, rather a surmised result is satisfactorily worthy. Surmised figuring is a developing pattern in equipment and programming outline that endeavours this characteristic resilience for mistake for effectiveness pick up as far as required equipment, speed and additionally control. A few practically rough plans for essential number juggling squares including adders and multipliers have been proposed. The outline of quick and proficient adders has pulled in extraordinary consideration in the rough processing area. Not at all like the low-control rough adders, a large portion of these fast, low latency surmised adders abuse the way that the convey engendering chain for most information mixes is shorter than that for the most pessimistic scenario.

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Some unmistakable cases of these elite adders are: mistake tolerant adders (ETAs) relatively remedy snake (ACA-I), variable dormancy theoretical viper (VLSA), precision configurable snake (ACA-II), effortlessly corrupting viper (GDA) and bland exactness configurable snake (GeAr). Another sort of surmised adders are low-control adders, exhibited in. Keeping in mind the end goal to choose a suitable estimated viper for a given application, similar execution of the accessible outlines must be thought about. The outlines specified above have been assessed and looked at as far as basic way delay, required equipment and power assets and mistake insights. Generally, the blunder execution assessment and examination exhibited for these adders depends on PC reenactments, which must be executed thoroughly for little - measured adders.

3. PROPOSED METHODOLOGY:

The analytical model for probability of error provides an accurate measure for accuracy comparison of a wide variety of approximate adders. In order to compute the exact probability of error, we need to simulate the adder for all possible input combinations. It facilitates comparison among arbitrary bit width approximate adders without the need of time-consuming simulations, which are always required to evaluate performance metrics used in existing works. Using the models developed by the methodology, the error statistics can be expressed as functions of circuit parameters, like number of input bits, carry chain length, number of overlapping prediction bits and number of sub-adders. Hence they can provide insights into the relationship between circuit specifications and error statistics, which can help the circuit designers, choose circuit parameters according to application requirements.

Carry-in is propagated by an n-bit addition when all n pairs of the input bits are propagating. This happens when the values of bits in every pair of addition arguments are unequal. When every pair of bits satisfy this condition, the carry-out will be equal to carry-in and the sum will be equal to 2 n − 1. Hence, the probability of carry-in propagation by adding X and Y is given as follows: Pr[P; k1, k2] = pZ(2n − 1) where Z = X + Y and pZ(k) = pX(k) ∗ pY (k). Pr[P; k1, k2] denotes the probability of propagation event for given k1, k2, indicating that pX and pY depend upon the bit locations k1, k2. In case of uniformly distributed inputs, probability of carryin propagation is evaluated by using k = 2n − 1 in Eq.

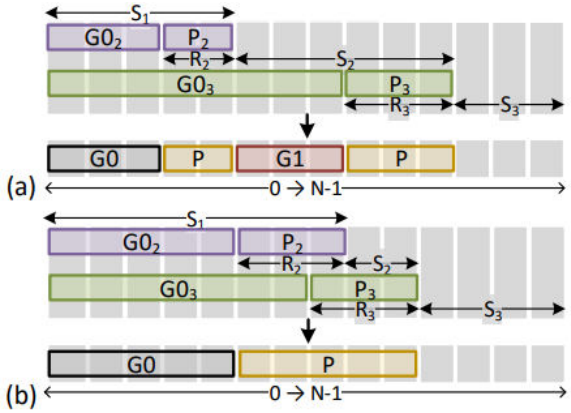

Fig.3.1. Error value in case of simultaneous error.

It was observed via simulations that if the approximate adders are cascaded, then the individual bits in the output of adders. Still remain approximately uniformly distributed. This is because sum from every single full adder can be 1 or 0 with equal probability.

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They are not exactly uniformly distributed because of the occurrence of error. However, since the occurrence of error is infrequent in most adder configurations, we found that the distribution of output bits is going to be very close to the uniform distribution. Thus the probability of error models remains approximately the same for every approximate adder and they can be applied by considering each adder as an independent component.

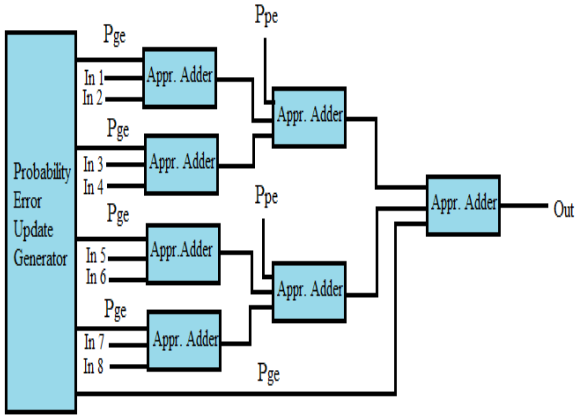

Fig.3.2. Circuits with multiple approximate adders.

6. SIMULATION RESULTS

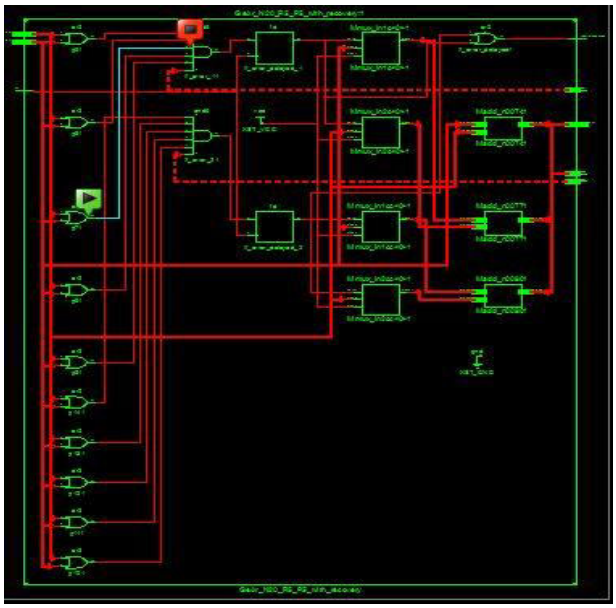

Fig 6.1 Schematic Diagram

Fig 6.2 RTL Waveforms

5. CONCLUSION

In this paper, a generic methodology for probability of error analysis of approximate adders is presented. The methodology can be applied to calculate exact probability of occurrence of error and the PMF of error in any configuration of the adder model presented for given input distributions and hence these configurations can be reliably compared without the need of exhaustive or Monte-Carlo simulations. The analytical models also yield insights into the dependence of error performance on circuit parameters. Models for some configurations are verified through exhaustive simulations and simulation results are shown to be in perfect agreement with the analysis. The proposed methodology can serve as a useful tool for predicting comparative error performance of various configurations. Comparative performance of some GeAr adder configurations in a practical application of Gaussian smoothing of an image is also predicted and verified.

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