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1Ø MULTILEVEL INVERTER TOPOLOGIES BY SELF-VOLTAGE EQUIVALENT CAPABILITIES

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Abstract: Inthis examination, two new structures of single-stage half and half staggered both symmetrical and hilter kilter arrangements that canbe utilized indrives and controlof electrical machines&association of sustainable power sources. The proposed arrangement utilizes a lessnumber of semiconductor gadgets and DCsources as contrasted and regular and recently created topologies whichlead toa decrease in expense and establishment zone. Theproposed topology represents an indispensable bit of leeway of self-voltage adjusting ofits capacitor voltage paying little mind to load type, load elements and balance record. Additionally, the proposed topology is extended in a fell manner which decreases the multifaceted nature and improves the exhibition essentially. Awide scope of correlation is finishedwith traditional and recently created topologies to demonstrate the predominant exhibition of proposed topologies in regards to an all out numberof switches and DCsources. Themulti-bearer beat width balance system is embraced for creating exchanging beats for individual switches. A lab model is produced fortestingthe presentation oftheproposed topology for9-leveland17-levelinverters.

1. INTRODUCTION

Staggered inverter (MLI) gives the answer for conquer the voltage confinement of the old style 2-levelinverter and to arrive at the higher powerlevel by utilizing an arrangement association of different semiconductor gadgets with reasonable control method. The first MLItopology was presented around fourdecades back, and from that point forward immense push is found inthefield of intensity converters and theirapplications [1–3]. MLI is utilized in highpower applications, for example, AC enginedrive[4, 5], dynamic power channels [6, 7] and reconciliation of sustainable power source intothe framework [8, 9]. Aside fromhigh-voltage similarity, MLI likewise acts advantageous advantages such like improved power quality, diminished absolute consonant twisting, less voltage worry over the switches, great electromagnetic similarity, decreased exchanging misfortunes and dv/dt stressTraditionally,MLIs are ordered intothree classifications, and theyare: fell H-connect, flyingcapacitor and nonpartisan point braced (NPC) andthese topologies are generally alluded toas 'Old style Topologies' [10, 11]. Notwithstanding, the old style topologies have a few imperatives, for example the quantity of DCsources and switches are expanded which additionally increment fringe gadgets, for example, door driver circuit, insurance circuitand warmth sink. This augmentation inthe parts prompts increment in cost, by and large framework multifaceted nature, misfortunes and lessens the dependability and effectiveness of the converter. Consequently, alongside the

investigation of old style topologies, a generous push is found in the advancement of use arranged more up to date topologieswith a decreased numberof gadgets [12–14] andtheir regulation/control strategies requires a lot of bidirectional switcheswhich increment the misfortunes in theproposed topology as contrasted and regularCHB. Additionally, theproposed topology can't be worked in an uneven mode, thus falls behind ordinary lopsided CHB. The topologyof[18] at first proposes sub-MLIand after that for accomplishing a most extreme numberof yield levels in awry setup, the fell structure hasbeen proposed. It requires an alternate assortment ofswitches with respect to blockingvoltage capacities which increment the expense and unpredictability ofthe converter. Additionally, the power adjusting among various information sources is unimaginable and subsequently life is diminished. The topologies of [19, 20] utilize the arrangement association of DC sources. Likewise, a fell structure is proposed for acquiring the most extreme number of levels in yield. It requires an enormous number of bidirectional switches which expands the general misfortunes of the proposed inverter. The topologies of [17–20] experience the ill effects of one noteworthy disadvantage, for example the switches of its Hbridge need to hold up under the complete info voltage which limits the activity at higher-voltage levels. The topologies of [21–23] propose inverter which decreases switches essentially when contrasted and ordinary CHB. Notwithstanding, both double and trinary blends of DC hotspots for the hilter kilter activity of the proposed topologies are unrealistic because of which it lingers behind the regular CHB.In [24], a symmetrical topology of MLI is proposed which decreases the quantity of segments and has a basic tweak conspire. Switches of its H-connect need to manage the full evaluated voltage of the inverter which limits its application at high-voltage levels which is a noteworthy inconvenience. In [18], another topology for MLI is proposed, however the primary downsides for this topology are the utilization of bidirectional switches, an assortment of switches and limitation on high-voltage applications. In [25], another symmetrical MLI topology has been proposed utilizing less number of switches and lessening the exchanging misfortunes up, all things considered, as contrasted and regular MLI. Be that as it may, a noteworthy disadvantage is the loss of its measured quality. The topologies of [26, 27] require more switches as contrasted and the proposed topology. In [28], topologies have been displayed for both symmetrical and hilter kilter MLIs, yet the fundamental disadvantage is the scope of accessible power factor being exceptionally thin; just loads with power factor near solidarity can be provided. In [29, 30], two topologies dependent on created H-spans are presented. The principle disadvantage of these topologies is the necessity of countless autonomous DC sources which builds the expense of these topologies. From the above writing, it is reasoned that, to accomplish a higher number of yield levels with a less number of gadgets, extraordinary trade off has been made regarding number of bidirectional switches, unidirectional switches, DC sources, assortment of switches, assortment of warmth sinks, assortment of DC sources, unwavering quality, seclusion, straightforwardness, adaptability and exchanging misfortunes. The worry referenced above has been downsized, as it were, in the proposed

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topologies.

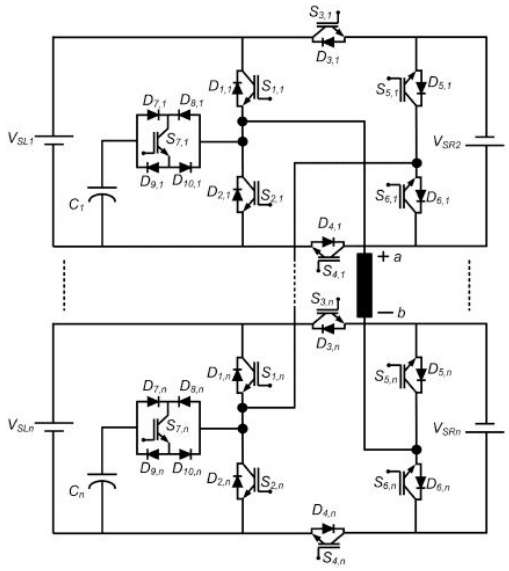

Fig. 1-Configuration of the proposed topology-I

Table 1 Switching table for 9-level inverter of topology-I

Output levels	'ON' state switches	Effect on capacitor voltage If 'i_L>0'	If 'i_L<0'
C_V	S_4, S_6, S_7	discharging	charging
V_{SR}	S_2,S_4, S_5	no effect	no effect
$C_V + V_{SR}$	S_4, S_5, S_7	discharging	charging
$V_{SL} + V_{SR}$	S_1, S_4, S_5	no effect	no effect
0 V	S_2, S_4, S_6	no effect	no effect
$-C_V$	S_3, S_5, S_7	discharging	charging
$-V_{SR}$	S_1, S_3, S_6	no effect	no effect
$-(V_{SL} + V_{SR} - C_V)$	S_3, S_6, S_7	discharging	charging
$-(V_{SL} + V_{SR})$	S_2, S_3, S_6	no effect	no effect

A symmetrical topology is introduced in [31] which uses single DC source in parallel of arrangement associated capacitors. The principle disservice of this topology is that solitary symmetrical setup is given. Also, four of its switches need to manage the all out voltage of the inverter limiting its application to medium voltage. The topology of [32] proposes a fell variant of the topology of [31] that can be worked at high-voltage levels as the sub-squares are associated in a fell way. In [33], the topology of [31] has been altered to lopsided form to arrive at a greatest number of yield levels. Usage of numerous bidirectional switches is the primary disadvantage of this topology. In [34], the topology of [31] has been displayed for both symmetrical and lopsided MLIs which arrive at a higher number of yield levels. The fundamental downside is the prerequisite of an enormous number of autonomous DC sources which builds its expense tremendously.In [35], another topology of the MLI is proposed for 5-level inverter utilizing single DC source and two CHB arrangements. In this topology, capacitor voltage of one of the CHB squares is managed by a stage move balance procedure which decreases the quantity of separated DC sources considerably sum. The primary constraint of this topology is that the switches of its fundamental H-connect need to hinder the all out yield voltage of the inverter which confines its application in higher-voltage application. The topologies of [36–39] propose pressed U-cell topology which diminishes the quantity of confined DC sources by a huge edge contrasted and traditional CHB. The principle bit of leeway of these topologies is that they don't require any outside hardware for keeping up its capacitor voltage in a reasonable state. In [40], another exchanging procedure is created by consolidating particular symphonious alleviation and specific consonant disposal strategies for four leg NPC inverter which diminishes the power misfortunes, yet in addition keeps up the DC capacitors voltage in a fair state with low-voltage swells even at lower exchanging frequencies. The topology of [41, 42] proposes topologies of MLI that diminishes the DC source necessity by utilizing capacitors without the help from an outside circuit, for example the topologies of [41, 42] have self-voltage adjusting capacities, yet the two topologies require an enormous number of switches as contrasted and proposed topologies.In this paper, two new topologies are exhibited

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which can be worked in both symmetrical just as deviated designs. The proposed topology has a secluded structure as it is associated in a fell manner and gives dependable activity to symmetrical and unbalanced designs with less voltage weight on the semiconductor switches. It doesn't require any outside circuit for adjusting its capacitor voltage because of its self voltage adjusting ability. 'Self-voltage adjusting' signifies the capacity of the capacitor to keep up its voltage in a decent state without requiring any guide from the outer circuit regardless of burden elements, balance file or homeless people. The symmetrical and deviated setups of proposed topologies produce the most extreme number of yield levels with less number of switches and confined DC sources relatively. The quantity of bidirectional switches additionally decreases altogether in the proposed topologies. The proposed topologies likewise have included the upside of equivalent DC source use and decreased misfortunes. A nitty gritty correlation of proposed topologies with traditional topologies and some as of late recently created topologies is done dependent on the quantity of switches and DC hotspots for both symmetrical and hilter kilter setups to viably demonstrate the advantages of the proposed topology.

2 Proposed MLI topologies

2.1 Proposed topology-I:

The summed up arrangement of topology-I in a symmetrical design is appeared in Fig. 1. Every cell in topology-I is made out of seven controlled switches, ten power diodes, two DC sources and one capacitor. The DC source on the left-hand side is numbered as VSL1, VSL2, … ,VSLn and on the right-hand side is numbered as VSR1, VSR2, … , VSRn ('n means the quantity of arrangement cell'). The summed up numerical articulation for topology-I in the symmetrical design for 'N' cells

$$\text{number of DC sources} = 2N \quad (1)$$

$$\text{number of capacitors} = N \quad (2)$$

$$\text{number of IGBT's} = 7 \times N \quad (3)$$

$$\text{number of diodes} = 10 \times N \quad (4)$$

$$\text{number of output levels} = (8 \times N + 1) \quad (5)$$

Exchanging plan for 9-level of topology-I is given in Table 1 alongside the capacitor charging and releasing states. It must be noticed that for unadulterated resistive burden, the capacitor releases at voltage levels 'CV' and 'CV+VSR', while charging of capacitor happens at voltage level '−CV' and '(VSL+VSR−CV)'. No different states can influence the capacitor voltages. Fig. 2 shows the progression of current at all the individual levels.

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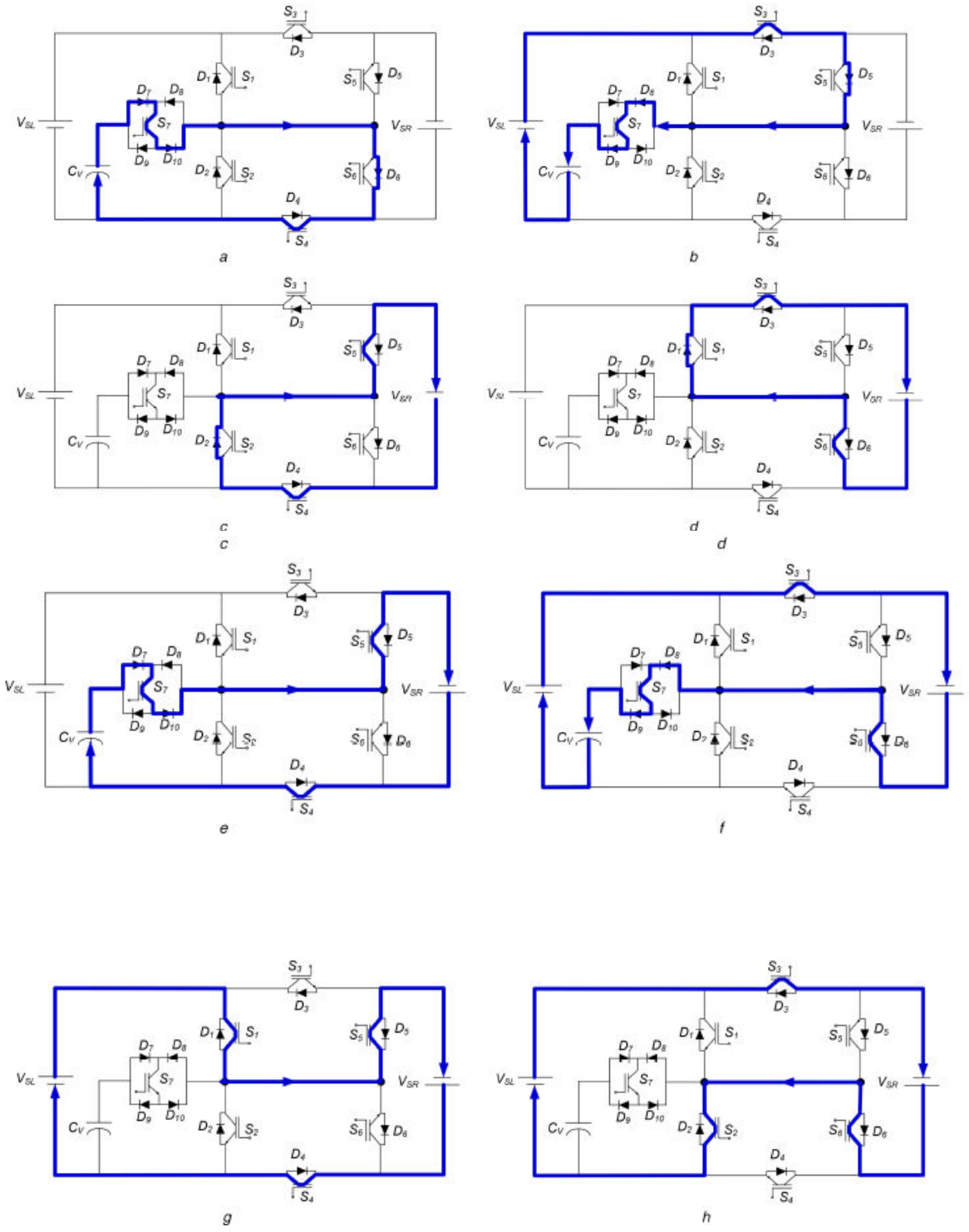

Fig. 2 Current flow direction of topology-I for 9-level output

(a) Output voltage = C_V, (b) Output voltage = − (V_{SL} − C_V), (c) Output voltage = V_{SR}, (d) Output voltage = − V_{SR}, (e) Output

(b) voltage = (V_{SR}+C_V), (f) Output voltage = − (V_{SR}

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$+V_{SL} - C_V$), (g) Output voltage = ($V_{SR}+V_{SL}$), (h) Output voltage = $-(V_{SR}+V_{SL})$, (i) Output voltage = 0_V

in every cell, and its summed up structure is given in Fig. 3 and called it as proposed topology-II. Like topology-I, the topology-II is likewise associated in a fell way to accomplish seclusion. The DC source on the left-hand side is numbered as VSL1, VSL2, … , VSLnand on the right-hand side is numbered as VSR1, VSR2, … , VSRn. It can likewise be worked as symmetrical arrangement by utilizing similar estimations of DC sources. Table 2 gives the distinctive exchanging states for 9-level yield for the proposed topology-II. For topsy-turvy activity, the estimations of DC sources are allocated by Table 3. In customary lopsided CHB, the

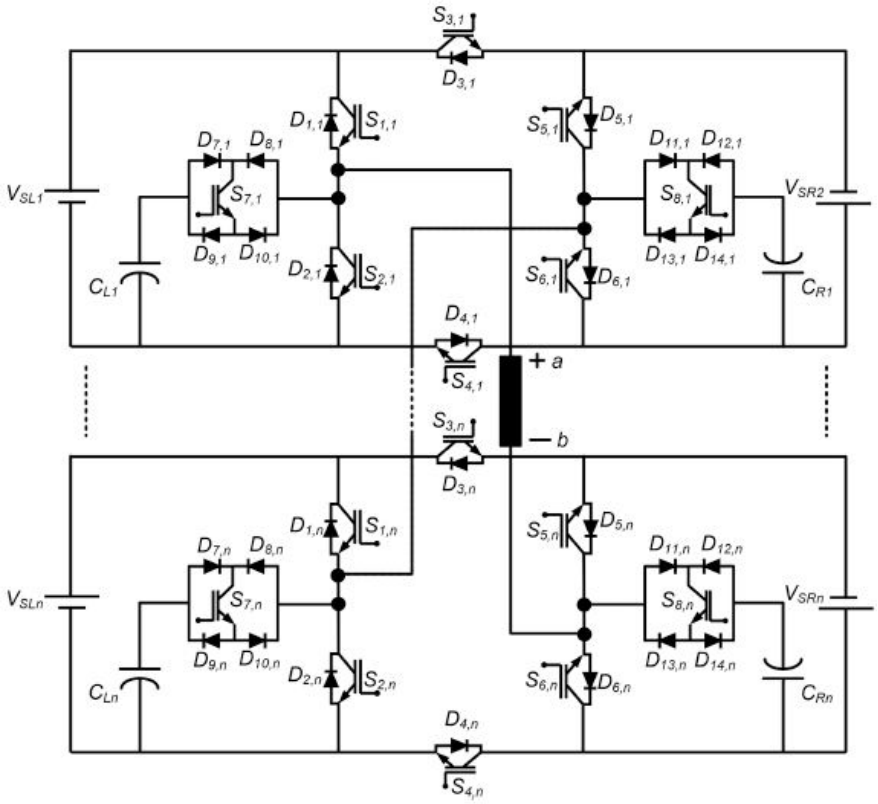

Fig. 3 Configuration of the proposed topology-II

Table 2 Switching table for 9-level inverter of topology-II

Output Levels	'ON' state switches	Effect on capacitor voltage			
		Capacitor C_L		Capacitor C_R	
		If '$i_L > 0$'	If '$i_L < 0$'	If '$i_L > 0$'	If '$i_L < 0$'
C_L	S_4, S_6, S_7	discharging	charging	no effect	no effect
$C_L + C_R$	S_4, S_7, S_8	discharging	charging	discharging	charging
$C_L + V_{SR}$	S_4, S_5, S_7	discharging	charging	no effect	no effect
$V_{SL} + V_{SR}$	S_1, S_4, S_5	no effect	no effect	no effect	no effect
0 V	S_2, S_4, S_6	no effect	no effect	no effect	no effect
$-(V_{SL} - C_L)$	S_3, S_5, S_7	discharging	charging	no effect	no effect
$-(V_{SL} + V_{SR} - C_L - C_R)$	S_3, S_7, S_8	discharging	charging	discharging	charging
$-(V_{SL} + V_{SR} - C_L)$	S_3, S_6, S_7	discharging	charging	no effect	no effect
$-(V_{SL} + V_{SR})$	S_2, S_3, S_6	no effect	no effect	no effect	no effect

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Table 3 Realization of different levels of proposed topology-II incorporating 'n' number of cells

Algorithm	Values of DC sources	Number of output levels	Configuration
first	$V_{SL1} = V_{SR1} = \cdots = V_{SLn} = V_{SRn}$	$8 \times n + 1$	symmetrical
second	$\frac{V_{SL1}}{2^0} = \frac{V_{SR1}}{2^1} = \frac{V_{SL2}}{2^2} = \frac{V_{SR2}}{2^3} = \cdots = \frac{V_{SLn}}{2^{2\times n-2}} = \frac{V_{SRn}}{2^{2\times n-1}}$	$4 \times [\sum_{m=1}^{n}(V_{SLm} + V_{SRm}) \div V_{SL1}] + 1$	asymmetrical
third	$\frac{V_{SL1}}{3^0} = \frac{V_{SR1}}{3^1} = \frac{V_{SL2}}{3^2} = \frac{V_{SR2}}{3^3} = \cdots = \frac{V_{SLn}}{3^{2\times n-2}} = \frac{V_{SRn}}{3^{2\times n-1}}$	$4 \times [\sum_{m=1}^{n}(V_{SLm} + V_{SRm}) \div V_{SL1}] + 1$	asymmetrical
fourth	V_{SL1} = initialise $V_{SR1} = 3 \times V_{SL1}$ $V_{SLn} = 4 \times \left[\sum_{m=1}^{n-1}(V_{SLm} + V_{SRm})\right] + V_{SL1}$ $V_{SRn} = 2 \times \left[V_{SLn} + \left(\sum_{m=1}^{n-1}(V_{SLn} + V_{SRn})\right)\right] + V_{SL1}$	$4 \times [\sum_{m=1}^{n}((V_{SLm} + V_{SRm}) \div V_{SL1})] + 1$	asymmetrical

estimations of DC sources are doled out in a predefined way of either double (2:1) or trinary (3:1) mix and as needs be the yield levels increment. Be that as it may, some as of late distributed writing demonstrates the working of deviated topology by allocating estimations of DC sources in a predefined way of 4:1 [33], 5:1 [33] and even 7:1 [30], because of which the quantity of yield levels colossally increments as contrasted and hilter kilter CHB. Hence, so as to arrive at the most astounding number of yield levels in the proposed topology-II, another calculation is embraced which is given in Table 3 (fourth calculation).

2.3 Capacitor voltage balancing

In the proposed topology, the capacitor voltage consistently stays in a reasonable state independent of the heap type, balance file or burden qualities. Likewise, the proposed topology does not require any convoluted strategies for keeping up its capacitor voltage in a adjusted state. This wonder can be clarified scientifically by capacitor ampere-second equalization condition; as indicated by this condition, the net change in capacitor voltage over single exchanging cycle under enduring state condition ought to be zero. Current crosswise over capacitor is given by

$$i_C(t) = C\frac{dv_C(t)}{dt} \tag{6}$$

where '$i_C t$' is the instantaneous capacitor current and '$v_C t$' is the corresponding voltage across the capacitor at the same instant.

Integration of the above equation over single switching cycle yields

$$\int_0^{T_S} i_C(t)\,dt = C\int_0^{T_S}\left(\frac{dv_C(t)}{dt}\right)dt \tag{7}$$

$$\int_0^{T_S} i_C(t)\,dt = V_C(t) - V_C(0) \tag{8}$$

Presently from (8), it tends to be said that the net change in capacitor voltage over single exchanging cycle is equivalent or corresponding to vital of capacitor current over a similar exchanging cycle. In enduring state, beginning and last estimations of capacitor voltages are the equivalent. In this manner

$$\text{average capacitor current} = \frac{1}{T_S}\int_0^{T_S} i_C(t)\,dt = 0 \tag{9}$$

From (9), it tends to be presumed that the normal worth or DC segment of the capacitor current must be zero in harmony. The point by point examination of capacitor voltage adjusting is displayed in Fig. 4a.

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3 Comparison studies

The proposed topology-I offers more advantages in symmetrical setup and topology-II in a deviated design. Along these lines, in this area, an appropriate correlation is drawn for topology-I in a symmetrical arrangement and topology-II is contrasted and recently created awry topologies.

3.1 Comparison of symmetrical MLI

Examination ofthe proposed topology-I with recently created topologies of regular CHB worked in symmetrical arrangement isgiven inFigs.5a and b. It very well may be seen that the proposed topology-I requires minimal measure of switches in a symmetrical setup. In addition fromFig.5b, it very well may be seen that the DCsource prerequisite in the proposed topology-Iis not as much as topologies27,30,34and equivalent to topologies of [26, 32]. Henceforth, the proposed topology-I insymmetrical setup requires minimal numberof gadgets as contrasted & ordinary and recently created topologies.

3.2 Comparison of asymmetrical MLI

Correlation ofthe proposed topology-IIwith recently created topologies of[18,27,29,30, 33,34]and regular CHB worked in hilter kilter design is exhibited inFigs. 5c and d. It tends to be seen thatthe proposed topology-IIrequires minimal measure of switchesin awry setup as contrasted and regular topologyand recently created topologies. Likewise, DCsource necessity is less as contrasted and CHBand the recently created topologies of[18,27,29,30,34], however requires more sourcesas the topology of[33] as delineated inFig. 5d. Fig. 5 demonstrates that the proposed topologies in symmetrical and uneven setups require minimal number of gadgets (switches and DC sources) as contrasted and regular and recently created topologies. In addition, the proposed topologies don't require any outside circuit for keeping up its capacitor voltage in a fair state. Table 4 gives the summed up correlation between the proposed topology-I and recently created topologies for 'N' number of yield levels which incorporates all out parts required for the single-stage inverter. Table 4 likewise gives the examination of different topologies dependent on all out kVA evaluations.

4 Simulation and experimental results

4.1 Modulation scheme

For controlling theswitches, the door sign are created utilizing a reasonable multi-transporter beat width tweak (MCPWM) method for bothtopology-Iandtopology-II. The transporter exchanging recurrence is keptat 100Hzand5kHz, though the reference signal recurrence iskeptat 50Hz. InMCPWM procedure, thebeatare produced by reasonable sensible activity among bearer and reference sign and after that the beats are bolstered tothedriver circuitwhich enhances the size of created heartbeats totrigger the individual switch [43]. In MCPWM system, the quantity of transporter sign required is reliant on the quantity of yield levels('M−1'). The essential methodology forMCPWM is given inFig.6a and entryway beats forthe proposed topology-I for 9-level aregiveninFig.6b.

4.2 Simulation results

Totest and look at the exhibition ofthe proposedtopologies, a recreation studyhas been completed utilizing MATLAB/Simulink.Topology-I is mimicked forsymmetrical design as 9-level inverter andtopology-II for the 17-level inverter. Diverse recreation and test parameters forboth thetopologies are given inTable5. For figuring thecapacitor esteem, beneath recipe is utilized:

$$C_S \geq (I_{out} \times t_{on})/(\%ripple \times V_{in}) \quad (10)$$

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where Iout isthecurrent conveyed bya capacitor, ton isthe charging/releasing time ofthecapacitor, %ripple isthe most extreme permissible swell substance incapacitor voltage (10% remittance istaken for proposedtopologies) and Vin is the capacitor adjustedvoltage. Fig.7a demonstrates the reenactment consequences design under two diverse exchanging example the exchanging recurrence is all of a sudden changedfrom 5kHzto100Hz.Fig. 7a portrays the waveformsof the yield voltage, yield current, capacitorvoltage and capacitorcurrent. From Fig. 7a, it very well may beseen thatthe inverter exchanging recurrence hasno effect oncapacitor voltage and capacitor keeps up itsvoltage at a fair stateatboth the exchanging frequencies. To look the exhibition of the proposedtopology-II in hilter kilter arrangement, 17-level yield waveformsare delineated in Fig. 7b. From thewaveforms portrayed in Fig. 7b, it tends to beseen that the capacitorvoltage is in a fair state at exchanging recurrence of 5 kHz.To successfully demonstrate the self-voltage adjusting of its capacitorvoltage under unexpected burden change, under various modulationindex and diverse reference frequenciesthe reproduction study iscarried out dependent on 9-levelinverter of topology-Iandresults aregiven in Figs. 7c and d. Theworking oftopology-I when thesudden burden progress happens at 0.1 s is appeared in Fig. 7c. Itcan be seen from Fig. 7c thatat0.1s the yield current increments;

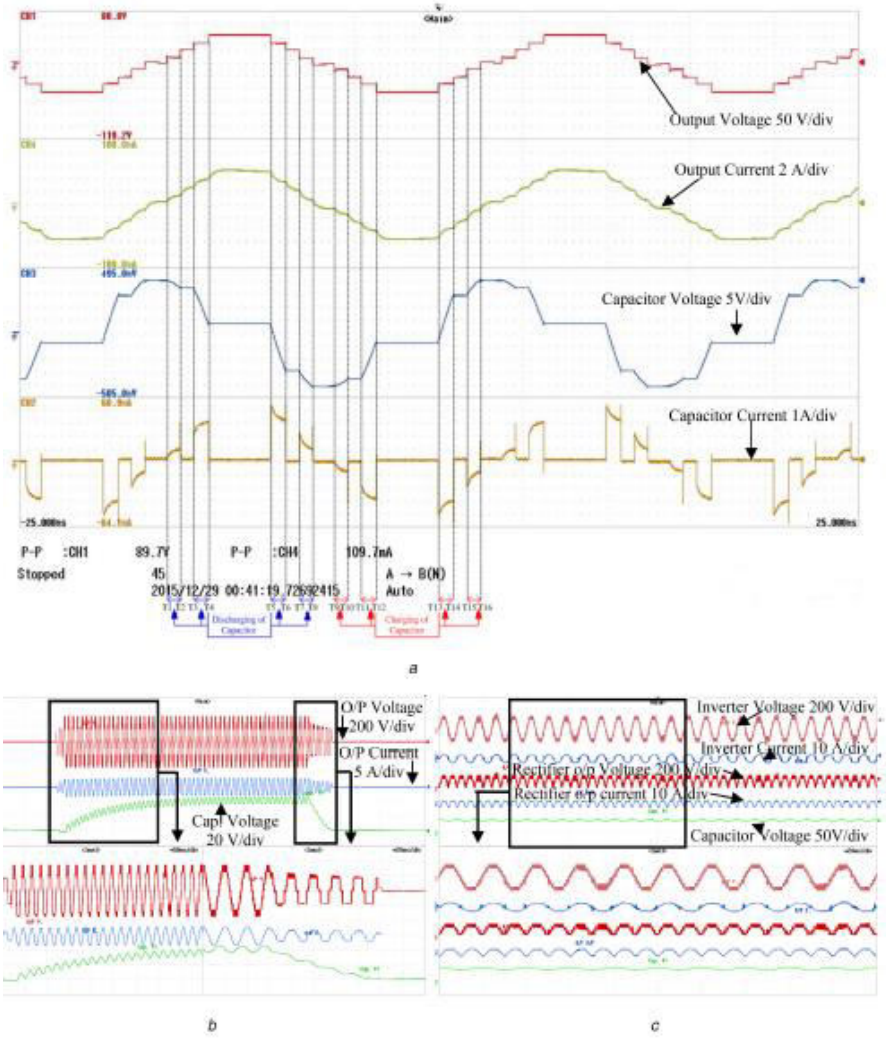

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Fig.4 Experimental results for demonstratingself-voltage balancing capabilities oftheproposed topology

henceforth, the capacitor current likewise builds, whichresults in more swells in capacitorvoltage, yet at the same time the voltage stays ina decent state. Theworking of topology-I when itis changed starting with one balance file then onto the next at 0.1s is appeared in Fig. 7d. It tends to be seen that at 0.1 s whenthe topology is changed solidarity adjustment file to 0.5 tweak file the yield current abatements because of whichcapacitor current additionally diminishes, which at last outcomes ina reduction in capacitorvoltage swell, however with adjusted voltage. Consequently fromFigs. 7c and d,it very well may be said thatthe capacitorvoltage inthe proposed topology consistently stays ina fair state, paying little heed to stack elements, adjustment record, exchanging recurrence orreference recurrence.

4.3 Experimental results

Here the definitely testing theworking of proposedtopologies, alaboratory model hasbeen created forthe 9-/17-level inverter of topology-I&topology-II, individually. For creating the constant exchanging beats, the dSPACE1103 controller hasbeen utilized and the produced heartbeats are then given to door drivercircuit for intensifying the created heartbeats and afterward at long last nourished to separate switches. The exploratory waveformsare dissected by the utilization ofscopecoder YOKOGAWA DL850E. Trial waveform, for example, yield voltage, yield current & capacitorvoltages for 9-level proposed topology-I at diverse exchanging frequencies isgiven in Figs. 8a and b. So also, resultsfor 17level of topology-II are givenin Figs. 8c and d. From Fig. 8, it is seen thatthe proposed topology functions admirably atlower just asat higher exchanging recurrence while keeping up itscapacitor voltage in a fair state forboth symmetrical and unbalanced configurations.To look at the charging and releasing ofthe capacitorvoltage in the proposed inverter, a trial study has beencarried out for the 9-levelinverter and result is given in Figs. 4a. FromFig. 4a, it tends to be seen thatthe normal estimation of thecapacitor current is constantly zero of every one completecycle. Therefore,it is presumed that voltage ofthe capacitor consistently remains adjusted regardless burden &tweak record.

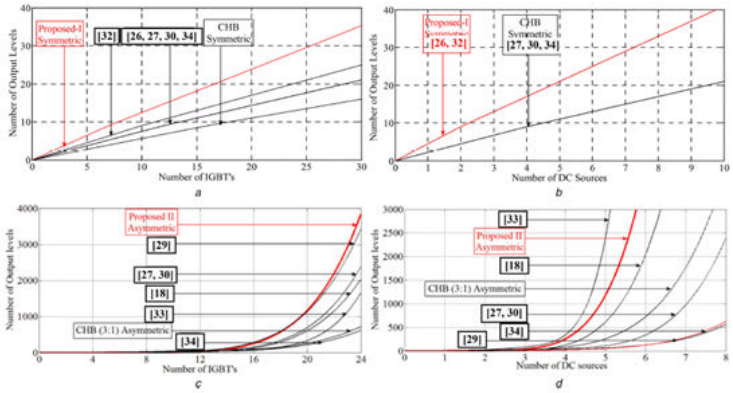

Fig. 5 Comparison of number of output levels (a) Versus number of IGBT's in symmetrical MLI, (b) Versus number of DC sources in symmetrical MLI, (c) Versus number of IGBT's in asymmetrical MLI, (d) Versus number of DC sources in asymmetrical MLI

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Table 4 Generalized comparisons for single-phase symmetrical MLI

Components	MLI topology								
	Topology-I	CHB	NPC	FC	[26]	[27]	[30]	[32]	[34]
main switches	$(N+19)/4$	$2(N-1)$	$2(N-1)$	$2(N-1)$	$3(N-1)/2$	$3(N-1)/2$	$3(N-1)/2$	$5(N-1)/4$	$3(N-1)/2$
main diodes	$(N+1)$	$2(N-1)$	$2(N-1)$	$2(N-1)$	$7(N-1)/4$	$7(N-1)/2$	$3(N-1)/2$	$2(N-1)$	$3(N-1)/2$
clamping diodes	0	0	$(N-1)\times(N-2)$	0	0	0	0	0	0
DC bus capacitor/ isolated supply	$(N+3)/4$	$(N-1)/2$	$(N-1)/3$	$(N-1)/3$	$(N-1)/2$	$(N-1)/2$	$(N-1)/2$	$3(N-1)/4$	$(N-1)/2$
FC	0	0	0	$(N-1)\times(N-2)/2$	0	0	0	0	0
total number of components	$(1/2)(3N+13)$	$(9/2)\times(N-1)$	$(N-1)\times(3N+7)/3$	$(N-1)\times(3N+20)/3$	$15(N-1)/4$	$11(N-1)/2$	$4(N-1)$	$4(N-1)$	$4(N-1)$
total blocking voltage on the switches ('V_{DC}' as input voltage)	$(17/8)\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$(9/4)\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$2\times(N-1)\times V_{DC}$	$(9/4)\times(N-1)\times V_{DC}$	$(9/4)\times(N-1)\times V_{DC}$

Additionally, a hypothetical clarification of capacitor voltage equalization should be possible from Fig. 4a. It very well maybe seen thatin the positive cycle the capacitor is associated in arrangement with the heap, subsequently releasing wonder happens, though in thenegative halfcycle (for example T9–T10, T11–T12, T13–T14 and T15–T16) thecapacitor associated arrangement withthe sourceand henceforth charging wonder happens. Presently, the time term of charging and releasing is kept up equivalent by utilizing reasonable exchanging procedure. Consequently, net vitality got is equivalent to net vitality conveyed by acapacitor inone complete cycle. Along these lines, capacitorvoltage consistently stays in a decent state.Fig. 4b demonstrates and settlesat half ofthe information voltage, for example 45Vand again returns to zeroatthe switch 'OFF' time. It must be noticed that thecapacitors utilized inthe proposed topologies set aside some effort to arrive at the relentless state conditionwhich causes some postponement while exchanging 'ON' theinverter. This sort of postponement is likewise found in the topologies exhibited in [35–38] additionally utilizes capacitors to decrease the DC source prerequisite. In every one of thesetopologies, the chargingand releasing procedures are straightforwardly relative to the heap esteem, for example forthe lower estimations of burden the capacitorcharges rapidly & bad habit versa. Totest theself-voltage adjusting abilities oftheproposed inverter, ithasbeen tried tentatively under non-straight loads, for example, diode rectifierand distinctive burden drifters and regulation records. Fig. 4c demonstrates the non-direct burden, for example diode rectifier. From Fig. 4c, it very well may be said thatthe capacitorvoltage stays in a reasonable stateunder non-straight burden. Consequently, itis seen that independent of burden type, tweak record or burden elements, the capacitorvoltage consistently stays ina fairstate.

4.4 Loss analysis and efficiency

Computationof misfortunes isextremely fundamental piece ofthe framework plan. MLI experiences three methods of tasks and and exchanging mode. In blockingmode, the gadgets need towithstand the voltage over itsterminal, consequently no present will stream inthismode over the gadget because of which the misfortunes in thismodeare viewed as irrelevant. Henceforth, the larger parts of the misfortunes in MLI arein conduction and exchangingmode

$$P_{\text{Total}} = P_{\text{C}} + P_{\text{SW}} \tag{11}$$

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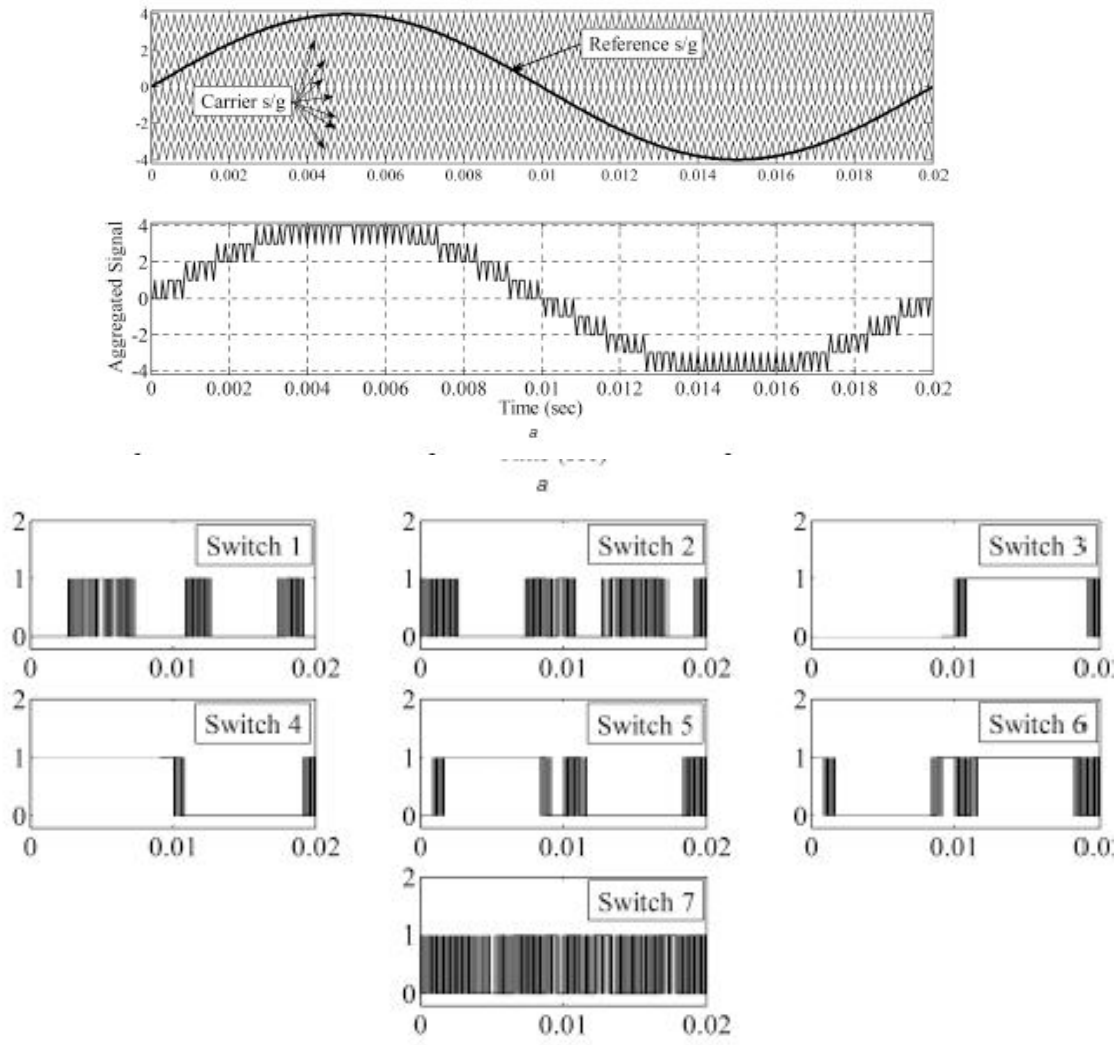

Fig. 6 Modulationscheme(a) Modulation strategiesfor the 9-levelMLI, (b) Gatepulses for respectiveswitches for9-level

Table 5 Simulationandexperimentation parameters

Parameters	Topology-I for 9-level	Topology-II for 17-level
source-I	90 V	30 V
source-II	90 V	90 V
capacitor, μF	1200	1200
load resistance, Ω	40, 80	40, 80
load inductance, mH	20, 200	20, 200
modulation index	unity, 0.5	unity
switching frequency, Hz	100 and 5000	100 and 5000

where P_{Total} is the totalloss, i.e. conductionloss (P_C) and switchingloss ($^{P}_{SW}$).

4.4.1 Conduction losses:

Conduction mode is depicted as the measure of intensity lost when the gadget is in 'ON' state [44]. Inthispaper, the two diodes and protected entryway bipolartransistors (IGBTs)are utilized creating yield levels; subsequently, conduction misfortunes for both the gadgets are appeared. First conduction misfortunes for individual

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gadgets are determined and afterward summed up to the proposed MLI. The voltagedrop over an IGBT canbe composed as

$$V_{CE}(i_c) = V_{CEO} + r_c \times i_c \qquad (12$$

where 'V_{CEO}' is the forwardvoltage drop acrossthe IGBT, 'r_c' isthe internalresistance ofIGBT and 'i_c' is thecollector current. The instantaneousvalue of IGBT conductionlosses is

$$p_{C,T}(t) = V_{CE}(t) \times i_c(t) = V_{CEO} \times i_c(t) + r_c \times i_c^2(t) \qquad (13)$$

Where ' $i_c t$ ' isthe instantaneous current. Average lossescan beexpressed as

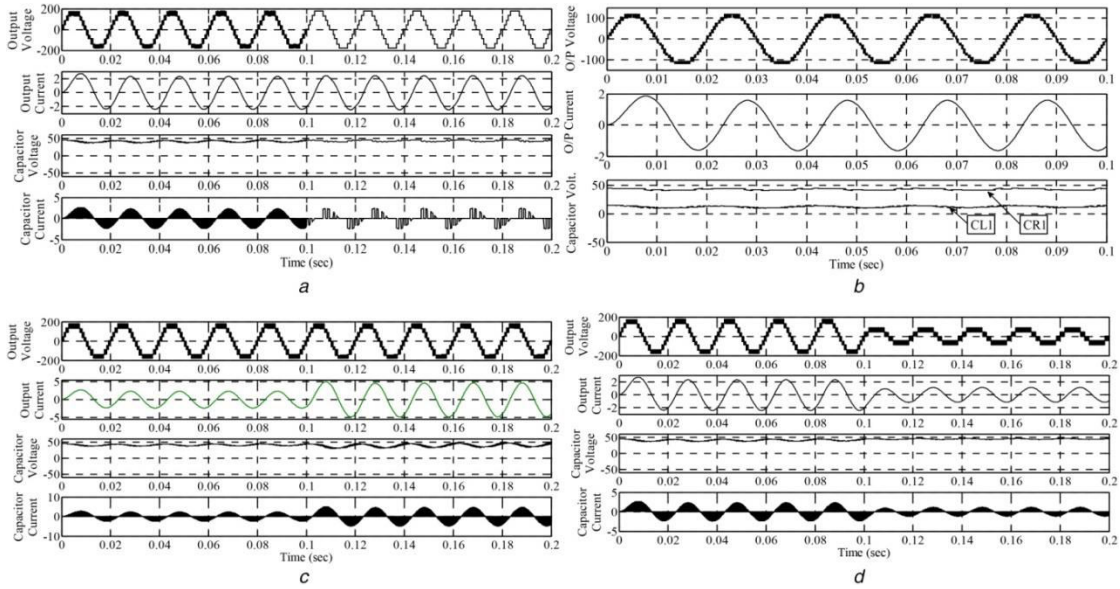

Fig. 7Simulation results
(a) 9-Levelwaveforms oFtopology-I at twodifferent switchin frequenciesof 5 kHzand100 Hz, (b) 17-Level waveformsoftopology-II at5 kHz switchingfrequency, (c) Suddenloadtransition, (d) Suddenchange in modulationindex, i.e.from unity to 0.5

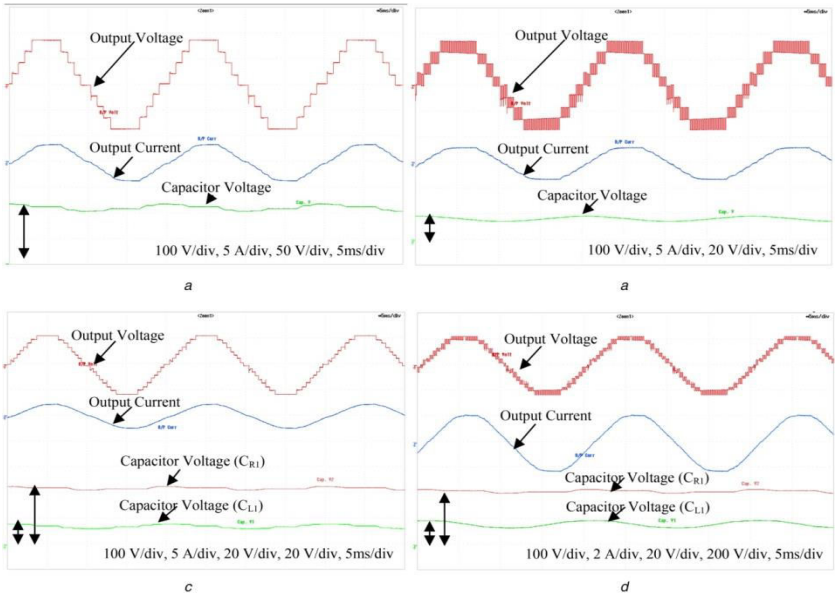

Fig. 8*Experimental results**(a)*9-Level waveformsof topology-Iat carrierfrequency 100 Hz

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b) 9-Level waveformsof topology-I atcarrier frequency5 kHz, ***(c)*** 17-Levelwaveforms oftopology-IIat carrier frequency100 Hz, ***(d)*** 17-Levelwaveforms oftopology-II atcarrier frequency5 kHz

$$P_{C,T} = \frac{1}{T_{SW}} \int_0^{T_{SW}} p_{C,T}(t)\,dt = \frac{1}{T_{SW}} \int_0^{T_{SW}} (V_{CEO} \times i_c(t) + r_c \times i_c^2(t))\,dt \quad (14)$$

$$P_{C,T} = V_{CEO} \times I_{c,av.} + r_c I_{c,rms}^2 \quad (15)$$

Table 6 Forwardvoltagedrop and internal resistanceofIGBT anddiode[45]

Series	Blocking voltage, V	Current capacity, A	IGBT		Diode	
			V_{CEO}, V	r_c, mΩ	V_{DO}, V	r_d, mΩ
FF600R06ME3	600	600	1.9	1	1.95	0.8
FF600R12KE3	1200	600	2.15	1.25	2.5	1
FF500R25KF1	2500	500	3.6	3	2.8	1.4

Table 7 Conduction losses for CHB

Switch number	Conduction losses FF600R06ME3	
	IGBT, W	Diode, W
1	11.543	7.621
2	13.044	0.098
3	5.934	0.489
4	11.886	0.274
5	10.627	2.799
6	13.044	0.098
7	10.619	1.428
8	11.886	0.274
9	9.193	0.900
10	13.044	0.098
11	12.491	2.898
12	11.886	2.224
13	5.458	0.008
14	13.044	0.098
15	12.817	6.686
16	11.888	0.274
total loss	178.406	26.267

Table 8 Conduction losses for the proposed topology-I

Switch number	Conduction losses FF600R06ME3	
	IGBT, W	Diode, W
1	6.509	2.108
2	7.092	2.259
3	25.464	0.099
4	22.800	0.170
5	12.166	1.029
6	14.427	1.755
7	10.847	22.110
total loss	99.304	29.530

$$P_{C,D} = V_{DO} \times I_{D,av.} + r_d I_{D,rms}^2 \quad (16)$$

where 'V_{DO}' is the forward voltage drop, 'r_d' is the on-state resistance and '$I_{Dav.}$, I_{Drms}' are the average and root-mean square (RMS) current of diode. For calculating the above-mentioned losses and to draw a suitable comparisonbetween CHBand proposed inverter, a MATLAB/Simulinkmodel is built inwhich data providedin the datasheets areused. Specificationsof MATLABmodel are:

Total input voltage: 2000 V.

Number of DCsources:four(500Vsuppliedby each DCsource).

Valueofresistance: 100 Ω.

Valueofinductor: 100 mH.

Table 6 offers thevalues ofthe forward fall across IGBT and diodeas obtainedfrom datasheets at the side of itsinternal resistances for IGBT's ofseries FF600R06ME3andFF500R25KF1. Table seven offers the worth of conductivity losses forCHB. Table eight offers the conductivity lossesfor proposed-I electrical converter.As may be seen from Tables seven and eight, conductivity losses square measure morein CHB as compared with proposedtopology-I. conductivity losses square measure thirty seventh (approx.) less in proposedtopology-I for each IGBTand diodesas compared with symmetricalCHB. Asseen fromTable eight, within thelowest voltage ratedswitch, i.e. S7, the foremost losses square measure within thediode; this is often as a result of the two-way switch that consists of 1 IGBT and 4 diodes. Hence, mostofthe lossesoccur

where 'I_{cav} . ' is the average value of collectorcurrent and 'I_{crms} . ' isthe rms. value ofcollector current. Similarly, conduction lossesfordiode can alsobe approximatedas

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within the diode. the very best voltagerated switches havemajor losses inIGBT since the conductivity throughthe diode isnegligible.

4.4.2 Switching losses:

Calculationof shift losses is complicated asno straightforward equation may be found forvoltage and current throughout a shift transient. shift lossesdepends on variety of shift transitions, i.e.transition from 'ON'to 'OFF' and transition from 'OFF' to'ON', block voltagecollector current, gate resistance andjunction temperature. It conjointly depends onmodulation strategy enforced.

$$E_{\text{off},i} = \int_0^{t_{\text{off}}} v(t) \times i(t)\,\mathrm{d}t = \int_0^{t_{\text{off}}} \left[\left(\frac{V_{\text{B},i}}{t_{\text{off}}} \times t\right)\left(-\frac{I}{t_{\text{off}}} \times (t - t_{\text{off}})\right)\right] \mathrm{d}t = 1/6 \times V_{\text{B},i} \times I \times t_{\text{off}} \quad (17)$$

where $E_{\text{off},\,i}$ is theenergy ofthe '*i*th' switch, $V_{\text{B},\,i}$ isthe blockingvoltage ofthe '*i*th' switch, *I*is thecurrent through the '*i*th' switchbefore turningoff and t_{off} is theturn-off time of the'*i*th' switch. mathematical expressionfor calculationof energy lossduring turn-on periodis

$$E_{\text{on},i} = 1/6 \times V_{\text{B},i} \times I' \times t_{\text{on}} \quad (18)$$

where $E_{\text{on},\,i}$ is theenergy loss ofthe '*i*th' switch, $V_{\text{B},\,i}$ is theblocking voltageof the '*i*th'switch, *I′* isthe current throughthe '*i*th' switchafter turningON and t_{on} isthe turn-on timeofthe '*i*th'switch. Henceassuming $I = I'$, thetotal switching powerlosses forindividual switchcan becalculated as

$$P_{\text{loss},i} = (E_{\text{off},i} + E_{\text{on},i}) \times f_{\text{s}} = \frac{1}{6} \times V_{\text{B},i} \times I \times (t_{\text{on}} + t_{\text{off}}) \times f_{\text{s}} \quad (19)$$

where f_{s} isthe switchingfrequency ofthe '*i*th' switchand $P_{\text{loss},\,i}$ is thepower lossfor the '*i*th' switch.From (19), itis clearthat

$$P_{\text{loss},i} \propto V_{\text{B}} \text{ and } P_{\text{loss},i} \propto f_{\text{s}} \quad (20)$$

Asearlier mentioned thatthe obstruction voltage ofthe H-bridge switches utilized in several topologies hasbeen reduced to 0.5 in proposedtopology-I, therefore from (20) it's terribly clearthatthe switch losses of the switches of H-bridge scale back to half the polygon cellin proposedtopology.To compare the switch lossesof 9-level symmetricalCHB thereupon of 9-level projected topology-I, (19) will bewrittenas

$$P_{\text{loss}} = \frac{1}{6} \times V_{\text{B}} \times I \times (t_{\text{on}} + t_{\text{off}}) \times f_{\text{s}} \quad (21)$$

Assumingthat t_{on} & t_{off} areof sameperiod and theycarry the samecurrent *I*, (21) can be writtenas

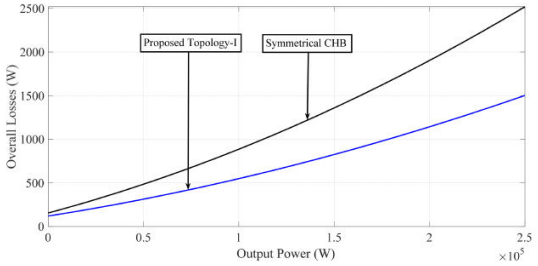

Fig. 9 Comparison of overalllosses on multipleoperatingpoints

$$P_{\text{loss}} = c \times V_{\text{B}} \times f_{\text{s}} \quad (22)$$

where $c = \frac{1}{6} \times (I \times t_{\text{on}}) + t_{\text{off}}$ isa constantthus from(22) switching lossesfor 9-level symmetricalCHB having's voltagesource V_{DC} can bewrittenas

$$P_{\text{loss, 9-level CHB}} = 16 \times c \times V_{\text{DC}} \times f_{\text{s}}. \quad (23)$$

Now within the projected topology-Ithere's one IGBT with obstruction avoltage of VDC, fourIGBTs with obstruction voltage 2×VDC and 2 IGBTswith obstruction voltage 4×VDC. the2IGBTs with obstruction voltage 4×VDC ar switched one time throughout a basic cycleas mentioned earlier. Letthe shift frequency bedenoted by fs and harmonic bedenoted by FO. Then by mistreatment (19), shift losses for 9-level projected inverter-I havingvoltage supply 2VDC will be written as

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$$P_{\text{loss, 9-level Prop-I}} = c \times (V_{DC} \times f_s + 4 \times 2 \times V_{DC} \times f_s + 2 \times 4 \times V_{DC} \times f_o) \quad (24)$$

$$P_{\text{loss, 9-level Prop-I}} = 8 \times c \times V_{DC} \times \left(\frac{9}{8} \times f_s + f_o\right) \quad (25)$$

Since $\left(\frac{9}{8} \times f_s \gg f_o\right)$, (25) can be written as

$$P_{\text{loss, 9-level Prop-I}} = 9 \times c \times V_{DC} \times f_s \quad (26)$$

From (23) and (26)

$$P_{\text{loss, 9-level Prop-I}} \cong \frac{P_{\text{loss, 9-level CHB}}}{2} \quad (27)$$

Hencefrom (27), itis clear that theswitching lossesof the 9-level proposedinverter-I are almosthalf as thatof9-level symmetrical CHBunder similaroperatingconditions.

4.4.3 Overall losses: Inthis area, a correlation hasbeen made between the proposedtopology and the regular CHB dependent on in general misfortunes and delineated in Fig. 9. For examination reason, the reenactment results havebeen takeninwhich the qualities gave in datasheetsare utilized to viably figuring the general misfortunes. To demonstrate the predominance of the proposedtopology over traditional CHB, the recreation results havebeen takenat different working focuses. FromFig.9, it very well may be seen thattheproposed topology haslower in general misfortunes as contrasted andCHB.

5 Conclusions

This paperproposes two new mixture topologies ofsymmetrical and unbalanced MLI withthe self-voltage adjusting of its capacitorvoltage and witha decreased numberof gadgets. For acquiring the most extreme numberof yield levels in awry arrangement, another calculation is proposed. Theproposed topologies have been tried tentatively for9-level and 17-level invertersunder various exchanging frequencies. For successfully exhibiting theself-voltage adjusting wonder of capacitor voltage, the proposedtopologies havebeen tried undernon-straight burden, responsive burden, under various balance file and diverse burden progress. Awide scope of correlation is drawnbetween theproposed topologies, ordinary andthe recently created topologieswhich demonstrate that theproposed topologies require minimal numberofswitches and DCsources as contrasted and differenttopologies.

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