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Title **GRID CONNECTED CONVERTER STRATEGIES FOR IMPROVED DC-LINK VOLTAGE CONTROLS**

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GRID CONNECTED CONVERTER STRATEGIES FOR IMPROVED DC-LINK VOLTAGE CONTROLS

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Abstract:-This paper exhibits a effective manage machine to improve dc-interface voltage manipulate exhibitions for Grid associated Converters (GcCs). The proposed manipulate methodology relies upon on a flexible PI controller and is deliberate to guarantee brief temporary response, low dc-connect voltage vacillations, low community present day THD and excellent aggravation dismissal after surprising adjustments of the dynamic energy drawn via the GcC. The relative and basic additions of the considered versatile PI controller are self-tuned so they are appropriate as to the working purpose of the controlled framework and additionally its state. A few reenactment and exploratory outcomes are exhibited to affirm and approve the adequacy and achievability of the proposed dc-connect voltage control system.

Index Terms:-DC-link voltage control, adaptive PI controller, Grid connected Converters

1. INTRODUCTION

These days, control converters have a significant job in a huge size of mechanical Applications due to the fact that they allow effective energy Transmission among the matrix (on one side) and hundreds or strength assets (on the other component). The usually utilized electricity converters topologies employ a dc-interface as a transitional degree for the electricity change method however a Grid associated Converter (GcC) and a channel dependent on detached (inductive and moreover capacitive) components. For example, this is the scenario of customizable pace drives [1-2], sustainable power resources [3-4], dynamic electricity channels [5-6], UPS frameworks [7] and consecutive frameworks [2],[8]. Proficient dc-be part of voltage manage is enormous for such programs to

lessen voltage variances within the dc-interface [9], which can be predominantly added about by the usage of arbitrary adjustments (specially abrupt and decrease off modifications) within the electricity drawn with the aid of manner of the GcC. At the point whilst those vacillations go their limits, the warranty gadgets are actuated prompting a framework close-down [3],[9]. Hence, the manipulate targets concerning the dc-interface voltage may be condensed within the accompanying key focuses: 1) the voltage over the dc-interface capacitor have to be stored at a regular an incentive thru controlling the strength motion in the AC aspect of the GcC with the purpose that two destinations are fulfilled: the first is the upkeep of the capacitor price, while thesecond one is the supply of a heap

associated with the dc-be part of (for the amending mode case) or then again the trade of the strength given by way of a DC source (for the reversing mode case), 2) the dc-joint voltage changes should be constrained, 3) the age of excessive lattice contemporary song should be anticipated and four) The deviation from the team spirit energy aspect pastime introduced about by the matrix modern-day swells should be averted. The most as often as possible utilized dc-interface voltage controller is the PI controller [10],[11]. Distinctive PI controller plan strategies were depicted in writing. Among them, we can refer to the post zero scratch-off strategy, the shaft position technique and the ideal model strategy [8],[11]. For these techniques, the PI controller is normally balanced as for numerous requirements: C1) soundness; C2) dynamic exhibitions; C3) aggravation dismissal; and C4) step reactions with low overshoot [12]. So as to fulfill each this kind

of imperatives, some exam works exhibited the plan of flexible PI controllers [13-17]. Different ones consolidate between the benefits of the PI controller and the feed ahead remuneration strategy [18-20]. Contrasted with the normal DPC, the dc-interface voltage is taken into consideration for willpower of the changing states via an replacing desk. Thus, no outside circle is required and the dynamic exhibitions are profoundly improved. Be that as it may, this strategy. In this way, the DPC joined with restrict manipulate can not be applied for packages that require steady replacing recurrence, just like the instance of LCL-primarily based GcCs when you consider that it'll prompt reverberation issues. In addition, this control will prompt high framework current THD esteems during relentless state activity if low mean exchanging recurrence is accomplished [23], [26].

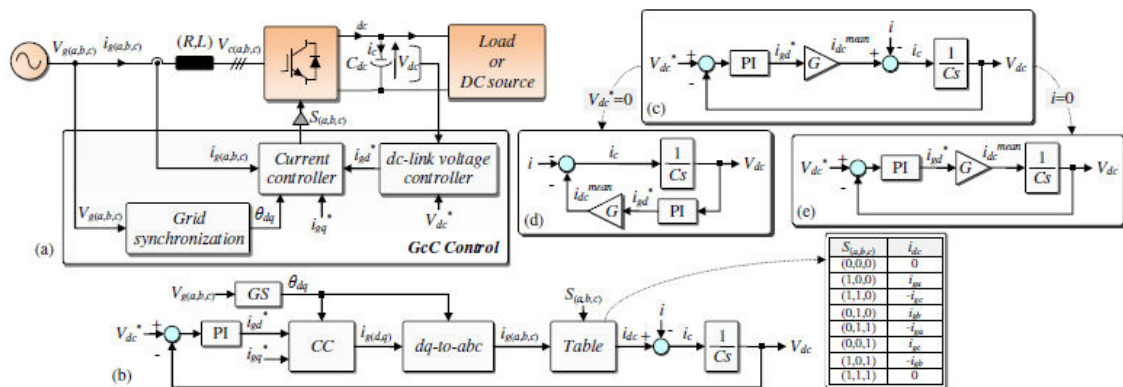


Fig. 1. (a) Commonly used control structure for Grid-connected Converters (b) Model of the dc-link voltage control system (c) Simplified model of the dc-link voltage control system (d) Equivalent simplified model when $V_{dc}^* = 0$ (e) Equivalent simplified model when $i = 0$

This paper proposes an powerful flexible PI controller for the dc-connect voltage control. The bendy idea of the proposed PI controller ensures the numerous manipulate necessities C(1..Four) referenced in the past phase notwithstanding the decrease of network modern THD at some point of enduring state interest, which is for the most element introduced approximately by using

dc-interface voltage controller's yield sign. The corresponding and quintessential will increase Of the taken into consideration versatile PI controller are self-tuned via the running reason of the managed framework or potentially its united states (as an example temporary or unflinching country). For that, a band throughout the dc-joint voltage reference is characterised. At the

factor whilst the planned dc-interface voltage is out of doors this band, the PI additions were selected constants with the cause that an splendid dynamic is achieved. Something else, the PI increases come to be variable in order that the recently referenced compels stay still fulfilled. Additionally, an enemy of windup procedure is included request to forestall enormous overshoot after advance bounces of the dc-interface voltage reference. The remainder of the paper is sorted out as pursue. Area II displays an improved demonstrating, examination and structure of the dclink voltage controller. At that point, area III depicts the proposed versatile dc-connect voltage controller.

2. MODELING, DESIGN AND ANALYSIS OF THE DC-LINK VOLTAGE CONTROLLER

A. Modeling and design of the dc-link voltage controller

The tested framework is portrayed on Fig.1.A, in which L (one after the other R) is the channel inductor (for my part the channel resistor); C is the capacitor of the dc-interface; $V_g(a,b,c)$ allude to the elements of the matrix voltage vector within the everyday reference outline; $i_g(a,b,c)$ allude to the segments of the network present day vector inside the commonplace reference define; $S(a,b,c)$ are the GcC converting states; V_{dc} is the dc-interface voltage; V_{dc}^* is the dc-interface voltage reference; i_{dc} is the prevailing turning out from the energy converter; i_c is the triumphing streaming into the capacitor C; I is the modern-day devoured/created thru the heap/the DC supply associated with the dc-connection; and $i_g(d,q)^*$ are the d and q segments of the lattice current reference within the synchronous reference outline (d,q), in which the d hub is connected to the community voltage vector. Fig.1.A shows

likewise that the control structure of a GcC consists of 3 principle works: the matrix synchronization [21], the present controller [22] and the dc-join voltage controller [11]. Fig.1.B demonstrates the model of the dc-be a part of voltage manage framework. In this decide, GS and CC constitute network synchronization and modern-day controller, one at a time. It thoroughly can be noticed that the dc-join voltage control isn't always as a LTI framework. This is specifically due to nonlinearities supplied through using the idc desk that techniques idc contemporary depending on matrix flows $i_g(a,b,c)$ and related converting indicators $S(a,b,c)$. To improve the model, the connection the various imply estimation of idc (i_{dcmean}) and i_{gd}^* flows is right off the bat decided. This relationship is concluded thru situation (1) [20]. In this condition, PAC is the dynamic strength advocated inside the AC facet of the GcC, V_{gm} is the quantity of the degree voltage, i_{gd} is the d phase of the framework current and PDC is the dynamic strength strengthened within the DC facet of the GcC. Assuming that $V_{dc} \approx V_{dc}^*$ and brushing off the power misfortunes on the GcC and at the interior resistor of the inductive channel ($PAC \approx PDC$), the connection among i_{dcmean} and i_{gd}^* flows can be concluded as appeared in condition (1).

$$\left. \begin{aligned} P_{AC} &= \frac{3}{2} V_{gm} i_{gd} \approx \frac{3}{2} V_{gm} i_{gd}^* \\ P_{DC} &= V_{dc} i_{dc}^{mean} \end{aligned} \right\} \rightarrow i_{dc}^{mean} \approx \frac{3}{2} \frac{V_{gm}}{V_{dc}^*} i_{gd}^* = G i_{gd}^* \quad (1)$$

$$\frac{V_{dc}}{V_{dc}^*} = \frac{\frac{GK_{pdc}}{C} s + \frac{GK_{idc}}{C}}{s^2 + \frac{GK_{pdc}}{C} s + \frac{GK_{idc}}{C}} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2)$$

$$\frac{V_{dc}}{i} = \frac{-\frac{1}{C} s}{s^2 + \frac{GK_{pdc}}{C} s + \frac{GK_{idc}}{C}} = \frac{-\frac{1}{C} s}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (3)$$

$$K_{pdc} = f(\xi, \omega_n) = \frac{2C\xi\omega_n}{G} \text{ and } K_{idc} = f(\omega_n) = \frac{C\omega_n^2}{G} \quad (5)$$

B. Analysis of the dc-link voltage controller

Analysis of the dynamic response to a step jump of V_{dc}^* . Based on equation (2), when a step jump is applied to the dc-link voltage reference value V_{dc}^* , the response of the dclink voltage V_{dc} (initially equal to V_{dc}^{init}) is expressed according to (6) (with $\Phi = \cos^{-1}(\xi)$).

$$V_{dc}(t) = V_{dc}^{init} + (1 + \frac{2\xi}{\sqrt{1-\xi^2}}) e^{-\xi\omega_n t} \sin(\omega_n \sqrt{1-\xi^2} t) - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t} \sin(\omega_n \sqrt{1-\xi^2} t + \Phi) (V_{dc}^* - V_{dc}^{init})$$

$$t_{peak} = \frac{F_1(\xi)}{\omega_n} \text{ and } M_p = V_{dc}(t_{peak}) - V_{dc}^* = F_2(\xi)(V_{dc}^* - V_{dc}^{init}) \quad (7)$$

$$F_1(\xi) = \frac{1}{\sqrt{1-\xi^2}} \text{tg}^{-1} \left(\frac{2\xi + \frac{\xi}{\sqrt{1-\xi^2}} \sin(\Phi) - \cos(\Phi)}{-\frac{2\xi^2}{\sqrt{1-\xi^2}} + \frac{\xi}{\sqrt{1-\xi^2}} \cos(\Phi) + \sin(\Phi)} \right)$$

$$F_2(\xi) = \frac{e^{-\xi F_1(\xi)}}{\sqrt{1-\xi^2}} (2\xi \sin(\sqrt{1-\xi^2} F_1(\xi)) - \sin(\sqrt{1-\xi^2} F_1(\xi) + \Phi))$$

$$V_{dc}(t) = V_{dc}^* - \frac{I_{max}}{C\omega_n \sqrt{1-\xi^2}} e^{-\xi\omega_n t} \sin(\omega_n \sqrt{1-\xi^2} t) \quad (8)$$

$$\left\{ \begin{aligned} t_p &= \frac{1}{\omega_n} \frac{1}{\sqrt{1-\xi^2}} \text{tg}^{-1} \left(\frac{\sqrt{1-\xi^2}}{\xi} \right) = \frac{F_3(\xi)}{\omega_n} \\ t_r &= \frac{1}{\omega_n} \frac{\pi}{\sqrt{1-\xi^2}} = \frac{F_4(\xi)}{\omega_n} \\ M_p &= V_{dc}(t_p) - V_{dc}^* = -F_5(\xi) \frac{I_{max}}{\omega_n} \\ F_5(\xi) &= \frac{1}{C\sqrt{1-\xi^2}} e^{-\xi F_3(\xi)} \sin(\sqrt{1-\xi^2} F_3(\xi)) \end{aligned} \right. \quad (9)$$

C. Analysis of the grid current harmonics

To derive the connection among the output contemporary harmonics and the chosen (ξ, ω_n) values, it shall be noticed that the grid cutting-edge harmonics are suffering from the ripples which can exist inside the dc-link voltage controller output sign.

$$i_{dc} = \underbrace{\frac{3}{4} m I_{gm} \cos(\Phi_1)}_{idc \text{ mean value}} + \underbrace{(\dots + I_{\omega c} \cos(\omega_c t - 3\alpha t + \Phi_{\omega c}^1))}_{HF} + \underbrace{I_{\omega c} \cos(\omega_c t + 3\alpha t + \Phi_{\omega c}^2) + \dots + I_{2\omega c} \cos(2\omega_c t + \dots)}_{HF} \quad (10)$$

$$\tilde{V}_{dc} = \frac{I_{\omega c}}{C(j(\omega_c - 3\omega))} + \frac{I_{\omega c}}{C(j(\omega_c + 3\omega))} + \frac{I_{2\omega c}}{C(j2\omega_c)} \quad (11)$$

$$\left| \tilde{i}_{dc} \right| = \frac{I_{\omega c}}{C} \left| \frac{1}{j(\omega_c - 3\omega)} \right| \times \left| K_{pdc} + \frac{K_{idc}}{j(\omega_c - 3\omega)} \right| + \frac{I_{\omega c}}{C} \left| \frac{1}{j(\omega_c + 3\omega)} \right| \times \left| K_{pdc} + \frac{K_{idc}}{j(\omega_c + 3\omega)} \right| + \frac{I_{2\omega c}}{C} \left| \frac{1}{j(2\omega_c)} \right| \times \left| K_{pdc} + \frac{K_{idc}}{j(2\omega_c)} \right| \quad (12)$$

$$NCCR = \frac{|\tilde{i}_{dc}|}{I_{gm}} = \frac{I_{2\omega c}}{CI_{gm}} \frac{1}{(2\omega_c)^2} \times \underbrace{\sqrt{(2\omega_c)^2 K_{pdc}^2 + K_{idc}^2}}_{NCCR3} + \frac{I_{\omega c}}{CI_{gm}} \frac{1}{(\omega_c + 3\omega)^2} \times \underbrace{\sqrt{(\omega_c + 3\omega)^2 K_{pdc}^2 + K_{idc}^2}}_{NCCR2} + \frac{I_{\omega c}}{CI_{gm}} \frac{1}{(\omega_c - 3\omega)^2} \times \underbrace{\sqrt{(\omega_c - 3\omega)^2 K_{pdc}^2 + K_{idc}^2}}_{NCCR1} \quad (13)$$

Given that $I_{\omega c}$ and $I_{2\omega c}$ are relative to the matrix current size I_{gm} [28] (with a coefficient that relies upon the connected regulation record m), the NCCR relies upon the utilized capacitor, the utilized exchanging recurrence, the utilized adjustment file m and the chose increases K_{pdc} and K_{idc} for the PI controller. The swells around the exchanging recurrence in the dq synchronous reference outline (for example separately $(fc-3f)$, $(fc+3f)$ and $2fc$) become individually $(fc-2f)$, $(fc+4f)$ and $(2fc+f)$ swells in the common reference outline. Accepting that $H_{cc}(s)$ is the shut circle move capacity of the inward current control circle, the framework current will have symphonious substance with a greatness equivalent to $NCCR1 \times |H_{cc}(j(\omega_c - 2\omega))| + NCCR2 \times |H_{cc}(j(\omega_c + 4\omega))| + NCCR3 \times |H_{cc}(j(2\omega_c + \omega))|$.

This symphonious substance will impact the lattice current THD particularly for low dc transport capacitor esteems, low exchanging recurrence esteems and high chose K_{pdc} and K_{idc} gains (when ω_n increments). For the instance of variable exchanging recurrence, it is hard to infer the fundamental consonant substance of the dc-interface voltage. Be that as it may, for a given fundamental consonant substance, the network current THD is impacted in a

similar way as the instance of a consistent exchanging recurrence activity.

3. PROPOSED ADAPTIVE PI CONTROLLER

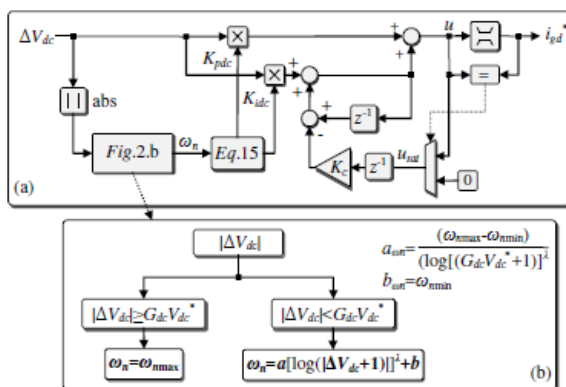
A.Design of the adaptive PI controller

The discrete-time model of the proposed versatile PI controller is given by condition (14). In this condition, the corresponding and essential additions ($\check{K}_{pdc}, \check{k}_{pdc}$) are resolved utilizing a versatile procedure, which is meant to limit the dc-connect voltage homeless people (for example For the duration of transient states) and the lattice contemporary THD (as an instance during steady states). To maintain a strategic distance from huge overshoots of the shipping voltage, in particular after develop hops of the dc-interface voltage reference V_{dc}^* , an enemy of windup adjustment [24] become included.

$$\begin{cases}
 u[k] = \check{K}_{pdc} \Delta V_{dc}[k] + s[k] \\
 s[k] = s[k-1] + \check{K}_{idc} T_s \Delta V_{dc}[k] - \underbrace{K_c u_{sat}[k-1]}_{\text{Anti-windup correction}}
 \end{cases}$$

$$(Sat) \begin{cases}
 \text{if } (u[k] > I_{g \max}) \Rightarrow (i_{gd}^*[k] = I_{g \max}) \\
 \text{elseif } (u[k] < -I_{g \max}) \Rightarrow (i_{gd}^*[k] = -I_{g \max}) \\
 \text{else } (i_{gd}^*[k] = u[k])
 \end{cases}$$

$$\text{if } u[k] \neq i_{gd}^*[k] \Rightarrow u_{sat}[k] = u[k] \text{ else } u_{sat}[k] = 0$$



where k is the k th examining period, igd^* is the network current reference accessible at the immersion yield (Sat), ΔV_{dc} is the dc-interface voltage blunder, T_s is the testing period, $I_{g \max}$ the greatest bearable framework current worth, u_{sat} is the counter windup term and K_c is the counter windup increase. In this work, K_c was set to 0.02. Notice, that lower K_c esteems won't productively wipe out dc-connect voltage overshoots, while higher K_c esteems will influence the dynamic of the dc-interface voltage reaction. For the structure of the versatile PI controller, the damping proportion ξ was right off the bat chosen considering the accompanying requirements: 1) Very little damping proportion (near zero) will bring about oscillatory reaction and 2) Very high damping proportion will result in over damped framework that can influence dynamic exhibitions. A decent bargain between the previously mentioned imperatives is by all accounts a damping proportion ξ somewhere in the range of 0.7 and 1.

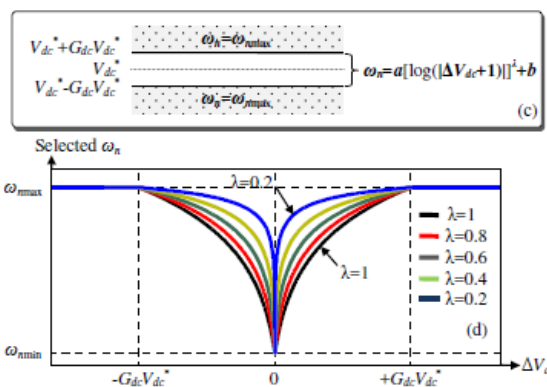


Fig. 2. (a) Adaptive anti-windup PI controller scheme (b) Computation process of the ω_n value (c-d) selected ω_n value according to ΔV_{dc}

The estimations of the higher and lower band points of confinement are equivalent to $V_{dc}^* + G_{dc}V_{dc}^*$ and $V_{dc}^* - G_{dc}V_{dc}^*$, individually. Outside the band, particularly during startup or after advance changes of the dc-interface voltage reference V_{dc}^* , the

normal recurrence ω_n is chosen equivalent to $\omega_{n \max}$. For this situation, the controller is utilized as a standard PI with an enemy of windup activity. Inside the band, the ω_n worth relies upon the size of the dc-connect voltage mistake $|\Delta V_{dc}|$ and is chosen by the capacity given by condition (15). The

primary motivation behind this capacity is to build the chosen ω_n esteem when the extent of the dc-interface voltage blunder $|\Delta V_{dc}|$ increments during transient states. Then again, during unfaltering states, when $|\Delta V_{dc}|$ is close zero, the chose ω_n worth must be roughly equivalent to ω_{nmin} to prompt a low network current THD.

$$\begin{cases} \omega_n = a[\log(|\Delta V_{dc}|+1)]^\lambda + b & \text{if } |\Delta V_{dc}| \leq G_{dc}V_{dc}^* \\ \omega_n = \omega_{nmax} & \text{if } |\Delta V_{dc}| > G_{dc}V_{dc}^* \end{cases} \quad (15)$$

where $(0 < \lambda \leq 1, a = \frac{(\omega_{nmax} - \omega_{nmin})}{[\log(G_{dc}V_{dc}^* + 1)]^\lambda}, b = \omega_{nmin})$

How to set the parameter G_{dc} ?

The voltage rating of the dc-connect voltage capacitor and GcC power switches is figured under unique conditions with a fitting security factor. When all is said in done, 10% overshoot of the dclinkvoltage is considered under unique conditions. To this reason, the Gdc increase (characterized As the 1/2 of the share between the band well worth and Vdc*) is picked with the purpose that the dc-join voltage variances remain decrease than 10%Vdc*, even after surprising and severe changes of the information contemporary I. This implies, after a level leap of the data modern I equivalent to its maximum excessive worth $\pm I_{max}$, the dc-join voltage Vdc have to live in the band $\pm G_{dc}V_{dc}^*$ around the dc-interface voltage reference Vdc*.

How to set the parameter ω_{nmax} ?

As referenced beforehand, The dynamic of the CC circle is anticipated extraordinarily quick with understand to that of the dc-be part of voltage control circle. The time regular τ_v of the dc-interface voltage manage circle is same to $1/\text{Re}(p(1,2))=1/(\xi\omega_n)$. Accepting that τ_i is the time constant of the CC circle, the time steady τ_v have to be extra outstanding than $10\tau_i$. In this work, the time steady of the utilized CC circle τ_i is lower than 1ms. So

as to accomplish a period consistent τ_v more prominent than 10ms, the ω_n value must be lower than a most extreme worth ω_{nmax} equivalent to $1/(\xi*10\text{ms})$. Along these lines, the ω_{nmax} worth is chosen equivalent to $142.86 \text{ rad/s} = 2\pi 22.73 \text{ rad/s}$.

How to set the parameter ω_{nmin} ?

The ω_{nmin} worth can be resolved with the goal that the reaction time t_r (given by condition (9)) don't surpass a fair limit, even after greatest power load association/separation. In this work the bearable furthest reaches of t_r is set multiple times the lattice time frame ($t_r=10*20\text{ms}=200\text{ms}$). For a ξ worth set to 0.7 and dependent on condition (9), ω_{nmin} is equivalent to $21.99 \text{ rad/s} = 2\pi 3.5 \text{ rad/s}$.

How to set the parameter λ ?

Reenactments are done so as to look at the exhibitions of the versatile PI controller (counting the counter wrap up activity) With the ones of the usual PI controller. The utilized reenactment parameters are delineated on Tab.1 and the acquired duplicate outcomes are appeared on Fig.3. Fig.Three.A contrasts among recreations consequences obtained and the same old PI manipulate (for constant PI additions tuned for $\omega_n=\omega_{nmin}$ and $\omega_n=\omega_{nopt}$) and people got with the proposed versatile PI control. The common recurrence ω_{nopt} is resolved so that, when a stage bounce equivalent to I_{max} is connected to the information currenti, the subsequent Mp worth is equivalent to $G_{dc}V_{dc}^*=10\%V_{dc}^*$. In this way, in view of condition (9), ω_{nopt} is processed as pursues

$$\omega_{nopt} = F_5(0.7) \frac{I_{max}}{G_{dc}V_{dc}^*} = \frac{416.88 \times 1.25}{0.1 \times 150} = 34.74 \text{ rad/s} \quad (16)$$

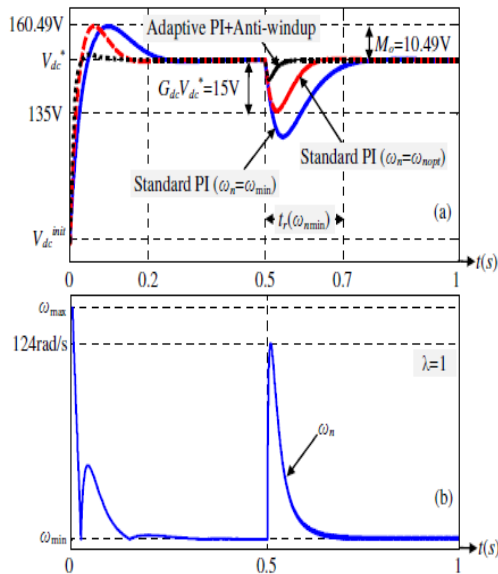


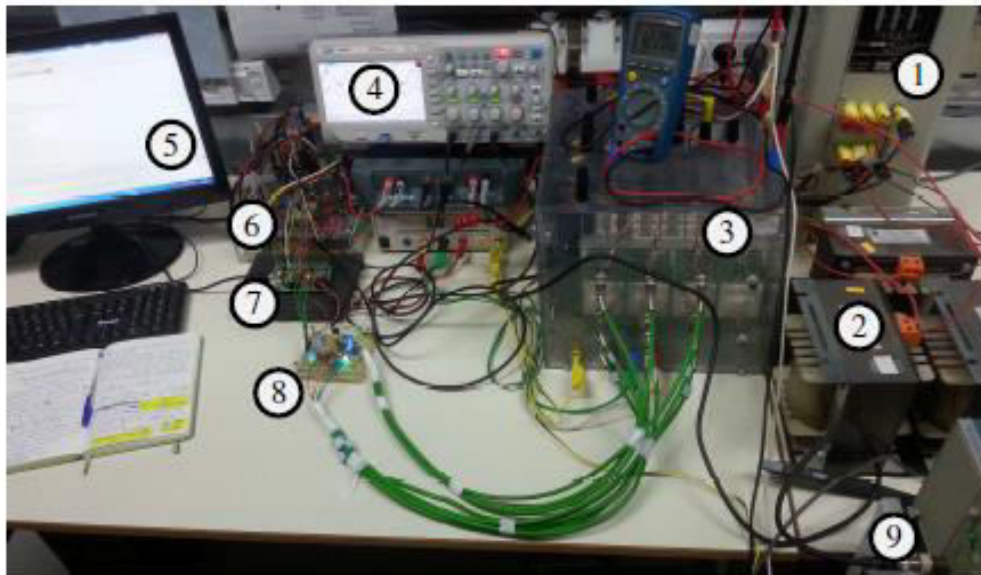
Fig. 3. Simulation results ($\zeta=0.7$, $V_{dc}^{init}=100V$, $V_{dc}^*=150$, $i=0$ at $t=0s$ and $i=I_{max}$ at $t=0.5s$) (a) Comparison between standard PI control and adaptive PI control (b) waveform of the selected ω_n value for the adaptive PI controller

TABLE I: SYSTEM PARAMETERS

| Symbol | Description | value | unit |
|-----------------|---|--------------|----------|
| S | GcC rated power | 20 | kVA |
| L | Inductive filter | 40 | mH |
| C | Dc-link voltage capacitor | 1100 | μF |
| Z_{load} | Load Impedance | 120 | Ω |
| I_{max} | Maximum load current | 1.25 | A |
| V_{dc}^{init} | DC-link voltage initial value | 100 | V |
| V_{dc}^* | DC-link voltage reference value | 150 | V |
| G_{dc} | Ratio of the DC-link voltage band | 10 | % |
| λ | Used coefficient for ω_n computation | 1 | - |
| ω_{max} | Maximal natural frequency | $2\pi 22.73$ | rad/s |
| ω_{opt} | Optimal natural frequency | $2\pi 5.35$ | rad/s |
| ω_{min} | Minimal natural frequency | $2\pi 3.5$ | rad/s |
| ζ | Damping ratio | 0.7 | - |
| K_c | Anti-windup coefficient | 0.02 | - |
| T_s | Sampling period | 50 | μs |

Fig.3.b shows the waveform of the chose ω_n esteem for the versatile PI controller. Notice that ω_n is practically equivalent to ω_{nmin} during unfaltering state activity. During transient states it builds significantly and winds up equivalent to ω_{nmax} when the extent of the dc-connect voltage mistake surpasses as far as possible (during startup).

4. EXPERIMENTAL RESULTS .



- ① Autotransformer ② Inductors ③ GcC ④ Scope ⑤ Host PC
- ⑥ Measurement board ⑦ Microcontroller ⑧ Resistive load
- ⑧ Switching signals interface board

Fig. 4. Experimental set-up

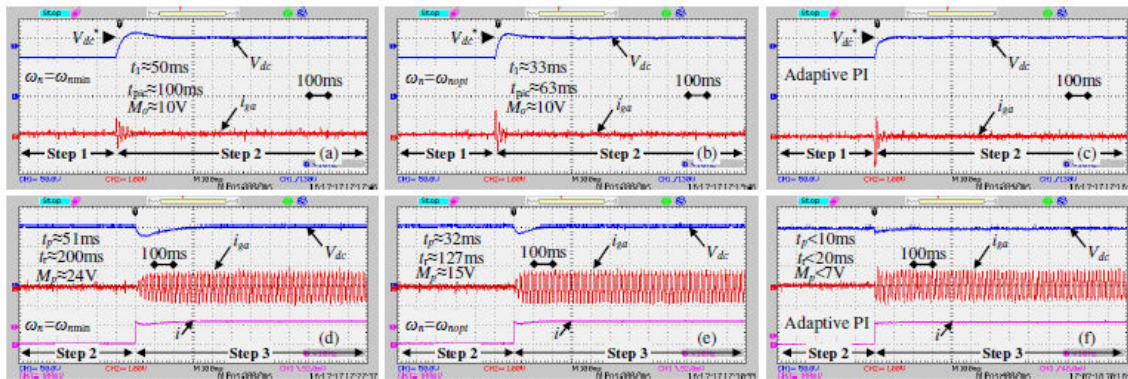


Fig. 5. (a-b-c) DC-link voltage V_{dc} (50V/div) and grid current i_{gd} (3.28A/div) waveforms during steps 1 and 2 (a) Standard PI controller ($\omega_n = \omega_{min}$) (b) Standard PI controller ($\omega_n = \omega_{opt}$) (c) Proposed adaptive PI controller (e-f-g) DC-link voltage V_{dc} (50V/div) and grid current i_{gd} (3.28A/div) waveforms during steps 2 and 3 (e) Standard PI controller ($\omega_n = \omega_{min}$) (f) Standard PI controller ($\omega_n = \omega_{opt}$) (g) Proposed adaptive PI controller

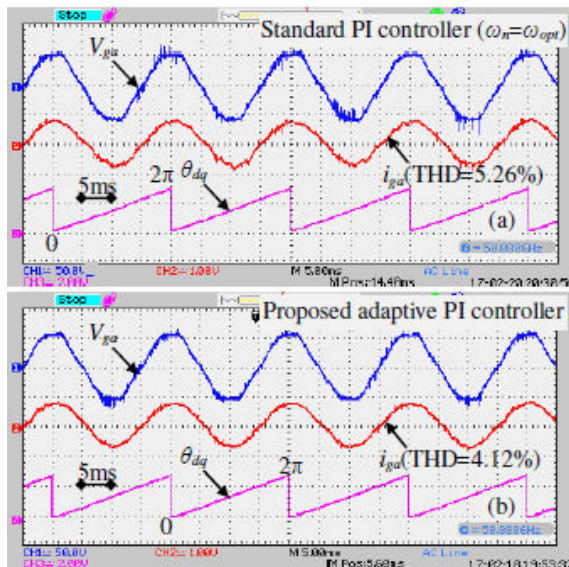


Fig. 6. Grid voltage V_{ga} (50V/div), grid current i_{gd} (3.28A/div) and grid voltage position θ_{dq} waveforms during steady state operation and using (a) a standard PI controller tuned for $\omega_n = \omega_{opt}$ (b) the adaptive PI controller.

5. CONCLUSION

This paper exhibited an improved dc-link voltage controller relying on a flexible PI controller with an enemy of windup approach. The relative and indispensable additions of the proposed PI controller are self-tuned so the accompanying imperatives are fulfilled: 1) no overshoot after improve hops of the dc-interface voltage reference enter; 2) quick unique reaction after enhance bounces of the dc-be a part of voltage

reference; 3) short powerful response after growth hop of the statistics contemporary I and four) low lattice modern THD esteem during relentless us of a interest. The taken into consideration control have become tentatively attempted on a prototyping level. The obtained take a look at outcomes are very much like hobby effects and exhibit the viability and unwavering excellent of the acquired control technique.

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