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Title **DESIGN AND ANALYSIS OF 16 BIT PIPELINE BY USING CMOS TECHNOLOGY**

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DESIGN AND ANALYSIS OF 16 BIT PIPELINE BY USING CMOS TECHNOLOGY

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CONJECTURAL:

In This manner we discuss about the analog to digital converters by designing a 16-bit pipeline by using the "Split ADC architecture system level design of ADC component to invent the attributes of analog to digital converters in matlab it is basic function in an system level to verify the activity of ADC.it is an nonlinear we are invited.

1.ESTABLISH:

In analog to digital converters are using word Hippo in digital communication modern communication the advantage of CMOS technology to be led to the execution of signal process with low cost and high yield..this is produce for low power and low voltage sub antonyms, CMOS automation. The major project is to plan of manufacture in 16 bit 10mhz pipeline ADC transfer to CMOS manufacture for planning a pipeline ADC .it comes from desired characteristics of the function to novel "split."

The ADC construction using nonalgorithm Analog to digital converter.

In this design the components are present:

1.The system level characterization prior of ADC.

2.designing level of analog subsystem.

3.The fabrication of integrated circuits.

4.Implementation of digital functions.

5.Integrated circuit testing the data implementation.

This report contains implementation of regarding our design results and conclusion drawn In addition,it out lines prior work in this field and layout for the future of this project

2.FRAMEWORK INFORMATION

The purpose of this section is to provide an introduction to the key issues relevant to our project. The first section covers ADCs, followed by Pipeline ADCs, and prior work.

ADCs(analog to digital converter)

In analog to digital convertors the realword till continue analog signal such as temperature and voltage converted into digital represent that can be processed transmitted and stored.

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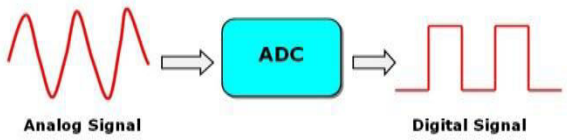

Fig 1: ADC convertor

Simply put, The analog to digital convertor samples an analog type wave form at the unit time and digital values in every sample. This is given by the ratio of during conversion, signal effect into one of finite no of discrete level of separate by one LSB code. this process ,also known as quantization ,results in a finite resolution known as the quantization error(Q.E).

There are many different ADC design, but they all fall under two categories the signals at the minimum sampling rate, whereas over-sampled converters take more samples than required to achieve high resolution. The table below summarizes different ADC architectures.

2.2 PIPELINE ADC

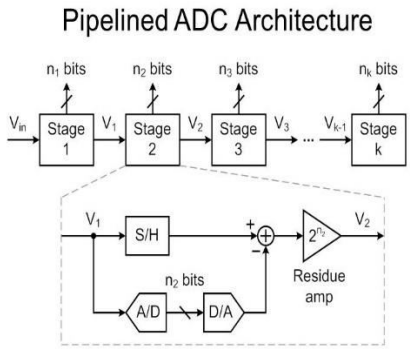

FIG 2: Pipeline ADC

The pipeline ADC has four types and produces 4-bits with a 1-bit overlap, hence an effective 3-bits. In this the result, are four types together yield an effective 12bits.

The last four four bit light ADC supply the last four bits of the total sixteen bits that require from pipeline Analog to digital convertor. In this the advantage of pipeline ADC is more then two operation can carried out. Al though this complete converter of analog input to the digital values take through this stages. the next stage of this convert to one analog voltage can be produced alternative with this stages of a subsequence convertor. In each and every stage the pipeline Analog to digital converter, the first stage is converted in to the analog voltage input to discrete values. In this the carried through out a four bit light analog to digital converter. The discrete values are send through digital convertor to compare with the actual input voltage of the stages. The differences between the input voltage and voltage result from digital converter. from both ADC and DAC. The error is amplified by the appropriate gain factor, the subsequent stage of the pipeline ADC as the input voltage to the next stages.

2.3.PRIOR WORK:

A 12-bit 10MHZ Pipeline analog to digital converter using Open-Loop Residue Amplification was proposed to do digital background calibration. This technique is used as an enabling element to replace precision amplifiers by simple power power-efficient open-loop stages. A key difference between [4] and previous closed-loop designs is that the residual charge packet on the capacitive array is not redistributed onto a feedback capacitor, but is fed directly into a resistively loaded diff-pair to produce the desired full-swing residue voltage.

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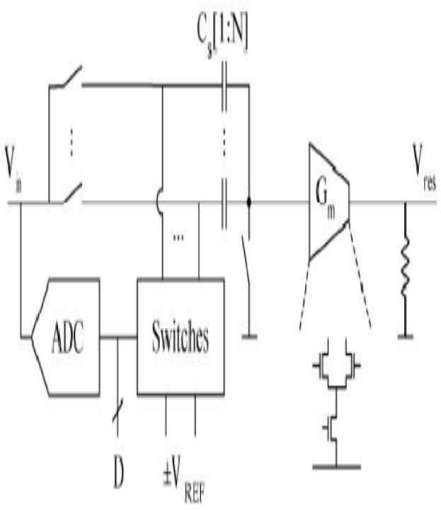


FIG 3: Prior work of ADC

The non-idealities that arise from the resistively loaded diff-pair stage are corrected digitally, there by moving complexity into the digital domain, which is the preferred tradeoff in IC Design.

The work in uses a 3V supply rail, and a 0.35µCMOS process. In addition, the 1st stageimplementation is used to implement a 12-bit 100MHz Pipeline ADC. Our design is different from in that a 2.5V supply and a 0.25µprocess are used to design a 16-bit 10 MHz Pipeline ADC.

3.Characterization of a Pipeline ADC:

3.1.Linear Vs Non-Linear Gain Stage:

It consist of the code that was used to a 16-bit pipeline analog to digital converter. The below figure illustrates the output code of stage. it is the function of the analog input voltage. The figure clearly shows the 16 different levels that are associated with this ADC. The general difference between these two kinds of gain stages is shown in the below. Around the edges of each level,

FIG 4: Non linear Histogram

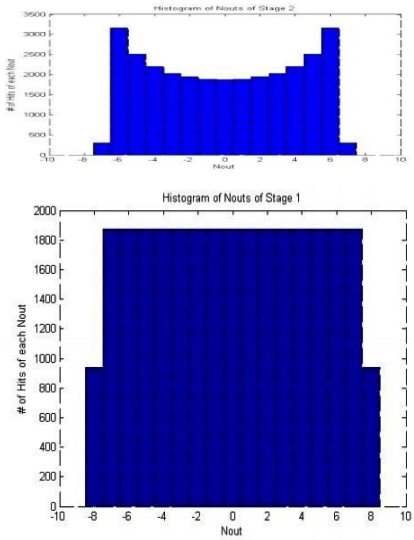
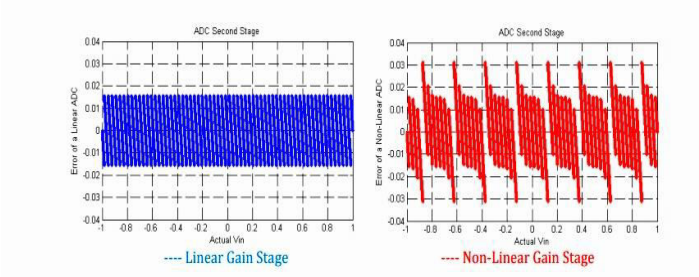


FIG 5: Linear Histogram



Finally, we can also see the non-linear relationship between the error of a stage and the input voltage to the pipeline ADC. The figure below illustrates that with a linear gain stage, the error associated with each code level is the same throughout. However, since the codes begin to deviate away from the edges of the 16-levels we see that there is more error associated at the
edges of these 16-levels.

3.2.Non Linearity of The ADC:

the amount of non-linearity that we will be working with, we simulated a cascade differential pair (see next section) and conducted a DC sweep to measure its output

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voltage as a function of the input voltage to arrive at a transfer characteristic. Non-linearity are better measured when one looks at the difference between the non-linear gain stage and a linear-best fit line. Any difference between these two will show the amount of non-linearity that exists in the non-linear gain stage, i.e. the cascade differential pair. The figure below shows the simulated data along with the linear best fit line. It also shows the residuals, the difference between these two lines.

3.3.Cubic Approximation of Simulated ADC:

One method of correcting non-linearity is by using a cubic approximation of the simulated data. The figure below shows this cubic approximation and the amount of error that result from the difference between the simulated data and the approximation.

The max residual is approximately 80µV.Correcting the non-linearity with a cubic approximation drastically reduces the non-linearity that exists in the simulated data. From a maximum non-linearity of 1.5mV, we were able to reduce the non-linearity with a cubic approximation such that the max non-linearity after correction was only 80µV.

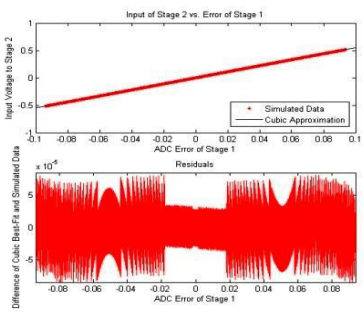

FIG 6 : Cubic approximation data

3.4Digital Look up Table:

As an alternative to the Cubic Approximation method, a digital look up table (DLT) was implemented with some matlab algorithm (attached in Appendix A). This algorithm uses a known list of Doubts (Code outs) to figure out the original Vin that caused these codes using an initial guess. The figure below shows the percentage error that was evident from using this procedure for each Vin. These minimal percentage errors show that the DLT is another alternative to the cubic approximation that has been implemented above.

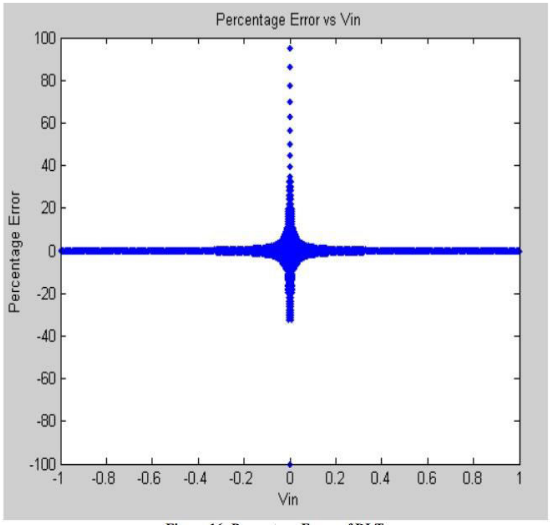

FIG 7 : Percentage Error of DLT

4.Circuit Level Simulation of the Analog Subsystem:

The Common Mode Feedback, Replica Bias, and the Switched Capacitor Network were simulated in Cadence. This section explains the design of each of these blocks in detail. The stage1 implementation from is repeated here for convenience.

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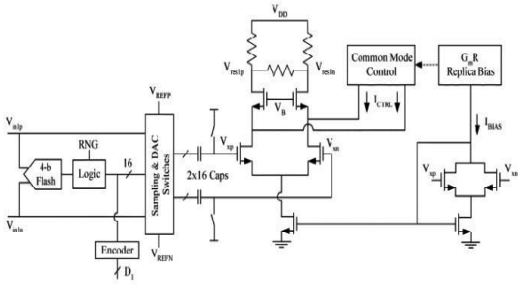


FIG 8 : Implementation of Pipeline ADC

4.1Basic Differential Pair Circuit:

The analog subsystem design began with the simulation of a resistively loaded differential pair circuit. As explained in the Prior Work section, a resistive load was preferred to an active load due to deep-submicron compatibility. The low supply voltage (2.5V and Ground) leaves little headroom for a load transistor causing it to easily turn off. A resistively loaded approach means that the high-gain requirement of the diff-pair should be relaxed and the non-linearity arising from this stage corrected digitally.

The differential pair circuit specifications were as follows:

- Differential Mode gain = 8
- Input Bias Voltage = 1.25V
- Input Voltage Swing = +/-1.5 V
- Output Bias Voltage = 2 V
- Output Voltage Swing = +/- 0.4 V
- Bias Current = 200uA
- Rail Voltages = 2.5V, GND

The gain requirement is not stringent, meaning that proximity of 8 is acceptable. This is again a big advantage in terms of design because a precision amplifier will increase analog complexity where as the present design with its continuous digital background calibration will estimate and remove imprecision errors digitally. The first simulation was that of a simple differential pair circuit. Please see Appendix A2 for circuit parameters. The simulated diff-pair circuit is shown below:

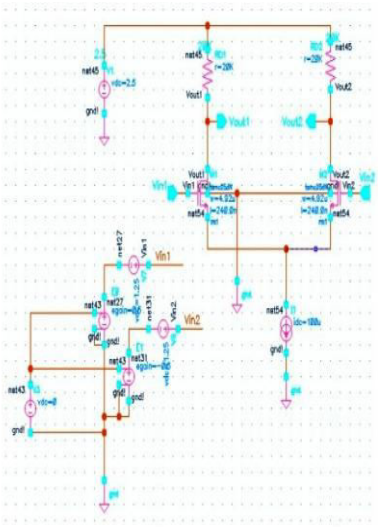
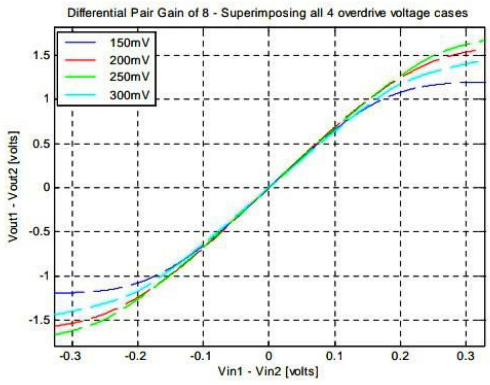


FIG 9: Circuit Schematic of a Diff-pair



The general pattern that is evident from superimposing all 4 VOV cases is that the linear range of the differential output increases with increasing VOV. The slope near the operating point (i.e. differential gain) in all the cases is approximately 8 as expected because the load resistor values were adjusted in each case to yield a gain of

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8. However the output bias voltage will naturally change with varying load resistor values because of the varying voltage drop across the load. It is obvious then that only 1 of 3 diff-pair specifications can be met with a basic diff-pair circuit:

• Differential Mode Gain

• Output Bias Voltage

• Output Voltage Swing

Achieving all 3 specifications would require a more complex design, which is covered in the next section In terms of a cubic approximation for the differential output signal, the following plots for differential output and residue were produced (input voltage steps of 0.001Volts). Since the differential input is fed into a 4-bit Flash ADC (16 levels) the input signal swing is be +/- 1.5 V, there are 3/16 = 188mV in each code level Therefore the differential input range of +/- 94mV is of primary concern.The following plots show the differential output and residue versus differential input for all 4 VOV cases.

4.2. Cascade Diff Pair with Pi Resistor Network:

As shown in the previous section, a design that controls differential gain, output bias voltage and output swing independent of each other is desired. In addition, a design that decreases the Max Residue for an overdrive voltage of 300mV below that of the 250mV case would be useful.To verify this hypothesis, a cascade gain stage was added to the diff-pair. A cascade has two main properties:

1. High Output Impedance, resulting in high gain.

2. Limiting the voltage across the input transistor.

To illustrate the first property, a simple common source amplifier is simulated with and without a cascade. As shown below, the non-cascade curve has a positive slope in the active region whereas the cascade has an almost zero slope. Since the output impedance is given by the inverse of the slope, it is obvious that the cascade has produced very high (ideally infinite), the addition of a cascade did very little to improve the shape of the curve.

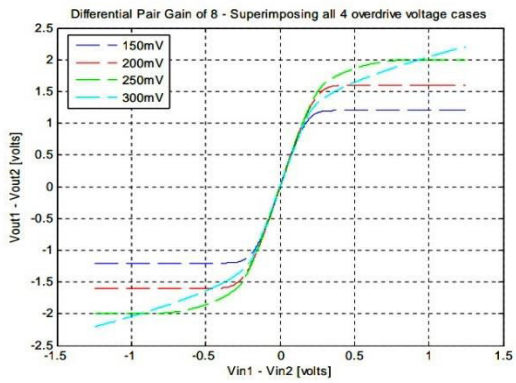

FIG 10 : Diff-Pair Output vs Input

One possible explanation for this behavior is that in the small signal model, the high output impedance of the cascade stage is placed in parallel with the resistive load of the diff-pair. Therefore the maximum effective output resistance of the diff pair is dominated by the resistive load. By increasing the resistive load, however, will

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lead to a lower output bias voltage, and will cause the input MOSFETS to crash into triode.To overcome this issue of gain versus output bias, a Pi-Resistor configuration isused, which is basically a resistor that connects both the outputs. This extra resistor, RG reduces the gain because in differential mode RG/2 is placed in parallel with the load resistor, RB. Nevertheless in common mode RG is Open, and only RB controls the output bias voltage. As a result RB is picked to be a large enough resistor, i.e.RB ‖ RG/2 > RDwhere RD is Gain/Transconductance. RG, which is used to knock down the gain to a desired level is then picked accordingly to satisfy the above equation.In addition, An increase in ID will increase the across the load resistors, and will bring down the output bias voltage causing the MOSFETs to crash.Therefore, ID needed to be changed in a way that satisfies the Voltage Swing condition but keeps the output bias at 2V and the input MOSFET trans conductance at 800µA/V.

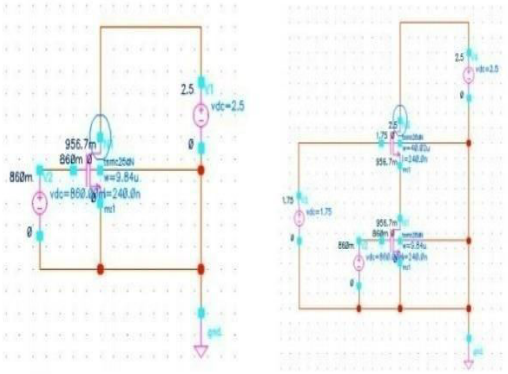

FIG11 : Simple and Cascaded Source Circuit

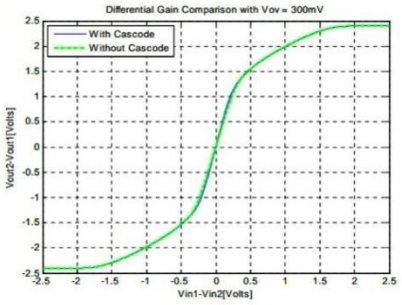

FIG 12 : Diff-pair Characteristics

4.3. Common Mode Feedback & Replica Bias the enhanced of the output resistance, to the basic output biasing point is unstable and highly sensitive to supply voltage variations and complementary device mismatches. The dc overcome this drawback, common-mode feedback is used for bias stabilization and a Replica-Tail Feedback technique to keep the tail current constant despite variations in the input common mode voltage level. If VOCM increases, the CMFB current is reduced accordingly to bring VOCM back to 2V. Similarly, a decrease in VOCM will cause the CMFB to pump additional current to bring VOCM back to 2V. This circuit works in a negative feedback loop,

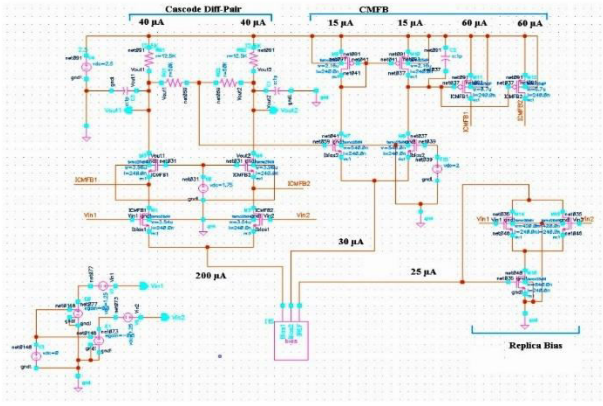

FIG 13 : Replica bias Circuit

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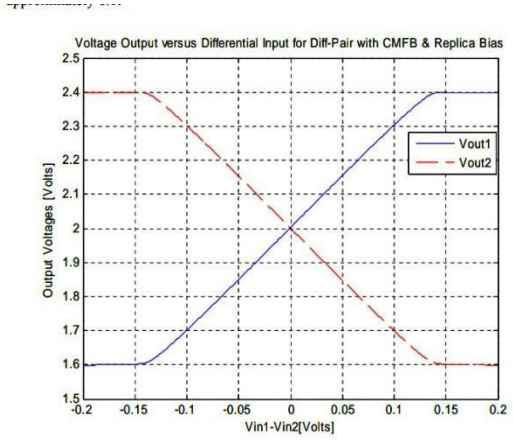

FIG 14 : Output vs Input for Replica Bias

4.4. Switched Capacitor Network

The networks have become very popular due to their accurate frequency response as well as good linearity and dynamic range. Filter coefficients of a switched capacitor network can be easily obtained as they are determined by capacitance ratios which can be set very precisely on an integrated circuit (with an order of 0.1 percent error). By modifying the capacitance ratios, we can change the settling time and also the frequency response of the entire network. Moreover, a switched-capacitor network takes up a dramatically less amount of die-area as compared to a simple RC integrator, which may serve the same purpose. A smaller amount of die-area also results in a lower cost as size is very costly in IC manufacturing industry The schematic of our initial block is shown below. This circuit has two main phases. In phase 1 (P1), the capacitor is sampling the input voltage relative to 1.25V. capacitor adjust to correct for the DAC voltage levels. Although complicated, this process occurs systematically.

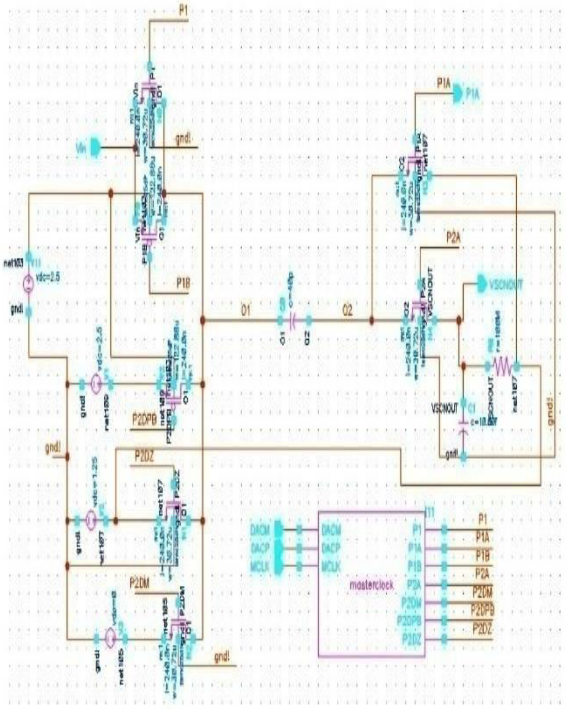

FIG 15 : Switched Capacitor Network

The potential to the left of the capacitor, O1, the set to the input voltage of Sample and Hold Circuit. This separation of charge between the capacitor plates charges up the capacitor, 1.25Vbeing supplied. When the capacitor has charged up to the correct voltage, then P1 turns off and P2 turns on. At Phase 2, the voltage at the capacitor switches to the correct DAC voltage level (0V, 1.25V or 2.5V) as determined by the DAC. There are two signals from the DAC that indicate whether a signal is closer to a low, mid or high voltage. The truth table of this is shown below.

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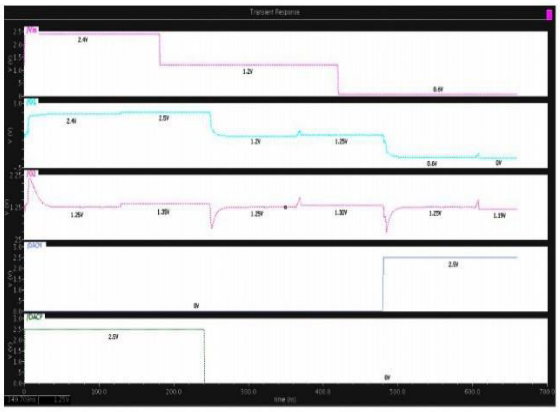

FIG 16 : Transient Analysis of SCN

5. Quantizer

The design of the pipeline ADC consists of a 4-bit quantizer. The following circuit is a 2-bit quantizer designed by Tsai Chen, and we are in the process of modifying it to 4-bit. In this design the voltage reference levels are set by mismatches in the current sources.

An alternative approach that was implemented in a 3-bit pipeline ADC by Thomas Liechti uses a differential difference amplifier with a 2 Vpp differential signal (1Vpp single ended) and centered about Vdd/2 (=0.9V).The voltage levels are generated using a resistive ladder and this work for our designing process.

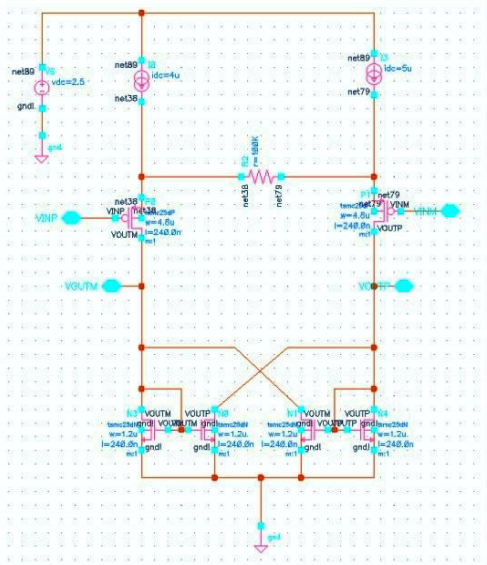

FIG 17 : Preamp for the Quantizer

6. Conclusion

This design made significant in our aim to design a 16-bit 10MhzPipeline ADC.

• This majority of analog subsystem of the ADC in Cadence.Due to the complexity of the project and the various hurdles we came upon during the design phase, we did not have enough time to be able to achieve all the goals we set out to meet initially. Some of the work that still needs to be completed includes the fabrication work including the lay out work of the analog subsystem. Once the fabricated IC has been received, further work will be needed for data acquisition using a software package similar to Lab view. Further on the final design block to verify its performance.

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