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PV CELL FED HIGH GAIN SINGLE STAGE BOOSTING INVERTER FOR INDUCTION MOTOR DRIVE APPLICATION

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Abstract- For very high voltage gain of a Photo-Voltaic system, this paper proposed a high gain single stage boosting inverter for induction motor drive application. Easy control capability, optimum size, affordable cost with high voltage gain made the system employable. AC voltage conversion is achieved along with boosting of DC voltage of Photo-Voltaic system of inverter. The proposed system consists of a high voltage gain - high efficiency - switched inductor boosting converter (SIBBC). The proposed converter switch is derived with a sinusoidal modulation, so that the converter output voltage is a rectified sine wave which requires only a folded cascade as a second stage. The proposed system is used to connect the PV module to the grid with achieving maximum Power Point Tracking (MPPT) control; AC module. The converter operates in DCM to inject a sinusoidal current into the grid with unity power factor. The proposed dc-ac system has some advantages such as low cost, small size and simple control. In addition, the grid connection, MPPT, and unity power factor controls are executed through only one switch, the converter switch. Minimization of switching losses is employed with only two switches and operated at very high frequency. Easy control capability, optimum size, affordable cost with high voltage gain made the system employable. The proposed SSBI is fed with Photovoltaic system and connected to Induction motor, the overall circuit model is simulated in Matlab/simulink software and the results are analysed.

Key words: Bipolar voltage multiplier (BVM), hybrid boosting converter (HBC), nature interleaving, renewable energy, single switch single inductor, Induction motor drive.

I. INTRODUCTION

Solar energy is converted to electricity using an electronic device called solar panel using photo-voltaic effect. PV applications can be grouped into utility interactive and stand-alone applications [1]. Utility interactive applications provide a backup system to ensure that electricity is produced throughout the year irrespective of the weather conditions. While stand-alone

systems without the utility connection uses the electricity where it is produced [2]. However, to cater to the energy needs during non-sunny and cloudy period PV-charged battery storage system is used. PV systems with batteries can be used to power dc or ac equipment [3-5]. PV systems with battery storage are being used all over the world to power lights, sensors,

recording equipment, switches, appliances, telephones, televisions, and even power tools [6]. PV serves as an ideal source using the availability of low DC power requirement for mobile and remote lightning requirements [7]. Systems using several types of electrical generation combine the advantages of each. Engine generators can produce electricity anytime. Thus, they provide an excellent backup for the PV modules, which produce power only during daylight hours, when power is needed at night or on cloudy days. On the other hand, PV operates quietly and inexpensively, and it does not pollute [8]. In this paper a model of closed loop implementation of PI controller for hybrid boosting converter is presented. This controller maintains constant output voltage of the converter near to the utility voltage [9-10]. The input voltage to the converter is fluctuating between 20-45V, according to the sunlight intensity on PV cell. MATLAB based simulation is developed with PI controller. The need for energy in the present day scenario is never ending. This is certainly true in case of electrical energy, which stands as the largest one in total global energy consumption. The demand for electrical energy is increasing twice as fast as overall energy use and is likely to rise to 76% by 2030 from 12.5% in 2014. This situation can be managed only with the use of renewable energy sources as wind, tidal, solar etc [1]-[3]. Another concern is that in many overpopulated countries like India, there is a over usage of limited power generating resources and as a result many cities and towns are facing constant load shedding and blackouts. The existing power generation units are not sufficient to meet

the continuously rising power demand. The wide gap between generation and distribution location lead to the inefficiency in supplying power to the rural areas. This can be eliminated only by the use of advanced techniques in power electronics by providing uninterrupted power supply to the users by providing flexibility in source by placing the inverters [4]. Here the general PV system In order to convert and connect the solar energy to the grid, the low voltage of the PV panel first has to be stepped up significantly to match the utility level. This poses a challenge to the designer of PV inverters as the traditional boost converter cannot provide the required gain at high efficiency. Therefore, an extensive research effort is dedicated to developing various topologies of high step-up dc-dc converters [5]-[7] that can be used in tandem with a half- or full-bridge inverter [8] to implement a solar power generation system.

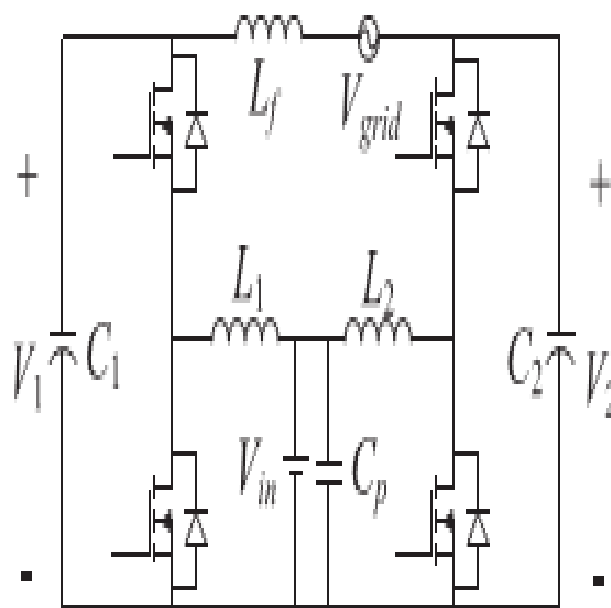


Fig.1. Topology presented in [15]

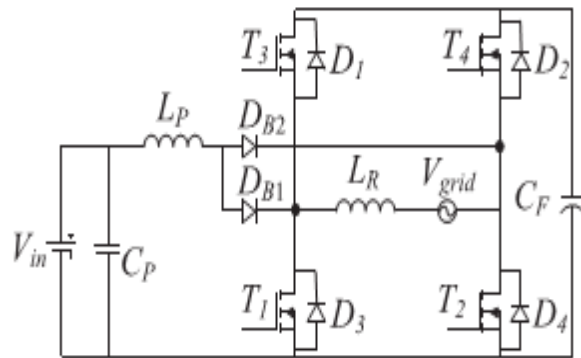


Fig.2. Topology presented in [17]

Another concern, typical to single-phase dc-ac power systems, is ac-dc power decoupling problem. A traditional solution is application of a decoupling capacitor on the dc-link between the input and output stages. The value of the decoupling capacitor depends on the rated power P_{dc} , the line frequency f , the average voltage across the capacitor V_{dc} , and the allowed peak-to-peak ripple Δv [9]

$$C_{dc} = \frac{P_{dc}}{2\pi f V_{dc} \Delta v} \quad (1)$$

The two-stage or the multistage micro inverters can have their decoupling capacitor on the high voltage dc link, and, according to (1), attain lower value of the decoupling capacitor [9]. However, some single stage micro inverters may require placing the decoupling capacitor at the PV module terminals. The low panel voltage, V_{dc} , and the desired low ripple, Δv , see (1), result in a substantial decoupling capacitor value and size (e.g., 2.4 mF for $V_{dc}=35V$, $\Delta v=6V$, and $P_{dc}=160W$ [1]). In field conditions, large electrolytic capacitors have short life and impair system's reliability. Therefore, the power decoupling problem becomes one of major concerns in micro

inverter design. Application of small non-electrolytic capacitors is strongly desired. To minimize the decoupling capacitor, additional power decoupling circuits were suggested in literature. A flyback-type single-stage topology with an additional power decoupling circuit proposed in [10] reported a decoupling capacitor of only 40 μF . However, the efficiency was only 70%. An improved topology employing leakage energy recycling [11] demonstrated 86% peak efficiency. Some other flyback-based topologies [12]–[14] also make use of an additional power decoupling circuit.

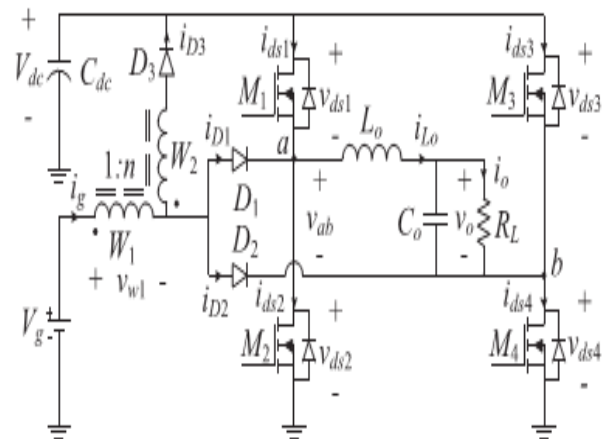


Fig.3. Topology of the proposed SSBI.

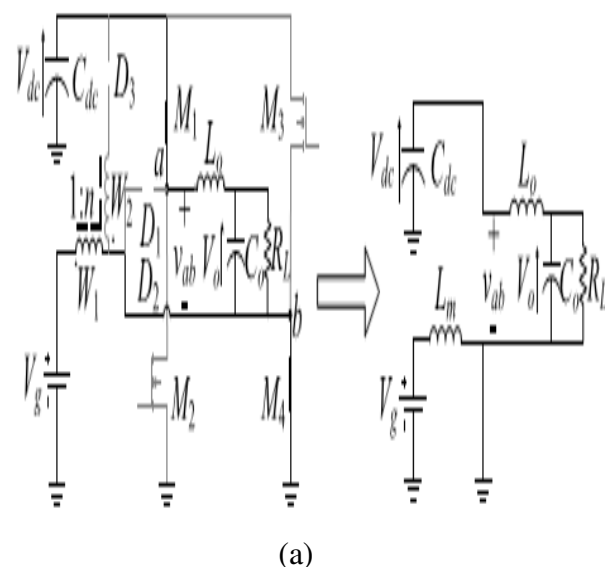
Single-stage topologies that can realize voltage step-up and inversion in a single stage were proposed in the past. In [15], a dual boost inverter was suggested. Here, the load is connected differentially between the outputs of two bidirectional boost converters (see Fig. 3.1). As a result, the topology resembles a common H-bridge with the boosting inductors connected to the legs' midpoints. The demerits of this approach are the limited dc step-up gain; circulating currents, which impair the efficiency; and somewhat complicated

control. Since the function of C_1 and C_2 is merely output filtering, the decoupling capacitor should be placed at the low voltage input, which is an additional disadvantage. Another single stage solution [16], [17] is shown in Fig. 2. Compared to [15], the topologies in [16] and [17] use a single boost inductor; have no circulating currents; have a high voltage dc link and, accordingly, a smaller decoupling capacitor. Also, traditional control methods can be applied. Moreover, the topologies proposed in [18] and [19] may provide other choices for single-stage solutions. However, the limited dc step-up of [15]–[19] necessitates using a more expensive high-voltage PV panels with 70–100 VDC output in order to get the desired dc-bus voltage compatible to grid-connected inverters. Alternatively, using the popular crystalline silicon modules with the 25–50 VDC MPP range, these topologies can implement a two-three panel string inverter, which, as any string architecture, is prone to the mismatch problem. In this paper, a single-stage boosting inverter (SSBI) is proposed for alternative energy/solar power generation. SSBI can be regarded as further improvement of [16] and [17]. SSBI can attain higher dc gain and, thus, operate off low dc input voltage of a single PV panel. By its concept of operation SSBI shares the switches of the power train in a manner that allows merging the dc–dc step-up converter stage and the grid-tied dc–ac inverter stage. Hence, SSBI is realized in a single stage. The power decoupling is performed at high voltage; thus, low value of dc-link decoupling capacitor is required. The SSBI easily lends itself to application of one cycle

control (OCC), which helps attaining high-quality ac output regardless of low frequency ripple across the dc link. However, any other control method can be applied. This paper presents theoretical analysis, simulation and experimental results obtained from a stand-alone 200 W prototype.

II. Description of the Proposed Topology

The proposed schematic diagram of the proposed SSBI is given in Fig.3, which is an improvement of the scheme given in [16] and [17]. SSBI is comprised of semiconductor switches $M1..4$, arranged in a full-bridge configuration; steering diodes $D1, 2$; dc-link diode $D3$, the tapped inductor (TI) $W1:W2$; the decoupling capacitor C_{dc} ; and the output filter L_o – C_o . The load is represented by the resistor R_L . The proposed SSBI is fed by a dc voltage source, V_g , considered to be derived of a single PV panel, and generates utility level ac output voltage V_o . Here, the input current is designated as i_g , the output current is i_o and its average component is I_o .



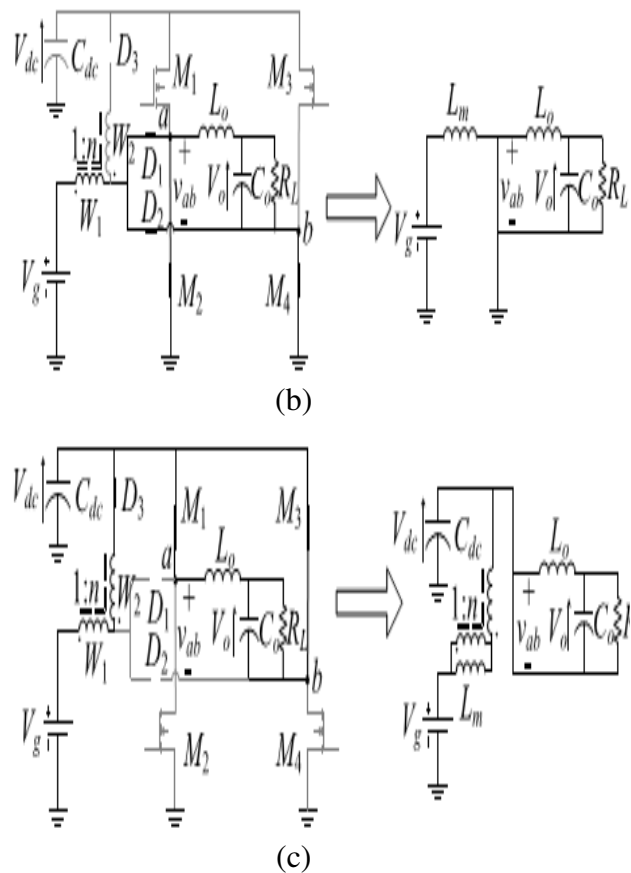


Fig.4. Topological states of the proposed SSBI and their equivalent circuits.

Compared to [16] and [17], the proposed SSBI topology has the advantages of a larger voltage step-up which can be achieved adjusting the TI turns ratio, and smaller decoupling capacitor, which is placed on high voltage dc bus. Principle of operation of the proposed SSBI is hinged on implementation of a specialized switching pattern of the H-bridge. In order to generate output voltage of positive polarity, three topological states are created during the switching cycle as shown in Fig. 4. Here, buck and boost sub topologies can be identified. The switching cycle starts with State A, shown in Fig. 4(a), which lasts for a duration of t_a . Here, the switches M_1 and M_4 are ON, whereas switches M_2 and M_3 are

OFF, D_2 conducts and D_1, D_3 are cut-off. During this state, the TI primary magnetizing inductance L_m is charged from the input voltage source V_g , while the dc voltage V_{dc} is applied to the input terminals of the output filter so the filter inductance L_o is charged feeding also the filter capacitor C_o and the load R_L . State B [see Fig. 4(b)] commences, as the switch M_1 is turned off and M_2 is turned on, whereas M_4 keeps conducting. State B lasts for a duration of t_b . Here, both D_1 and D_2 conduct while D_3 is cut-off. As a result, the TI magnetizing inductance L_m continues charging from the input voltage source V_g , whereas the input terminals of the output filter are shorted so the filter inductance L_o is discharged to the output capacitor C_o and the load R_L .

Table 1

Switching States of Semiconductor Devices

	Positive output voltage			Negative output voltage		
	State A	State B	State C	State A'	State B'	State C'
M_1	ON	OFF	ON	OFF	OFF	ON
M_2	OFF	ON	OFF	ON	ON	OFF
M_3	OFF	OFF	ON	ON	OFF	ON
M_4	ON	ON	OFF	OFF	ON	OFF
D_1	OFF	ON	OFF	ON	ON	OFF
D_2	ON	ON	OFF	OFF	ON	OFF
D_3	OFF	OFF	ON	OFF	OFF	ON

State C [see Fig. 4(c)] begins as the switches M_1, M_3 are turned on and M_2, M_4 are turned off. State C lasts for duration of t_c , and completes the switching cycle. Here, both D_1, D_2 are cut-off and D_3 conducts; the TI magnetizing inductance L_m is discharged via both windings and D_3 into the dc-link capacitor C_{dc} , while the input terminals of

the output filter are shorted and the filter inductance L_o feeds the output capacitor C_o and the load R_L . In order to generate output voltage of negative polarity, complementary switching states A, B, and C are created by the controller. Switching states of semiconductor devices throughout the switching cycle are summarized in Table 1. To create the desired switching states, proper switching signals for the H-bridge switches should be generated of the given buck and boost switching functions and the output polarity signal S_{bk} (D_{bk}), S_{bst} (D_{bst}), P , respectively. Here, the driving signals of the switches $M_1 \dots M_4$ are designated as $S_1 \dots S_4$, respectively. The required Boolean functions can be derived from Table 1

$$S_1 = \overline{\overline{P \cdot S_{bk} \cdot S_{bst}}}$$

$$S_2 = \overline{P \cdot S_{bk} \cdot S_{bst}}$$

$$S_3 = \overline{\overline{P \cdot S_{bk} \cdot S_{bst}}}$$

$$S_4 = \overline{P \cdot S_{bk} \cdot S_{bst}}$$

(2)

Key waveforms of the proposed SSBI throughout a line frequency cycle are illustrated in Fig. 5. Note that since the switching cycle of SSBI is comprised of three states, there are $3!$ possible permutations or state sequences. In other words, the order of appearance of the states is not unique and other possibilities exist, i. e. A–C–B, C–B–A, etc. An ideal SSBI can generate same dc–dc conversion ratio under any of these switching regimes. However, some state sequences may require switches

to be activated twice per switching cycle, which is undesirable in practice due to increased switching loss and/or extremely narrow on time. Proper synchronization of the gating signals also requires attention. The advantage of the implemented A–B–C state sequence is that each switch is turned on and off only once in a switching cycle, which helps reducing the switching losses.

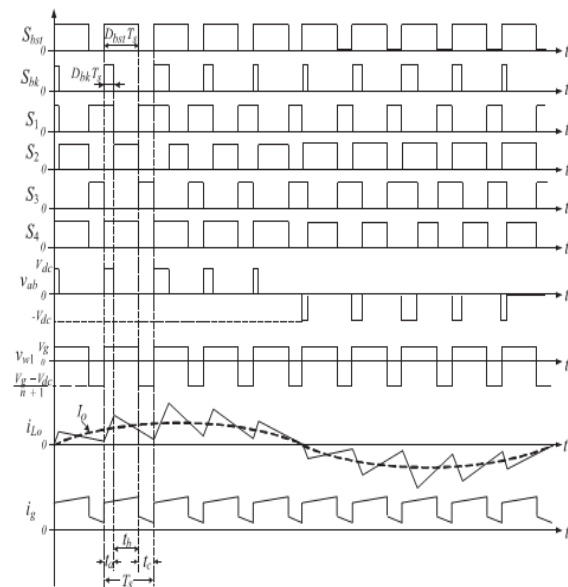


Fig.5. Key waveforms of the proposed SSBI

As a result of the proposed switching strategy, the voltage V_{ab} at the input terminals of the output filter is a three-level pulse train, which can be properly modulated to generate the desired output waveform of either polarity as shown in Fig.5.

III. SSBI Analysis and Simulation

To facilitate the analysis approach, the following assumptions are adopted: 1) all semiconductors are ideal with zero on resistance and voltage drop; 2) the decoupling capacitor and the output filter capacitor are sufficiently large and their voltage ripple is negligible; and 3)

continuous current operation of both the T_1 and the output filter inductor is assumed.

A. Derivation of Voltage Conversion Ratio Inspection of the converter's equivalent circuits in Fig.4 reveals that the power stage operates as a boost-derived TI dc-dc converter merged with a buck-derived full-bridge dc-ac inverter. Define t_a , t_b , and t_c the duration of states A, B, and C, respectively, and $T_s = t_a + t_b + t_c$ the switching period. Boost charging state, that is the time interval dedicated to charging the primary winding of the TI, takes place during states A and B [see Fig. 4(a) and (b)] whereas boost discharge takes place in state C. The total duration of the boost charging is therefore

$$t_{bst} = t_a + t_b \quad (3)$$

Accordingly, the resulting boost duty cycle D_{bst} is

$$D_{bst} = \frac{t_a + t_b}{T_s} \quad (4)$$

Hence, SSBI performs the dc-dc step-up conversion function identically to the TI boost converter. Adopting the approach of authors in [20] and the dc-dc voltage conversion ratio of SSBI is

$$M_{bst} = \frac{V_{dc}}{V_g} = \frac{1 + nD_{bst}}{1 - D_{bst}} \quad (5)$$

According to the aforementioned state description, the buck charging state, that is, the time interval dedicated to charging the output inductor, L_o , occurs in state A, where as buck discharge takes place in states B and C while the terminals of the

output filter are shorted. Thus, the duration of the buck charging is

$$t_{bk} = t_a \quad (6)$$

Accordingly, the resulting buck duty cycle D_{bk} is

$$D_{bk} = \frac{t_a}{T_s} \quad (7)$$

Clearly, under CCM condition of the output filter inductor, the voltage gain of the output section is identical to that of a buck converter and is given by

$$M_{bk} = \frac{V_o}{V_{dc}} = D_{bk} \quad (8)$$

Hence, the overall dc-ac voltage conversion ratio, M , of the proposed SSBI under CCM conditions can be derived combining (5) and (8)

$$M = \frac{V_o}{V_g} = M_{bk} M_{bst} = \frac{(1 + nD_{bst})D_{bk}}{1 - D_{bst}} \quad (9)$$

In stand-alone application, the buck duty ratio D_{bk} is modulated to attain a sinusoidal output voltage V_o of required amplitude and frequency, whereas the boost duty ratio D_{bst} is adjusted to satisfy load power demand and so stabilize the dc-link voltage V_{dc} . However, an important constrain arising from SSBI principle of operation is that the buck duty ratio D_{bk} should be smaller than the boost duty ratio D_{bst} at all times: $D_{bk} < D_{bst}$.

B. Voltage and Current Stress of Semiconductor Devices

Peak voltage and peak current of the semiconductor devices during a switching cycle are summarized in Table 2. The values

of the RMS currents of the semiconductor devices throughout the line cycle are given in Table 3. Here, the RMS value of buck duty cycle is defined as $D_{bk\text{rms}}=D_{bk}/\sqrt{2}$.

IV. Discontinuous Conduction Mode (DCM) Analysis

A. Derivation of the DCM Boost Conversion Ratio

Due to changing environmental conditions, the average PV output power can drop significantly. As a result, SSBI can enter DCM of the TI. This operation regime is investigated further. In the following analysis, it is assumed that SSBI is ideal (lossless components) and that the dc-link voltage V_{dc} is regulated in closed loop to a constant value. The ac–dc power balance suggests that the ac load is reflected to the dc link and can be modeled by an equivalent dc-link resistance R_{eq}

$$R_{eq} = \frac{V_{dc}^2}{P_o} \quad (10)$$

Where P_o is the average power level of the SSBI.

Since the principle of the dc–dc voltage step-up of the proposed SSBI is similar to that of the TI boost converter, Here, the TI is modeled as an autotransformer with a moderately low magnetizing inductance L_m . Typical waveforms of the input current $i_g(t)$ and diode current $i_D(t)$ in the DCM are illustrated, where V_{gs} is the driving signal of the switch M, i_{pk} is the peak current of the input current $i_g(t)$ and, I_D is the average diode current. The volt–second balance of the magnetizing inductance L_m suggests

$$\frac{V_{dc}}{V_g} = \frac{(n+1)D_{bst} + D_d}{D_d} \quad (11)$$

Where D_{bst} is the switch duty cycle, D_d is the diode duty cycle, and D_i is the idle duty cycle as illustrated. Charge balance of the output capacitor C_{dc} requires the average current of $i_{D(t)}$ equals the average load current, V_{dc}/R_{eq} ,

Table 2
Peak Voltage and Current Stresses per Switching Cycle

	Peak voltage	Peak current
M_1	V_{dc}	$I_{o\text{max}}$
M_2	V_{dc}	$I_{g\text{max}} + I_{o\text{max}}$
M_3	V_{dc}	$I_{o\text{max}}$
M_4	V_{dc}	$I_{g\text{max}} + I_{o\text{max}}$
D_1	V_{dc}	$I_{g\text{max}}$
D_2	V_{dc}	$I_{g\text{max}}$
D_3	$V_{dc} + nV_g$	$I_{g\text{max}}$

Table 3
Rms Current Stresses Per Line Cycle

$\frac{I_{d1\text{RMS}}}{I_{orms}}, \frac{I_{d3\text{RMS}}}{I_{orms}}$	$\frac{\sqrt{4\sqrt{2}D_{bst\text{rms}} - D_{bst}} + 1}{3\pi}$
$\frac{I_{d2\text{RMS}}}{I_{orms}}, \frac{I_{d4\text{RMS}}}{I_{orms}}$	$\sqrt{\frac{(n+1)^2 D_{bst\text{rms}}^2 (\pi D_{bst} + 2\sqrt{2}D_{bst\text{rms}}) + (n+1)D_{bst\text{rms}}^2 + 4\sqrt{2}D_{bst\text{rms}}}{4\pi(1-D_{bst})^2} + \frac{1}{1-D_{bst}} + \frac{4\sqrt{2}D_{bst\text{rms}}}{3\pi}}$
$\frac{I_{D1\text{RMS}}}{I_{orms}}, \frac{I_{D2\text{RMS}}}{I_{orms}}$	$\sqrt{\frac{(n+1)^2 D_{bst\text{rms}}^2 (\pi D_{bst} + 2\sqrt{2}D_{bst\text{rms}}) - 8\sqrt{2}D_{bst\text{rms}} + D_{bst}}{4\pi(1-D_{bst})^2} + \frac{1}{3\pi}}$
$\frac{I_{D3\text{RMS}}}{I_{orms}}$	$\frac{D_{bst\text{rms}}}{\sqrt{1-D_{bst}}}$

V. INDUCTION MOTOR

An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and

reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor. Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120f}{P}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

A. Control Strategy of Induction Motor

Power electronics interface such as three-phase SPWM inverter using constant closed loop Volts / Hertz control scheme is used to control the motor. According to the desired output speed, the amplitude and frequency of the reference (sinusoidal) signals will change. In order to maintain constant magnetic flux in the motor, the ratio of the voltage amplitude to voltage frequency will

be kept constant. Hence a closed loop Proportional Integral (PI) controller is implemented to regulate the motor speed to the desired set point. The closed loop speed control is characterized by the measurement of the actual motor speed, which is compared to the reference speed while the error signal is generated. The magnitude and polarity of the error signal correspond to the difference between the actual and required speed. The PI controller generates the corrected motor stator frequency to compensate for the error, based on the speed error.

5. MATLAB/SIMULINK RESULTS

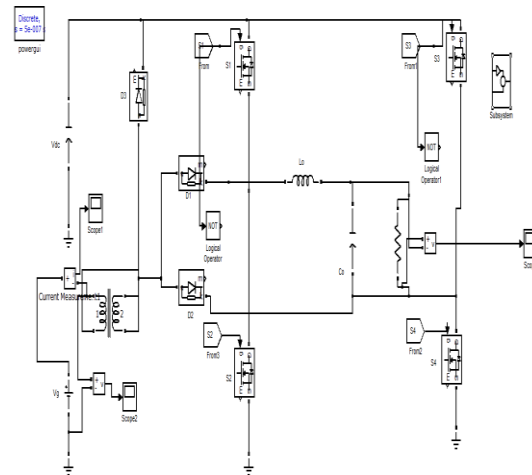


Fig.6. Matlab/simulink model of proposed Single Stage Boosting Inverter

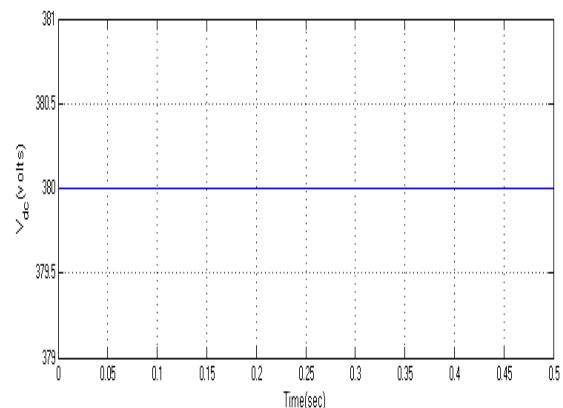


Fig.7. Input DC voltage

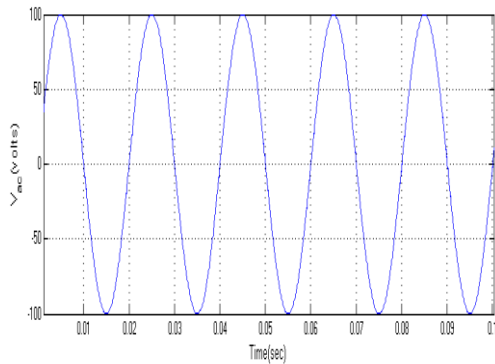


Fig.8.Output AC voltage

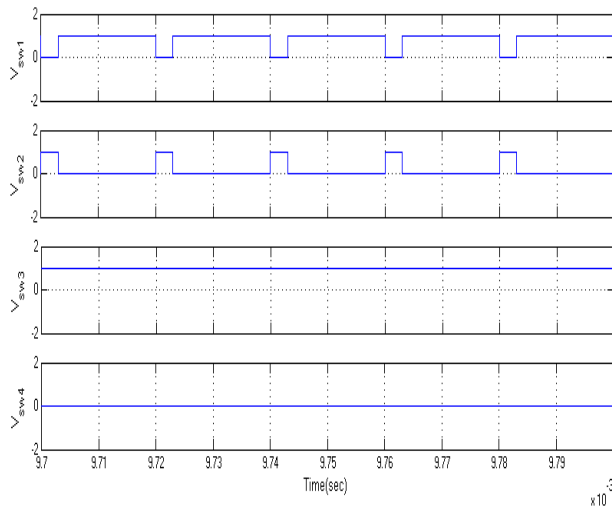


Fig.9.Switching Voltages

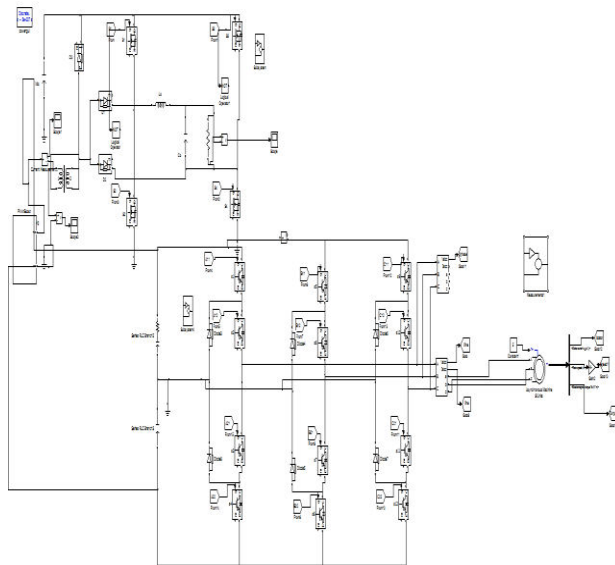


Fig.10.Matlab/simulink model of PV fed Single stage Boosting Inverter for Industrial Load

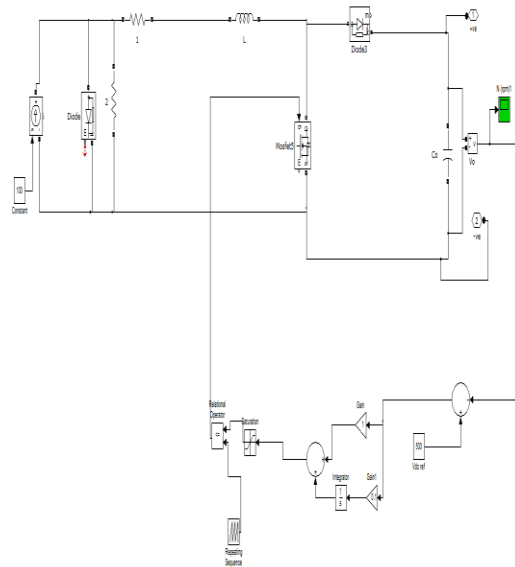


Fig.11.Matlab/simulink model of PV system

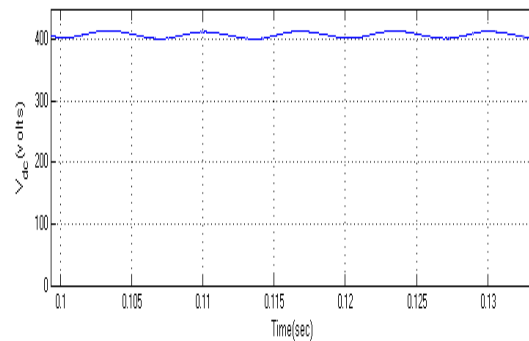


Fig.12.Input DC voltage

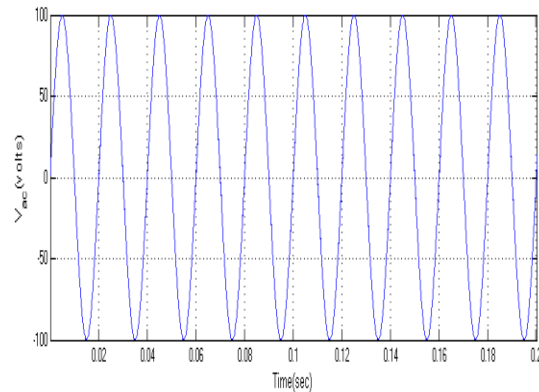


Fig.13.Output AC voltage

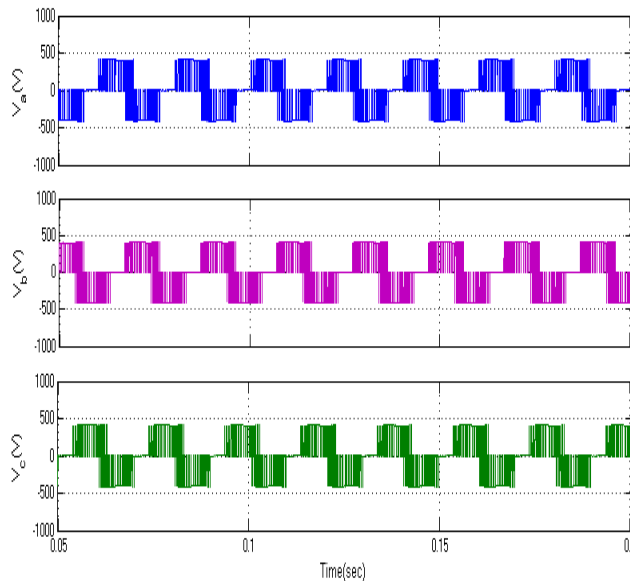


Fig.14. Inverter voltages

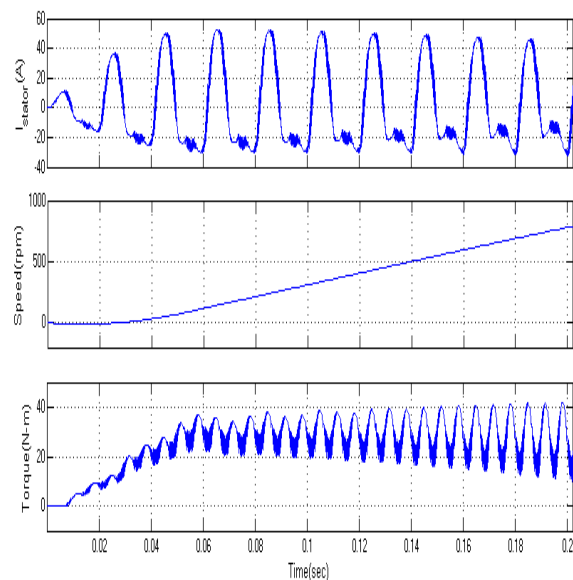


Fig.15. Waveforms of Stator Current, Speed and Torque of Induction motor

VI. Conclusion

A high-gain SSBI for alternative energy generation applications is presented in this paper. The proposed topology employs a TI to attain high-input voltage step-up and, consequently, allows operation from low dc input voltage. This paper presented

principles of operation, theoretical analysis of continuous and discontinuous modes including gain and voltage and current stresses. To facilitate this report, two stand-alone prototypes one for 48 V input and another for 35 V input were built. Acceptable efficiency was attained with low-voltage input source. The proposed SSBI topology has the advantage of high voltage step-up which can be further increased adjusting the TI turns ratio. The SSBI allows decoupled control functions. By adjusting the boost duty cycle D_{bst} , the SSBI can control the dc-link voltage, whereas the output waveform can be shaped by varying the buck duty cycle D_{bk} . The ac-dc power decoupling is attained on the high-voltage dc link and therefore requires a relatively low capacitance value. Pv cell fed proposed SSBI for Induction motor drive is simulated in Matlab/simulink software and the results are analysed.

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