International Journal for Innovative Engineering and Management Research
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ADPATIVE PERFORMANCE FOR SEVEN-LEVEL INVERTER USING PWM POD TECHNIQUE

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ABSTRACT:-

Multilevel inverters play a crucial part in the areas of high and medium voltage applications. The implementation of single phase seven level inverter with Dc link Switches based on POD technique is proposed in this paper. The multi level inverter is capable of generating seven level output with less component count is proposed. The PWM technique used in this work is Phase Opposition Disposition PWM(PODPWM). This technique uses single carrier wave and two sine waves for pulse generation. The inverter is connected to a R-load and performance are analyzed . By using the simulation results we can analyze the improvement of effiency.

INTRODUCTION

The Multilevel voltage source converter topologies are the best suited for medium and high

voltage applications in the industries. There are three main topologies of multilevel voltage source inverters: neutral point clamped (NPC), capacitor clamped (CC) and cascaded H-bridge (CHB). Multi level inverter are extensively used due to their increased power rating, reduced EMI, improving harmonic performance. The applications of multilevel inverter are reactive power compensation, variable speed drives etc. To cope up with the problems associated with the two-level inverter, multilevel inverters (MUs) are introduced. At low switching frequency multi level inverters are switched when compared to two level inverters, hence the switching losses are almost negligible. In the power industry the multi level converter topology has drawn tremendous interest since it can provide the high power required for high power applications. The inverter should meet the following requirements.

• To generate a pure sinusoidal output voltage.

• Inverter output current should have low total harmonic distortion (THD). In case of a two-level inverter, to satisfy the required THD the switching frequency should be high or the inductance of the output filter inductor need to be big enough , hence multilevel inverters (MUs) are introduced for grid connected inverter . The topological structure of Multi level inverters should be capable of withstanding high input voltage for high power applications. A new multi level inverter is proposed which is capable of reducing problems faced by usage of conventional multi level inverters. In power electronics have made the multilevel concept practical. One of the biggest advantages of using a MLI is that the transformer can be eliminated and this helps enhance efficiency and cost effectiveness. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. The advantages of proposed multi level inverter when compared with conventional Multi level inverter are :

1. The proposed multi-level inverter Number of devices is fewer than that of the conventional multi-level inverters. Therefore, the proposed system is more reliable and cost competitive than the conventional two-level and multilevel inverters.

2. To generate switching pulses to 10 switches used only one carrier signal is required in proposed Multi level inverter.One of the important issues about multi-level inverter is the voltage

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balance of the dc-link capacitor. The voltage of capacitor Cl and C2 should be equally balanced to VDC/2. A single sinusoidal reference is compared with each carrier signal to determine the output voltage for the inverter. In case of the N-Ievel NPC type multi-level inverter, N-l triangular carrier signals with the same frequency and amplitude are used so that they fully occupy contiguous bands over the range +VDC to -VDC. If the capacitor voltage is unbalanced, the output voltage becomes unsymmetrical and it results in a high harmonic content in the load current Three dispositions of the carrier signal to generate the PWM signal are considered as follows;

1) Phase disposition (PD); where all carriers are in phase.
2) Alternative phase opposition disposition (APOD); where each carrier is phase shifted by 180 degree from its adjacent carrier. 3) Phase opposition disposition (POD); where the carriers above zero voltage are 180 degree out of
phase with those below zero voltage

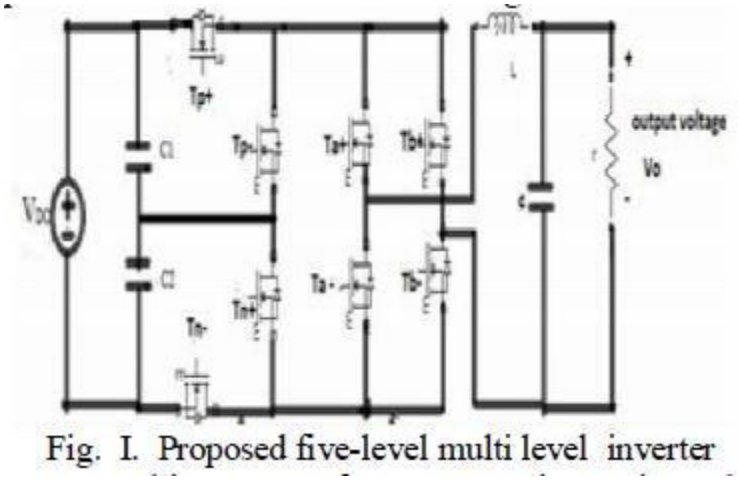

Fig. I. Proposed five-level multi level inverter

I. Proposed five-level multi level inverter This paper focuses on improving the efficiency of the multilevel inverter and quality of output voltage waveform. Harmonics Elimination was implemented to reduce the Total Harmonics Distortion (THD) value. To minimize the power demand and scarcity we have to improve the power extracting methods. There are many limitations in extracting power from renewable energy resources. To extract power from solar cells multilevel inverter is used. It synthesizes the desired ac output waveform

from several dc sources. In industrial applications multilevel inverter shows hope to reduce initial cost and complexity.

PROPOSED CASCADED MULTI LEVEL INVERTER

Based on cascaded H bridge multi level inverter fig.l illustrates the proposed multi level inverter . In the proposed multi level inverter two dc link capacitors Cl and C2 and 8 switches are used. Input supply to inverter is V dc and voltage across each capacitor is V dc/2. In order to eliminate the harmonics the output of the inverter is connected to LC filter. The switching sequence to generate 5 level output is shown in Fig.2.

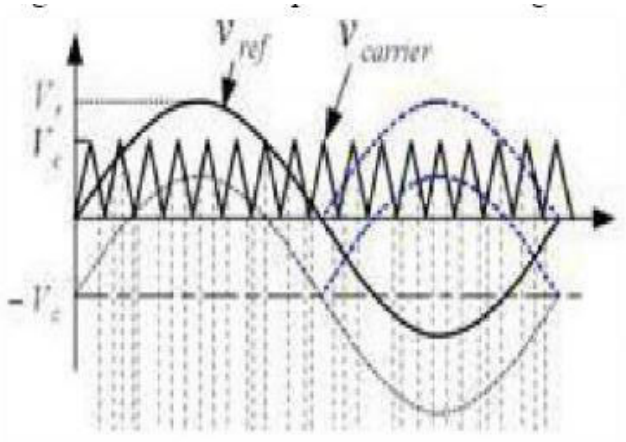

Fig. 2. Pulse generation using POD technique

Specifications of proposed inverter are as follows; Input DC voltage :100 volts

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Output Power : 250 watts
Filter inductance (L) : 300 IlH
Filter capacitance (C) : 150 IlF

TABLE I
SWITCHING CONDITIONS OF MULTI-LEVEL INVERTER

Output Voltage	Switching Conditions							
	T_p^+	T_p^-	T_n^+	T_n^-	T_a^+	T_b^+	T_a^-	T_b^-
V_{dc}	ON	OFF	OFF	ON	ON	ON	OFF	OFF
$V_{dc}/2$	OFF	ON	OFF	ON	ON	ON	OFF	OFF
$V_{dc}/2$	ON	OFF	ON	OFF	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF	OFF	OFF	ON	ON
$-V_{dc}/2$	OFF	ON	OFF	ON	OFF	OFF	ON	ON
$-V_{dc}/2$	ON	OFF	ON	OFF	OFF	OFF	ON	ON
$-V_{dc}$	ON	OFF	OFF	ON	OFF	OFF	ON	ON

A. POD Technique for Pulse Generation

POD stands for phase opposition and disposition technique. The proposed technique is based on POD technique. The proposed technique is used for pulse generation in multi level inverter shown. If sine wave is greater than carrier wave, witches Tp+ is on else Tp- is on. If sine wave 1 is positive then switches Ta+, Tb- are on and if sine wave is negative then switches Ta-,Tb+ is on. If sine wave 2 is greater than carrier wave ,switch Tn+ is on else switch Tn- is on.

SIMULATION ANALYSIS AND RESULTS

The technique used for pulse generation is POD technique .Simulation of proposed multi level inverter is carried out. 8 MOSFET are used as switches and output of multi level Inverter is connected to L,C filter to eliminate harmonics. L Figure 4 Dc supply of 100 volts is given using batteries and 2 dc link capacitors are used.

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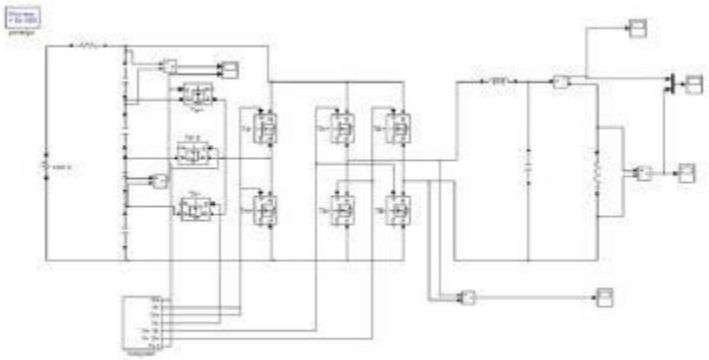

Fig 3 Block diagram of simulation

To measure the voltage across the capacitor Voltage measurement device is connected across each capacitor. Generally in order to turn on 8 switches 8 carrier signals are needed but using proposed technique single carrier wave is used to generate switching pulses to 8 switches. The output of Multilevel Inverter is connected to generate switching pulses to 8 switches. The output of Multilevel Inverter is connected to LC filter in order to eliminate harmonics and pure sine wave is obtained. Load Voltage are measured using voltage measurement device and Load current is measured using current measurement device. This type of MLI is mainly used for grid connected applications. Voltage is divided equally across two capacitors. Voltage across each capacitor is 50 volts. Voltage across each capacitor is measured using voltage measurement device

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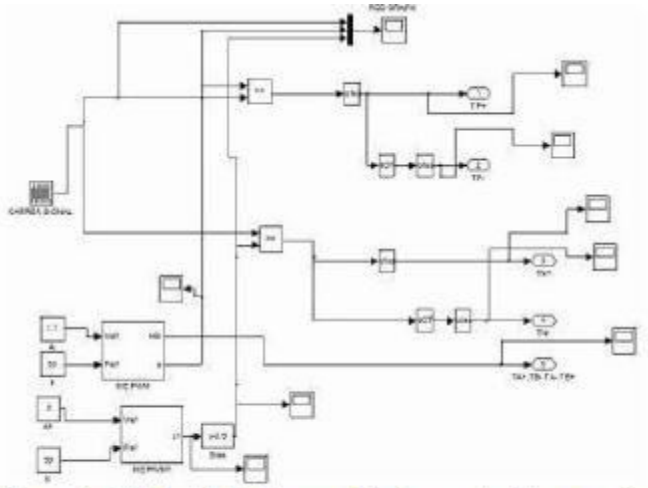

Fig. 4. SIMULINK model for switching pulse generation

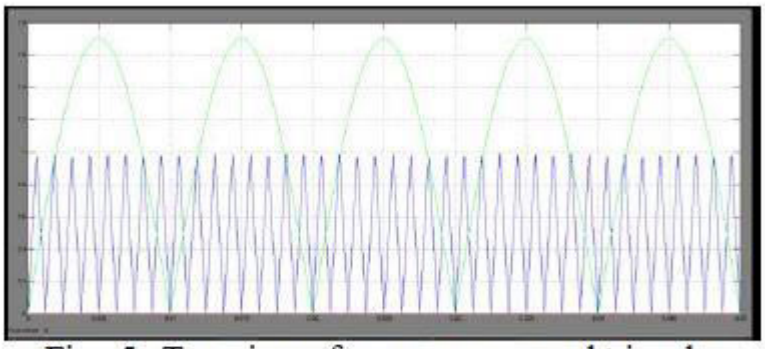

Fig. 5. Two sine reference waves and triangle carrier wave

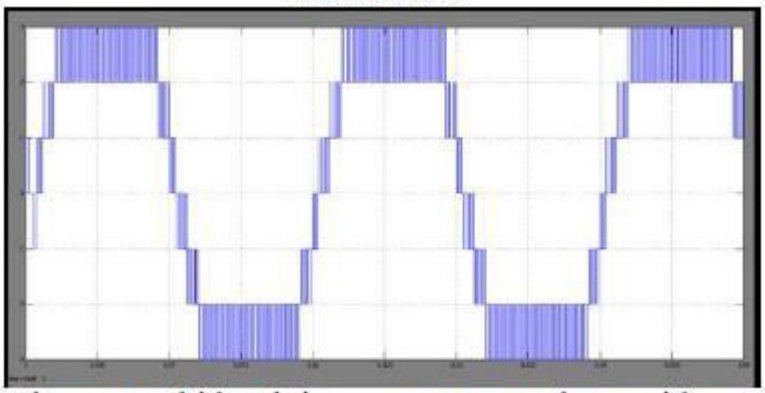

Fig. 6. Multi level inverter output voltage without LC filter

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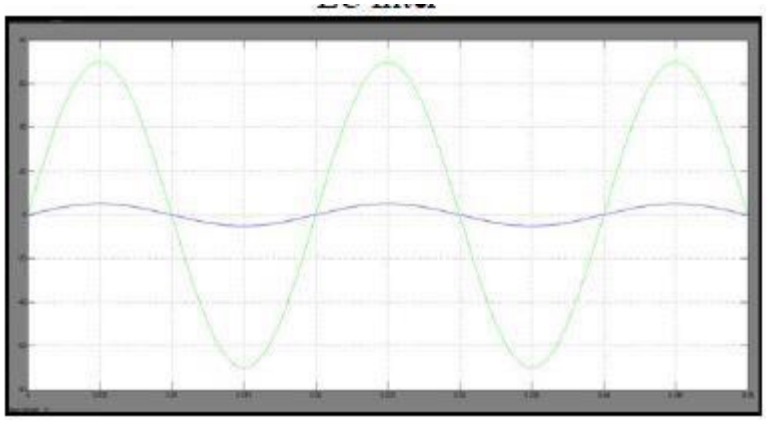

Fig. 7. Load voltage and load current (R-Load) with LC filter

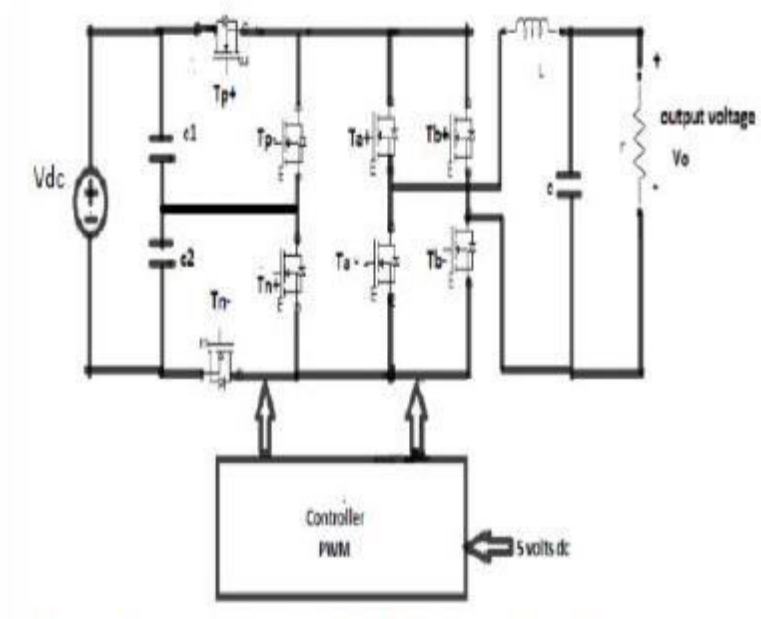

Fig. 8. Proposed single phase five-level inverter system

CONCLUSION

The control will be simulated using Proportional Integral Derivative(POD) controller.

Here we are increasing the levels from 5level to 7 level. A new Proposed topology can be easily extended to 7-level or higher level with minimized active device component count A new seven level inverter topology using POD technique is designed and the same is implemented. which is

capable of producing seven level output with less component count. No of dc supply sources used in proposed multi level inverter are less when compared to conventional Cascaded H bridge multi level inverter. At low switching frequency (50Hz) Switches are turned on . Hence switching losses are almost negligible.

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