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LOW POWER RECONFIGURABLE FFT PROCESSOR BASED ON RADIX-4

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ABSTRACT:

A novel, low-power, reconfigurable FFT processor is proposed. The architecture is served as a scalable IP core which is suitable for system-on-chip applications. The system can be configured as 16-point to 1024-point FFT. Flexibility is added to address the generation block, coefficient memory block and data memory block. Two switch blocks are implemented to route data and addresses to the right memory blocks. Compared with a conventional ASIC FFT processor, this FFT processor is characterized by having reconfigurability compared with an FFT processor which is mapped onto a general purpose reconfigurable architecture, it has lower-power and smaller area consumption.

Keywords: FFT, Complex logic block, mapping technologies.

1. INTRODUCTION

FFT is a very important technique in modern DSP and Telecommunication especially for application in OFDM system1 . The first FFT algorithm was proposed by2 the complexity to O (N log2 N) from O (N2) of DFT, N denote the FFT size. For hardware design different FFT Processor architecture have been proposed. The main classification is memory based3–4 and pipeline architecture styles5 . Memory based FFT processor design known as processor element approach. It consists of single processing element and memory unit, hardware cost is less but have long latency and low throughput. This drawback is overcome in pipeline architecture. The important pipeline types are SDF and MDC (Multipath Delay Commutator). In both the types multiplication complexity is same but the difference is memory size and Hardware utilization rate. SDF5–8 pipeline architecture require less memory size than MDC. Higher radix algorithm5 reduce computation complexity. The complex multiplier is realized by using digit slicing concept multiplier less architecture. In order to improve the power efficiency the buffer is designed with clock gating. Logic Encoding technique is used for counter design in control unit. The benefits of radix factorization for reduced hardware cost of custom FFTs have been largely unexplored. A ring-structured multiprocessor architecture was proposed in [9] to utilize mixed radix. A mixed-radix (radix 4 and radix 8) multipath delay feedback (MRMDF) architecture and indexed-scaling pipelined architecture were introduced in [10] and [11], respectively. A variable-length FFT processor that integrates two radix-2 stages and three radix-2 stages for FFT sizes 512, 1024 and 2048 was proposed in [12]. Prior work optimized various aspects of the FFT processors, but explored limited set of parameters. A systematic design methodology that integrates parallelism, radix factorization, and memory parameters for flexible FFTs has not been thoroughly investigated. We propose an FFT design methodology that jointly considers algorithm, architecture, and circuit parameters. We contribute with insights on how to use FFT radix structure for highly energy- and area-efficient implementations. Hundreds of architectures for 128- to 2048-point FFT exist by varying the degree of parallelism and radix factorization, as will be explained in this paper. Apart from parallelism and radix, delay buffers need to be efficiently implemented. Memory size partition and memory elements for delay lines of different lengths are evaluated. Our approach provides a cross-layered FFT design methodology to jointly optimize above parameters. For illustration, we will design for minimum power-area product (PAP). We will show an FFT processor that achieves the lowest energy per FFT operation, comparable area and much fewer processing cycles as compared to prior work. This paper is organized as follows. Section II gives a brief review of FFT operation, FFT radix structure and possible hardware architectures. Estimation of power and area and the use of FFT design techniques are discussed in Section III. As a proof of concept, Section IV presents a chip implementation of 3GPP-LTE compliant FFT (128 to 2048 points). Chip measurements indicate over a 2 better energy efficiency than prior work. Section V concludes the paper.

2. RELATED STUDY

The split-radix FFT algorithm mixes radix-2 and radix-4 factorizations, yielding an algorithm with fewer additions and multiplications than the radix-2 FFT. However, the split-radix algorithm has an irregular signal-flow structure and it can only be applied when is a multiple of 4. For the case where and are relatively prime, the DFT can be computed more efficiently using the prime-factor algorithm (PFA). The PFA decomposes and into smaller recursive sections without using the twiddle factors. The computation of the PFA has fewer multiplications but a complex re-indexing is required. For a power-of-prime size, the Winograd Fourier Transform Algorithm (WFTA) performs the decomposition efficiently using cyclic-convolution techniques. Since the cyclic-convolution operations often have coefficients of 1, 0, or , the WFTA requires fewer multiplications at the cost of more additions. The disadvantage of PFA and WFTA is that they only work for specific FFT sizes. Inspired by the split-radix algorithm, various radix factorizations have been proposed to implement efficient FFTs. For example, a split-radix FFT with minimal multiplicative complexity is proposed. High-speed low-power hardware implementations are presented. As mentioned before, prior work utilized radix factorization with limited success. The hardware complexity is minimized by only reducing the number of complex (full) multiplications for various radix FFTs. Also, the use of high-radix is commonly believed to be more area-efficient than low-radix algorithms due to the use of fewer complex multiplications. Signal Processing is the art and science of modifying acquired time-series data for the purposes of analysis or enhancement. Examples include spectral analysis (using the Fast Fourier or other transforms) and enhancing acquired data using digital filtering. SP(Signal Processing software’s is ideally suited for signal processing because of its strong support for lengthy time-series data, and because its many built-in signal processing commands can easily be used through simple dialogs. In addition, Igor´s language makes it straightforward to implement any kind of custom signal processing algorithm, greatly aided by the power of Igor´s Fourier (and other) transforms.

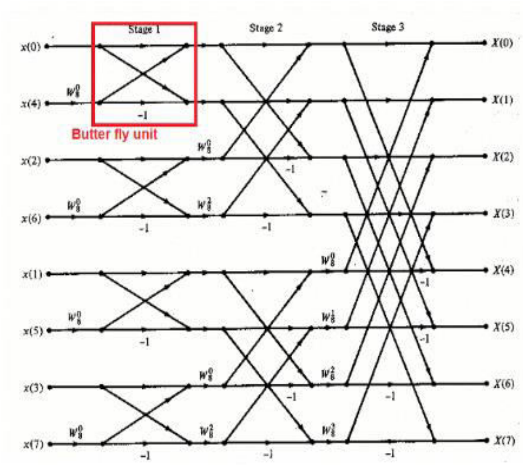

Fig.2.1. Model diagram

3. AN OVERVIEW OF PROPOSED SYSTEM

The FFT is a complicated algorithm, and its details are usually left to those that specialize in such things. This section describes the general operation of the FFT, but skirts a key issue: the use of complex numbers. If you have a background in complex mathematics, you can read between the lines to understand the true nature of the algorithm. Don&#39;t worry if the details elude you; few scientists and engineers that use the FFT could write the program from scratch. In complex notation, the time and frequency domains each contain one signal made up of N complex points. Each of these complex points is composed of two numbers, the real part and the imaginary part. For example, when we talk about complex sample X[42], it refers to the combination of ReX[42] and ImX[42]. In other words, each complex variable holds two numbers. When two complex variables are multiplied, the four individual components must be combined to form the two components of the product. The following discussion on the FFT uses this jargon of complex notation. That is, the singular terms: signal, point, sample, and value, refer to the combination of the real part and the imaginary part.

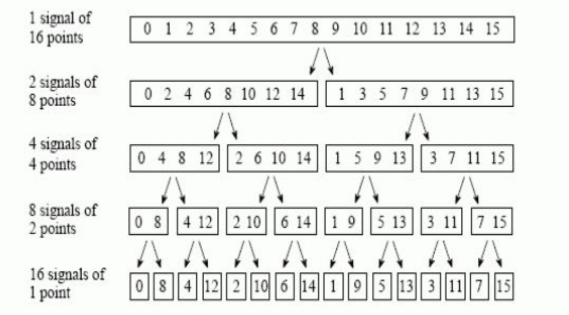

Fig.3.1. FFT decomposition.

The next step in the FFT algorithm is to find the frequency spectra of the 1 point time domain signals. Nothing could be easier; the frequency spectrum of a 1 point signal is equal to itself. This means that nothing is required to do this step. Although there is no work involved, don&#39;t forget that each of the 1 point signals is now a frequency spectrum, and not a time domain signal. The last step in the FFT is to combine the N frequency spectra in the exact reverse order that the time domain decomposition took place. This is where the algorithm gets messy. Unfortunately, the bit reversal shortcut is not applicable, and we must go back one stage at a time. In the first stage, 16 frequency spectra (1 point each) are synthesized into 8 frequency spectra (2 points each). In the second stage, the 8 frequency spectra (2 points each) are synthesized into 4 frequency spectra (4 points each), and so on. The last stage results in the output of the FFT, a 16 point frequency spectrum. Figure shows how two frequency spectra, each composed of 4 points, are combined into a single frequency spectrum of 8 points. This synthesis must undo the interlaced decomposition done in the time domain. In other words, the frequency domain operation must correspond to the time domain procedure of combining two 4 point signals by interlacing. Consider two time domain signals, abcd and efgh. An 8 point time domain signal can be formed by two steps: dilute each 4 point signal with zeros to make it an.

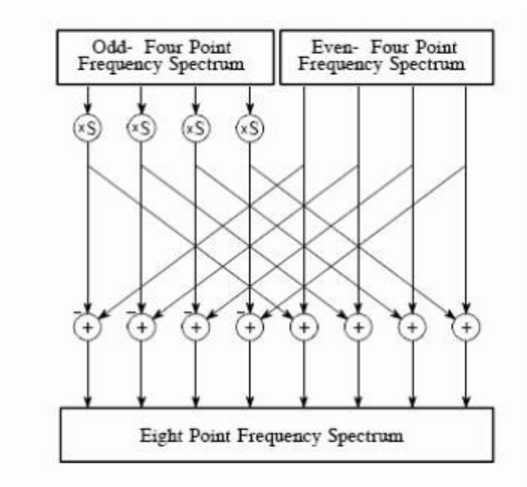
Odd- Four Point Frequency Spectrum
Even- Four Point Frequency Spectrum
xS
xS
xS
xS
+
+
+
+
+
+
+
+
Eight Point Frequency Spectrum

Fig.3.2. 8 points signal, and then add the signals together.

Proposed architecture is reconfigurable 128-2048 point FFT architecture as shown in fig. The method called architecture parallelism is used to achieve this. In architecture parallelism an N point FFT is divided into M and L point FFT (N=M*L). For P way parallel architecture, first stage comprises of P M- point FFTs and second stage with P L-point FFTs. When P=L, the single input SDF FFTs can be combined into a single Linput parallel FFT. The first stage pipelined 256 point FFT is reconfigurable to support 16-256 points. The second stage parallel FFT support 8 or 6 points. The overall FFT meets the 3GPP-LTE standard specification (128, 256, 512, 1024, 1536, 2048 points).

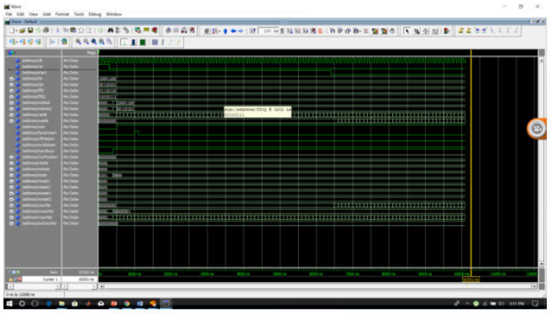

Fig.3.5. Simulation Results

4. CONCLUSION

Transpose-form structures are inherently pipelined and supports MCM which results significant saving in computation and increase in higher sampling rate. However, transposeform configuration does not directly support the block processing. In this paper, we have explored the possibility of realization of block FIR filter in transpose-from configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. We have made computational analysis of transpose-form configuration of FIR filter and derived a flow-graph for transpose-from block FIR filter with optimized register complexity. A generalized block formulation is also presented for transpose-from block FIR filter. Based on that we have derived transpose-form block filter for reconfigurable applications. We have presented the scheme to identify the MCM blocks explored the horizontal and vertical sub-expression elimination for the implementation of the proposed block FIR structure for fixed coefficients to reduce the computational complexity. A low-complexity design method using MCM scheme is also presented for the block implementation of fixed FIR filters. Performance comparison 10 shows that the proposed structure involve significantly less ADP and less EPS than the existing block direct-form structure for medium or large filter lengths while for the short-length filters, the existing block direct-form FIR structure has less ADP and less EPS than the proposed structure. ASIC synthesis result shows that the proposed structure for block-size 4 and filter-length 64 involve 42% less ADP and 40% less EPS than the best available FIR structure for reconfigurable applications. For the same filter length and block size, the proposed structure involves 13% less ADP and 12.8% less EPS than that of the existing direct-from block FIR structure. Based on these findings, selection of direct-form and transpose-form configuration based on the filter lengths and block-length is suggested for obtaining area-delay and energy efficient structures for block FIR filters.

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