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# HIGHLY EFFICIENT ASYMMETRICAL PWM FULL-BRIDGE CONVERTER FOR RENEWABLE ENERGY SOURCES

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**ABSTRACT:** This Paper proposes a full-bridge topology and asymmetric control scheme to achieve the zero-voltage switching (ZVS) turn-on of the power switches of the primary side and to reduce the circulating current loss. Moreover, the resonant circuit composed of the leakage inductance of the transformer and the blocking capacitor provides the zero-current switching (ZCS) turn-off for the output diode without the help of any auxiliary circuits. In addition, voltage stresses of the power switches are clamped to the input voltage. Due to these characteristics, the proposed converter has the structure to minimize power losses. It is especially beneficial to the renewable energy conversion systems. It improves the Power quality of the system and reduces the Installation cost of PV Cells.

**Keywords: zero-voltage switching (ZVS), the zero-current switching (ZCS), PV Cells.**

## 1 INTRODUCTION

The investigation on realistic strength sources (power segment, photo voltaic cells) has been prolonged in view of exhaustion of commonplace sources inside the earth. those sources produce low voltage essentialness. The sources which rely on situation situations like photovoltaic mobile produce fluctuating low voltage imperativeness. For this a front cease converter is required between low voltage supply and excessive voltage load as showed up in Fig.1. usually the front quit converter control factor of confinement is about 250W. At present the the front cease converter manipulate limit must be extended in mild of development of cell development. by way of this cost in step with watt is reduced as some distance as viable is extended. Thusly, the prolonged power rating of the the front-quit converter is needed to alter to huge electricity rating of the driven cells and decrease the cost consistent with watt of the viable power source gadget. the ordinary topologies considered for developing force restriction inside the front-quit converters, forward/flyback converters that use a operating snap with voltage doubler, LLC converters, and level move complete framework (PSFB) converters A operating clasp comprehends the zero-voltage trading (ZVS) by making use of the spillage inductance, the charging inductance, and the parasitic capacitance. The zero-cutting-edge buying and selling (ZCS) given by means of forward/flyback converters that usage the dynamic prop with voltage doubler . Voltage pressure inside the forward/flyback converters is higher over the primary switches of the

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transformer than the statistics voltage. MOSFET with low on-block RDS (on) can not be used. alongside those traces, with variable repeat control, LLC deafening converter can be utilized in all applications with variable data and yield voltages, solicitation of high viability and energy thickness. due to extensive records transmission voltage benefit controllability is cultivated with the aid of extending the repeat excessive. The topology of regular LLC reverberating because the front-stop converter of the scaled down scale inverter . Iis slightly completed in mild of the fact that it's miles hard to hold up high efficiency over fluctuating data voltage with unique weight situations. inside the point of view on high viability within the medium electricity packages the PSFB converters are substantially used. The trading motion is essential and is laboured with touchy trading without additional elements.The degree circulate manipulate plan isn't always legitimate, underneath the fluctuating records voltage, the overall-partner converter with in mild of the truth that its manage plan has some certified shortcomings, for instance, a constrained ZVS extent of the loosen leg switches, commitment cycle worry, first-rate revolving round present day disaster, and voltage spikes over the yield diodes. Voltage spike is an intense issue within the applications that require high voltage [21]. to beat the issue of the tight ZVS stretch out below the fluctuating information voltage, the freewheeling time allotment is progressively required. by then, by using the splendid streaming contemporary the conduction loss of the essential aspect is extended. The disposition executioner trading mishaps of the loosen leg switches are furthermore prolonged. because of the lacking imperativeness this is secured inside the spillage inductor ZVS venture of the loosen leg switches cannot be guaranteed underneath the mild weight circumstance. Alongside these strains, to address the problems of ZVS motion, additional contraptions are usually blanketed. those gadgets which might be used to widen ZVS develop but, the conduction setbacks and commitment cycle worry is extended. because of the resonation between the spillage inductance and the yield capacitor the PSFB converter in [24] gives a huge ZVS quantity of the loosen leg switches. It diminishes the soaring cutting-edge at some stage in the freewheeling time allotment. Regardless, the limited full repeat can cause preposterous modern-day nerves. along those traces, the same old PSFB converter with the more fastening circuit is in like way now not practical for fluctuating statistics voltage. As referenced over, the customary PSFB converters cannot satisfy high viability in fluctuating records voltage in mild of the way that extra contraptions for ZVS movement realise the baffling circuit shape and the influence mishaps.

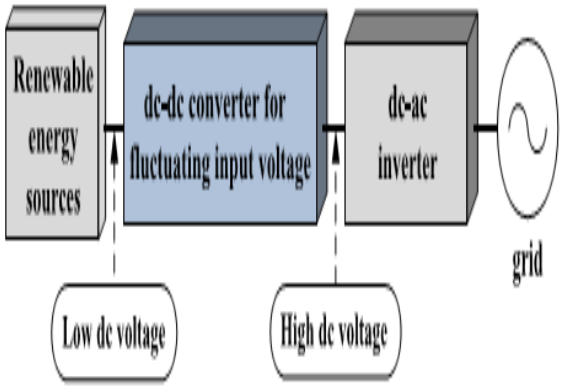


Fig.1. Renewable energy conversion system.

This undertaking proposes a complete-accomplice converter with unbalanced heartbeat width directed (APWM) manage

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this is fixed repeat system, with the aid of utilizing resonation of the fragments which achieves ZVS turn-on of the switches and ZCS flip-off of the yield diode. The voltage stresses over the strength switches (S1–S4) of the simple aspect are secured to the facts voltage and the voltage strain of the yield diode is in like manner faded with out a voltage spike. All round, APWM manipulate plan has the pressure with unbalance of the yield elements and the switch recovery difficulty of the helper side of the transformer. in any case, in the proposed APWM complete-interface converter, those problems may be abstained from through ZCS flip-off. The streaming present day catastrophe is moreover eliminated at the essential side of the transformer in light of the way that there's no freewheeling duration, which is specifically gainful for excessive capability underneath fluctuating records voltage than the customary front-give up converters. along those traces, the proposed APWM full-interface converter is logically appropriate for applications requiring excessive adequacy over fluctuating facts voltage.

## 2 Analysis OFAPWM full-BRIDGECONVERTER

### a) Circuit Configuration and Operation principle

A circuit arrangement of the incredibly effective APWM complete growth converter for low records voltage variety is showed up in Fig.three.2.the sport plan of the proposed converter is generally just like that of the normal complete-interface converter beside the dc blocking off capacitor and the discretionary aspect of the transformer. The fundamental aspect of the transformer consists of the primary winding turns Np, the four switches, and the dc blocking off capacitor Cb. The discretionary aspect has the assistant winding Ns, the yield diode Do, and the yield capacitor $C_o$.

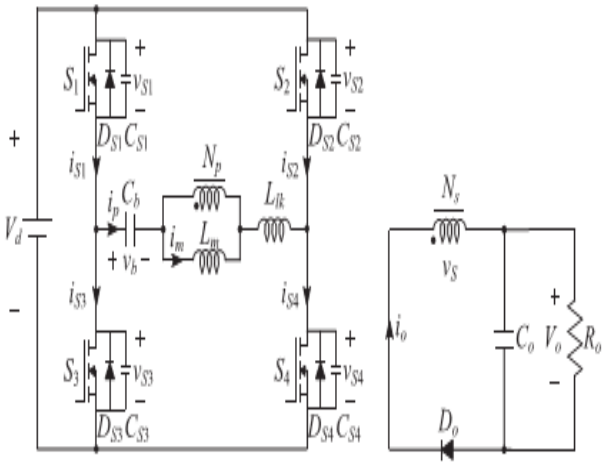


Fig.2.Circuit diagram of the proposed APWM full-bridge converter.

To look into the long-lasting country movement of the proposed APWM complete-interface converter, the going with suppositions are made.

1) The transformer is proven as an excellent transformer with the simple winding turns Np, the discretionary winding turns Ns, the charging inductance Lm, and the spillage inductance Llk

2) All switches S1–S4 are considered as impeccable modifications beside their frame diodes and yield capacitors (CS1=CS2=CS3=CS4= Coss).

three) The dc blocking capacitor Cb and the yield capacitor Co are enormous sufficient to push aside the voltage swell on it, so the voltages throughout over Cb and Co are regular.

whilst the switch S1 (S4) works with a commitment quantity D, structured upon the records voltage and weight situation, the transfer S2 (S3) works with a commitment volume 1−D. closer to the day's cease, the switches S1 (S4) and S2 (S3) are worked disproportionately. As such, the streaming contemporary lack of the essential facet can be abstained from in

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light of the fact that the proposed converter has no freewheeling length. Fig.three. 3 addresses the working modes, and Fig.three.4 addresses the speculative waveforms of the proposed converter beneath a continuing nation circumstance. The motion of the proposed converter can be segregated into six modes in the course of a trading duration Ts.

Mode 1[t0,t1]: At t0, the switches S2 andS3 are slaughtered. The simple modern ip discharges the yield capacitances CS1 and CS4 of the switchesS1 and S4 and costs the yield capacitancesCS2andCS3 of switches S2 and S3. The c program languageperiod of this mode is brief and inappropriate in light of the way that the yield capacitances Cossof the switches are near nothing. therefore, the fundamental current ip and the polarizing contemporary im are visible as predictable really worth.

Mode 2[t1,t2]: Att1, whilst the voltages vS1andvS4acrossthe switchesS1 and S4become 0, the terrible currentflows through their body diodesDS1andDS4before theswitchesS1 and S4are grew to become on. by way of then, ZVS movement is achieved with the turn-on of the switchesS1 and S4, and the resonation happens among the dc blocking capacitorCb and the fundamental inductor Lm+Llk of the transformer, yet resonation impact does not appear in mild of the way that the loud duration is any more drawn out than one buying and selling period Ts. for that reason, by using the complexity among the voltages of the statistics and the dc blocking capacitorCb, the heading of the basic currentipis changed and kept straightly as seeks after:

$$i_p(t) = i_p(t_1) + \frac{V_d - V_b}{L_m + L_{lk}}(t - t_1) \quad (1)$$

Where $V_d$ is the input voltage and $V_b$ is the average voltage across the dc blocking capacitor $C_b$.

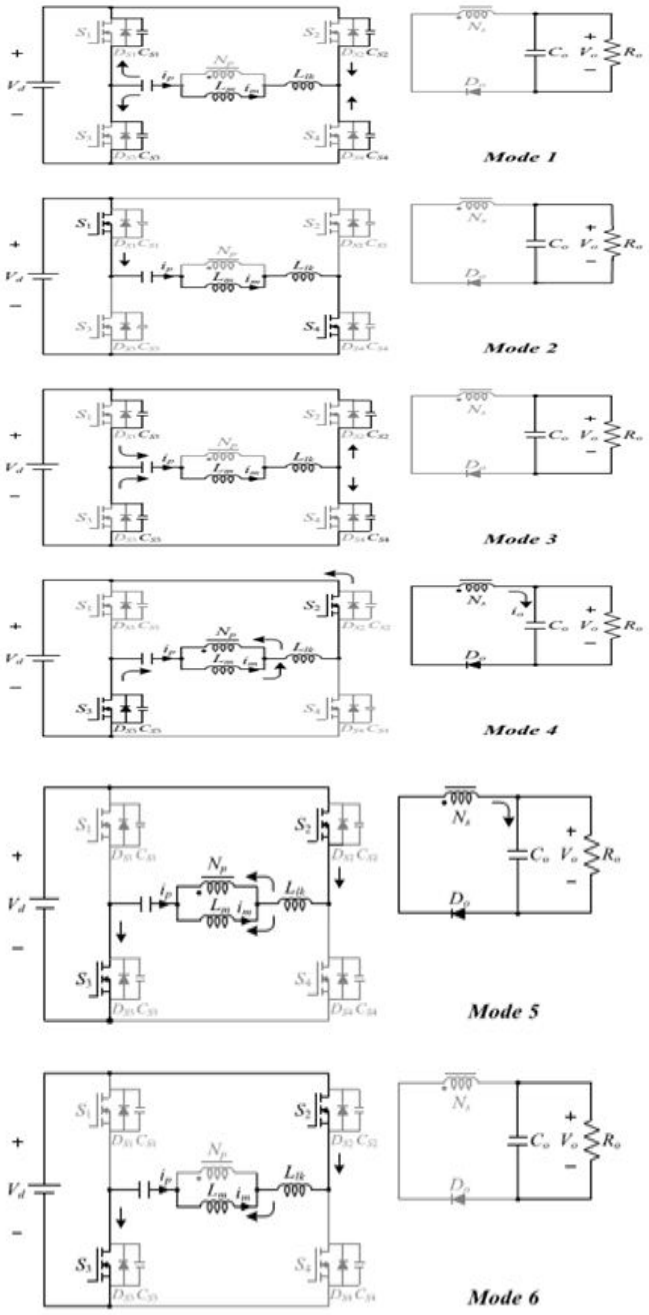


Fig.3. Operating modes of the proposed converter.

Mode three [t2, t3]: At t2, the switches S1andS4 are killed. The essential cutting-edge ip charges the yield capacitances CS1, CS4 of S1, S4 and releases the yield capacitancesCS2,CS3 ofS2,S4. Like Mode 1,the important currentip and the

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polarizing currentimare considered as steady really worth.

Mode four [t3, t4]: At t3, like Mode 2, ZVS turn-on of the switches S2 and S3 is carried out. The power positioned away inside the charging inductance is conveyed to the non-obligatory side of transformer, and the voltage over the polarizing inductance Lm is clasped with the aid of the reflected yield voltage as

$$L_m \frac{di_m(t)}{dt} = -\frac{V_o}{n} \quad (2)$$

Where $n=N_s/N_p$. Because the difference between the primary current $i_p$ and the magnetizing current $i_m$ is reflected in the output current $i_o$, the magnetizing current $i_m$ is decreased as

$$i_m(t) = i_p(t_3) - \frac{V_o}{nL_m}(t - t_3). \quad (3)$$

The reverberation happens among the dc blocking capacitor Cb and the spillage inductance Llk of the transformer. The voltage over the spillage inductance Llk of essential side is the distinction among Vd +Vb and the considered yield voltage Vo/n from the auxiliary viewpoint. along these lines, the country conditions can be composed as pursues:

$$L_{lk} \frac{di_p(t)}{dt} = -V_d - V_b + \frac{V_o}{n} \quad (4)$$

$$C_b \frac{dv_b(t)}{dt} = i_p(t) \quad (5)$$

Solving (4) and (5), the primary current $i_p$ is

$$i_p(t) = i_p(t_3)\cos\omega_r(t - t_3) + \frac{V_o/n - V_d - V_b}{Z_r}\sin\omega_r(t - t_3) \quad (6)$$

Where the resonant angular frequency $\omega_r$ and the impedance $Z_r$ of the resonant circuit are

$$Z_r = \sqrt{\frac{L_{lk}}{C_b}} \quad \omega_r = \frac{1}{\sqrt{L_{lk}C_b}}. \quad (7)$$

Mode five [t4, t5]: At t4, the critical modern ip ends up 0 and alters its course. additionally, the polarizing present day alters its direction for the duration of this intervening time. The yield contemporary io methodologies zero closer to the end of this mode with resounding qualities. on the factor whilst the yield contemporary io winds up zero, this mode closes.

Mode 6[t5,t6]: At t5, on the grounds that the reverberation propelled in Mode 4is finished, the yield modern io winds up zero. Be that as it could, the yield diode Do is saved up to on-state till the switchesS2andS3are killed. throughout this mode, the essential modern ipis equal to the charging contemporary im. for this reason, ZCS flip-off of the yield diode Do is achieved.

three.2.2 steady-state analysis

while the switchesS1andS4operate with an responsibility share D,the difference between the information voltage Vd and the regular voltage Vb of the dc blockading capacitor Cb is connected on the inductor of the transformer crucial aspect. while the switchesS2 and S3 paintings with an responsibility proportion 1−D, the contemplated yield voltage Vo/n is attached at the inductor of the transformer essential side and the yield diode Do is turned-on. for the reason that thunderous time of the whole gadget is any further than the useless-time span, conditions of the important contemporary ipfrom (1) and (2) are inferred as pursues:

$$i_p(t_3) = i_p(t_1) + \frac{V_d - V_b}{L_m + L_{lk}} DT_s \quad (8)$$

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$$i_p(t_1) = i_p(t_3) - \frac{V_o}{nL_m}(1-D)T_s. \quad (9)$$

From the reverberation of the essential side in Modes 4 and 5, since the spillage inductance Llk is a lot littler than the charging inductance Lm, the spillage inductance Llk is insignificant. In this manner, the accompanying condition can be gotten:

$$V_d + V_b \simeq \frac{V_o}{n} \quad (10)$$

From (8) to (10), the voltage gain between the input voltage $V_d$ and output voltage $V_o$ is expressed as follows:

$$\frac{V_o}{V_d} \simeq \frac{L_m}{L_m + L_{lk}} 2nD \simeq 2nD \quad (11)$$

Because the leakage inductance $L_{lk}$ is negligible, the average voltage $V_b$ of the dc blocking capacitor $C_b$ is expressed from (10) and (11) as shown in

$$V_b = V_d(2D-1) \quad (12)$$

Because of the charge equalization of the dc blocking capacitor Cb, the normal estimation of the essential current Ip is zero in the consistent state. Along these lines, the connection between the normal estimations of the charging current Im and normal yield current Io can be resolved as pursues:

$$I_m - I_p = I_m - \frac{1}{T_s}\int_0^{T_s} i_p(t)dt = nI_o. \quad (13)$$

From Fig.4, the average magnetizing current $I_m$ can also be obtained by

$$I_m = \frac{i_p(t_1) + i_p(t_3)}{2}. \quad (14)$$

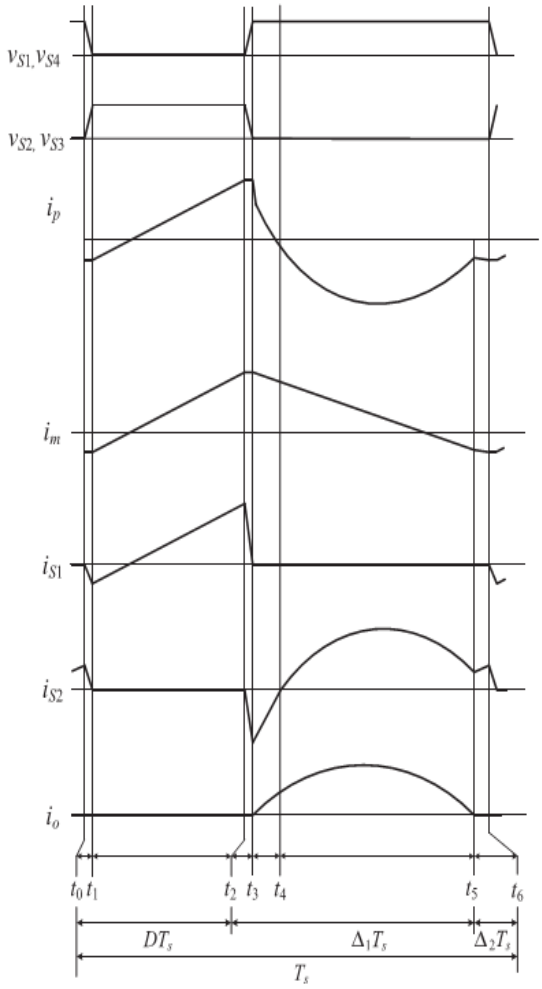


Fig.4.Theoretical waveforms of the proposed converter.

From (1), (13), and (14), the currents $i_p$ ($t_1$) and ip ($t_3$) are given by

$$i_p(t_1) = nI_o - \frac{(1-D)T_s}{nL_m}V_o \quad (15)$$

$$i_p(t_3) = nI_o + \frac{(1-D)T_s}{nL_m}V_o \quad (16)$$

Using (13)–(16), the resonant current (6) can be represented by

$$i_p(t) = \left(nI_o + \frac{(1-D)T_s}{nL_m}V_o\right)\cos\omega_r(t-t_3) - \frac{V_o}{nL_m\omega_r}\sin\omega_r(t-t_3). \quad (17)$$

## 3 SOFT-SWITCHING CONDITIONS

### a) ZVS Condition of the Power Switches

For ZVS turn-on of $S_1$ and $S_4$, the primary current $i_p$ ($t_1$) should be negative

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before $S_1$ and $S_4$ are turned on. Thus, from (15), ZVS condition can be expressed as follows:

$$nI_o - \frac{(1-D)T_s}{nL_m}V_o < 0. \quad (18)$$

Equation (18) is arranged by the min–max theorem as

$$\frac{n^2 L_m I_{o,\max}}{V_o} = \frac{n^2 L_m}{R_{o,\min}} < (1-D_{\max})T_s \quad (19)$$

Where $I_{o,max}$ is the maximum output current, $R_{o,min} = V_o/I_{o,max}$ is the minimum output resistance, and $D_{max}$is the maximum duty ratio of the switches $S_1$ and $S_4$under the minimum input voltage $V_{d,min}$. From (11), $D_{max}$ can be described as

$$D_{\max} \simeq \frac{V_o}{2nV_{d,\min}}. \quad (20)$$

in line with the assortments of the statistics voltage Vd and turn volume, the dedication volume of the switches S1 and S4. along those traces, from (three.19) and (three.20), the charging inductance Lm need to be deliberate to fulfill ZVS condition as seeks after:

$$L_m < \left(1 - \frac{V_o}{2nV_{d,\min}}\right) T_s \cdot \frac{R_{o,\min}}{n^2} \quad (21)$$

in which Ts is a trading length. according to the collection of the commitment quantity D, the crucial charging inductance regard Lm to satisfy the ZVS turn-on situation of the switches The ZVS flip-on circumstance of the switches S2and S3 can be spoken with a similar method for ZVS circumstance of the switches S1and S4. Thusly, ZVS assignment of S2 and S3 can be practiced when the essential present day ip (t3) is positive. From (three.16), ZVS province of S2 and S3 is imparted as seeks after:

$$nI_o + \frac{(1-D)T_s}{nL_m}V_o > 0. \quad (22)$$

The left component articulations of (22) are for each situation first class paying little heed to trouble assortments. as such, ZVS undertaking of the switches S2 and S3can reliably is satisfied.

some unique ZVS turn-on errand requires a sufficient pointless time among two change sets to genuinely discharge the voltage over the yield capacitance Coss of the switches. in view of the truth ip (t1) = im (t1) is appeared as predictable cost at some point or another of the dead time, the unimportant dead time Δtdead may be resolved as

$$\min\{|i_p(t_1)|, |i_p(t_3)|\} \geq 4C_{oss}\frac{dV_d}{dt} \quad (23)$$

From (15) and (16), the primary current $i_p$ ($t_3$) is always larger than the absolute value of the primary current $i_p$ ($t_1$). Therefore, (23) can be simplified as

$$\Delta t_{dead} \geq \frac{C_{oss}V_d}{|i_p(t_1)|/4}. \quad (24)$$

The primary current $i_p$ ($t_1$) should be negative for ZVS operation. Thus, (24) can be expressed as shown in

$$\Delta t_{dead} \geq \frac{4C_{oss}V_d}{\frac{(1-D)T_s}{nL_m}V_o - nI_o} \quad (25)$$

The minimum dead time $\Delta t_{dead}$ should be considered in the practical design of the magnetizing inductance because $\Delta t_{dead}$ is always smaller than $(1-D_{max})\,T_s$.

**b) ZCS condition of the Output Diode**

To accomplish the ZCS turn-off kingdom of the yield diode Do, the thunderous precise recurrence ωr have to be bigger than the simple rakish recurrence ωrc. for

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the reason that basic situation is ip (Ts) = im(Ts) at Δ2Ts = zero and D = Dmax, the primary particular recurrence ωrc may be portrayed thinking about the unimportant useless-time span of the electricity switches as pursues:

$$\left(\frac{n^2 L_m}{R_{o,\min}} + t_{S2,\min}\right)\cos\omega_{rc} t_{S2,\min} - \frac{1}{\omega_{rc}}\sin\omega_{rc} t_{S2,\min} - \frac{n^2 L_m}{R_{o,\min}} + t_{S2,\min} = 0 \quad (26)$$

Where$t_{S2,min}$is the insignificant flip-on length of the switches S2 and S The polarizing inductance Lmis typically intended for the charging currentim(t1)to be a little poor cost to decrease the conduction absence of the converter. Bythis presumption, (three.26) might be procured as pursues:

$$\tan\omega_{rc} t_{S2,\min} \simeq \omega_{rc}\frac{n^2 L_m}{R_{o,\min}} + \omega_{rc} t_{S2,\min} \quad (27)$$

From (21), (27) is expressed as shown in

$$\tan\omega_{rc} t_{S2,\min} < 2\omega_{rc} t_{S2,\min} \quad (28)$$

Thus, the critical angular frequency $\omega_{rc}$ can be calculated using a numerical method as shown in

$$\omega_{rc} \approx \frac{\pi + 1.462}{t_{S2,\min}} = \frac{\pi + 1.462}{(1 - D_{\max})T_s} \quad (29)$$

From (29), the dc blocking capacitance $C_b$ must satisfy the following relation:

$$C_b \le \frac{1}{\omega^2_{rc} L_{lk}} \quad (30)$$

According to the variation of the duty ratio $D$, the critical resonant capacitance $C_b$ to satisfy the ZCS turn-off condition of the output diode $D_o$.

## 4. MATLAB/SIMULATION RESULTS

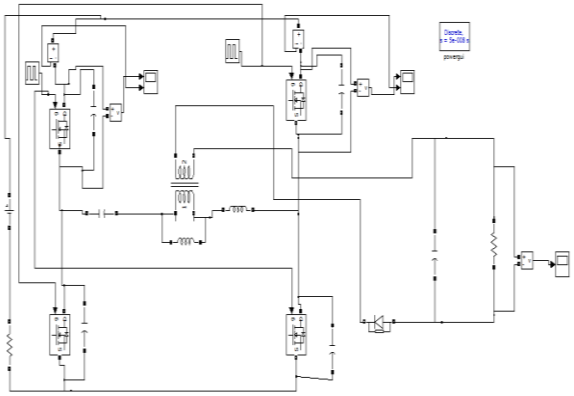
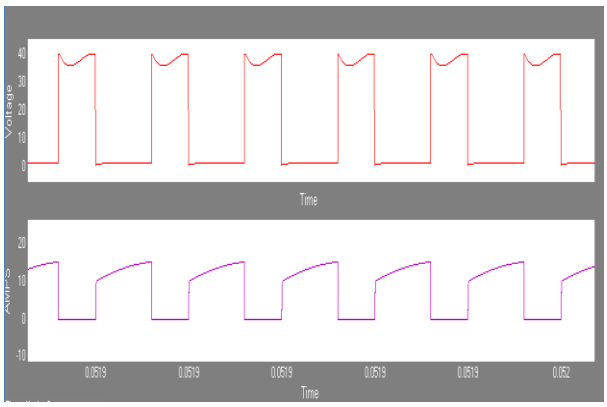
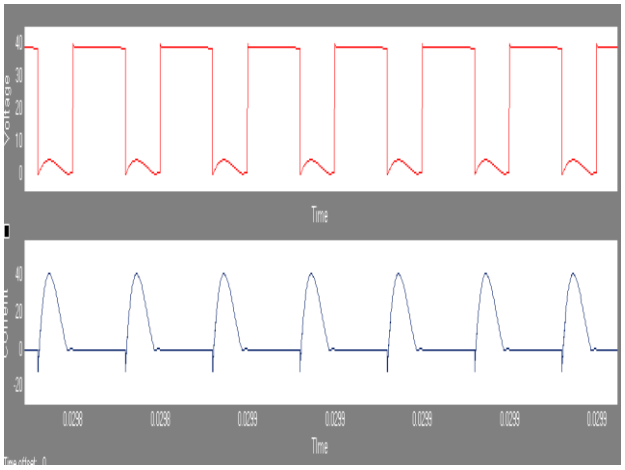


Fig.5. Matlab Circuit diagram of the proposed APWM full-bridge converter




a)




.b)

Fig 6 Simulation waveform of Voltage Experimental wave forms for ZVS turn on of the switches S1 and S2 at Vd=40v (a) vs1 and is1 (b)Vs2 and is2 at Vd=40V

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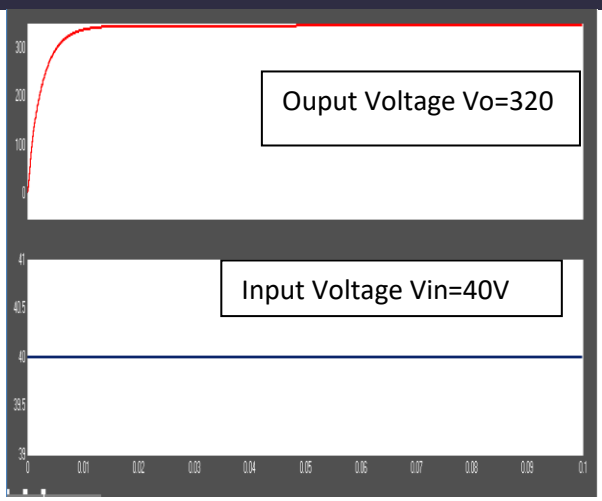



Fig 7 Simulation of Output voltage at Vd=40V

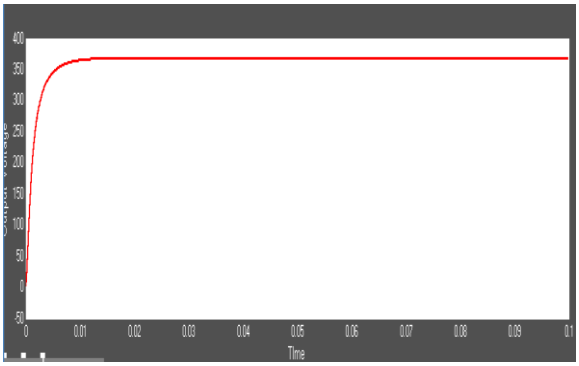
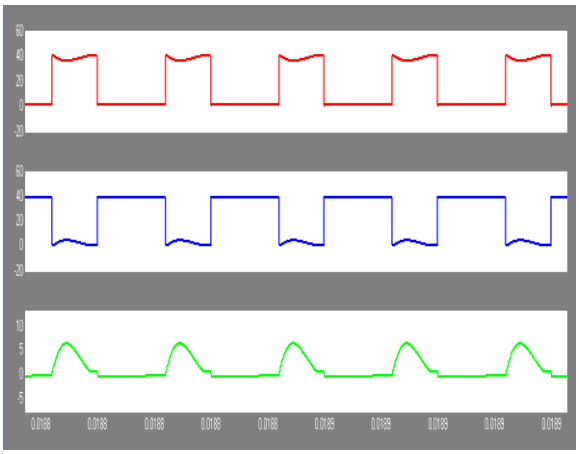
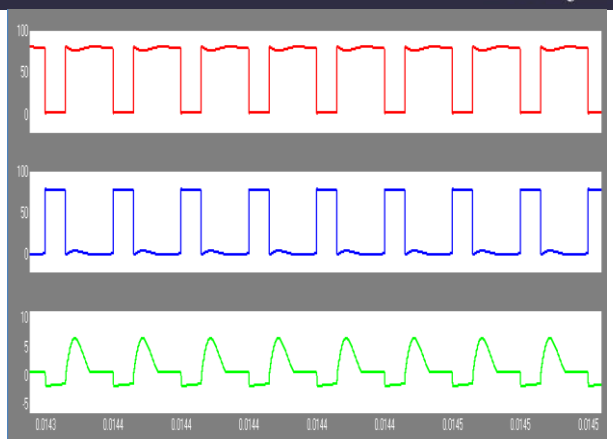


Fig 8 Simulation of Output voltage at Vd=40V



a)ZCS at VS2 and Iso



b)ZCS at VS2 and Iso at Vd=80V

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Fig 9 Experimental waveforms for ZCS turn off of the Diode (a) Vd=40v (b)Vd=80v

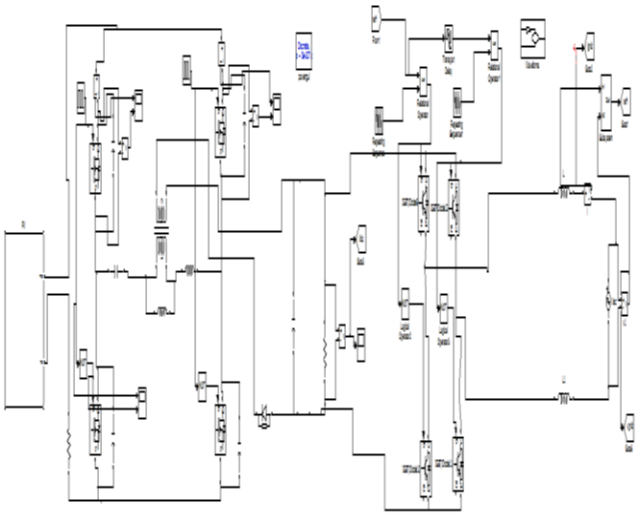
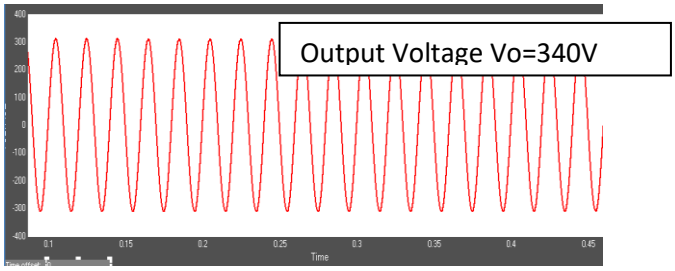


Fig 10 Matlab of the proposed APWM full-bridge converter PV Grid




a)Output waveform of PV Grid

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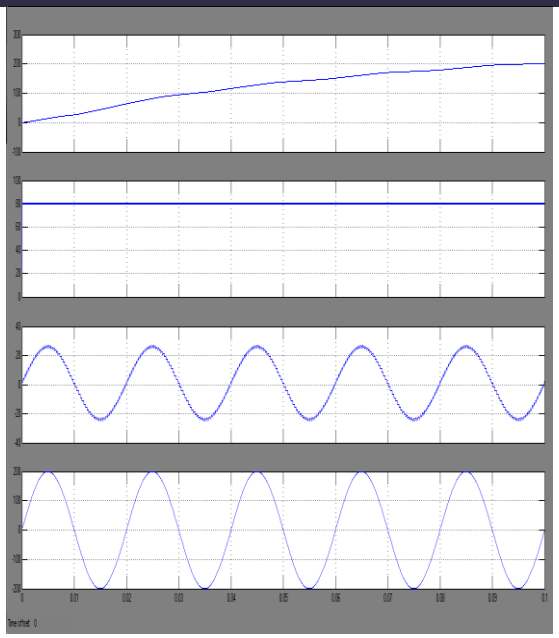


Fig 11 Simulation waveform of Dc voltage, phase voltage, grid current, grid voltage

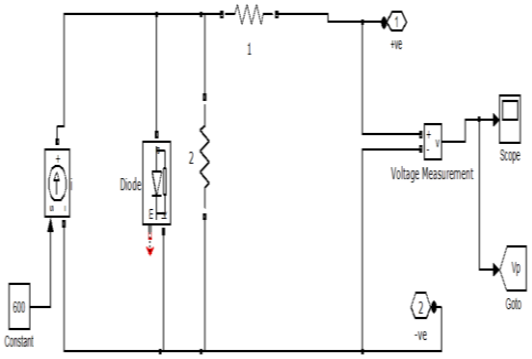



Fig 12 Matlab circuit for PV Grid

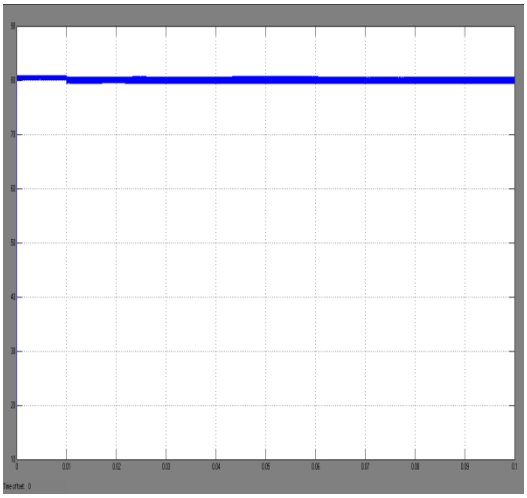


Fig 13 Simulation waveform for PV Voltage

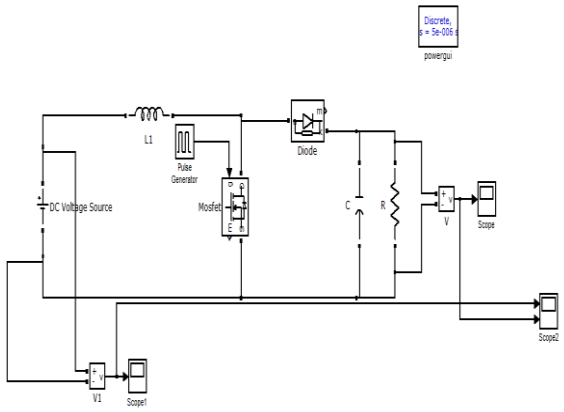



Fig 14 Simulink of Boost Converter

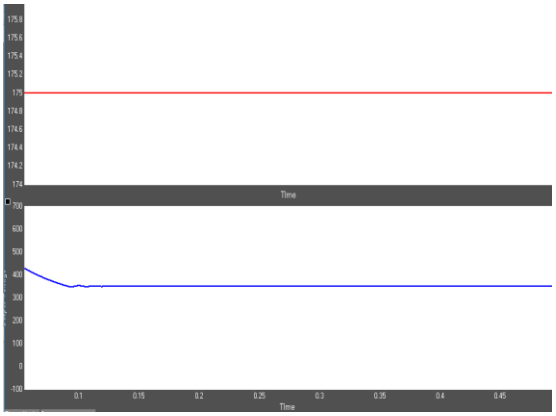
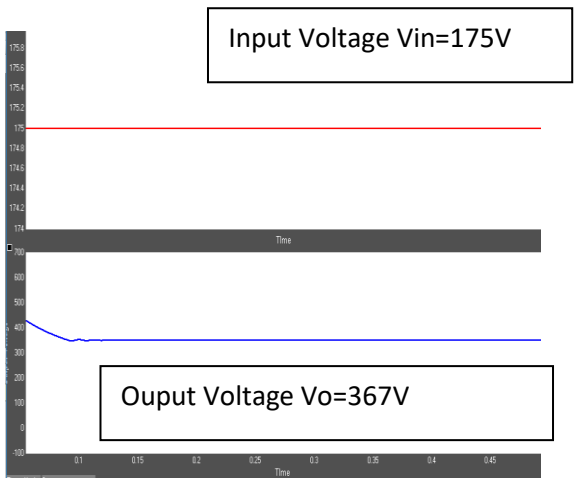


Fig 15 Simulation waveform for boost Converter

Comparison of output voltage between Boost Converter wave forms and APWM Full Bridge Converter Waveforms




a) Simulink of BOOST Converter

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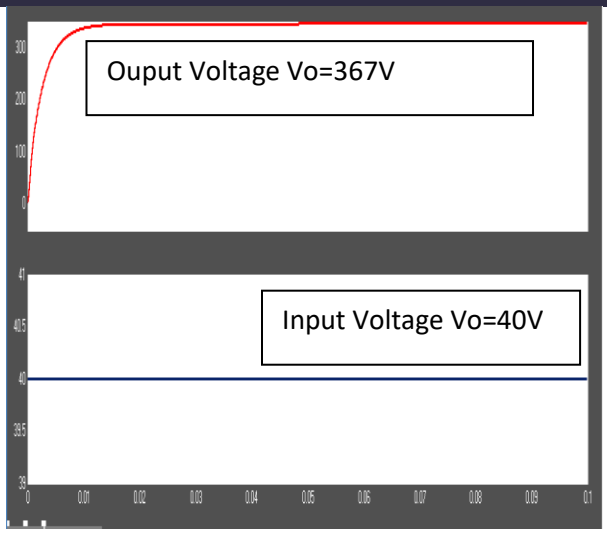


b)Simullink output waveform of APWM Full Bridge Converter

Fig 16 Simulation waveform for PV Voltage

## 5. CONCLUSION

On this errand, APWM full-interface converter for the realistic electricity source alternate systems that can shift between the information voltage of 40 and 80 V has been proposed. All energy switches paintings beneath ZVS and yield diode works underneath ZCS without more parts. Moreover, all energy switches are propped to the statistics voltage. as a consequence, the proposed converter has the shape to restrict control hardships. these significant focuses make the proposed converter appropriate for fluctuating records voltage on affordable electricity source alternate systems. APWM Converter associated with a Grid with an input PV Volage of 80V produces yield voltage extra than the standard improve converter. by way of the use of APWM full brdge Converter high the voltage growth is set five% when stood out from diverse converters.

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