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ENHANCED AREA EFFICIENT ARCHITECTURE FOR 128 BIT MODIFIED CSLA

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ABSTRACT

In the design of Integrated circuits, area occupancy plays a vital role because of increasing necessity of portable systems. Carry Select Adder (CSLA) is a fast adder used in data-processing processors for performing fast arithmetic functions. From the structure of the CSLA, the scope is to reduce the area of CSLA based on the efficient gate-level modification. In this paper 128 bit Regular Linear CSLA, Modified Linear CSLA, Regular Square - root CSLA (SQRT CSLA) and Modified SQRT CSLA architectures have been developed and compared. However, the Regular CSLA is still area consuming due to the dual Ripple-Carry Adder (RCA) structure. For reducing area, the CSLA can be implemented by using a single RCA and an add-one circuit instead of using dual RCA. Comparing the Regular Linear CSLA with Regular SQRT CSLA, the Regular SQRT CSLA has reduced area as well as comparing the Modified Linear CSLA with Modified SQRT CSLA; the Modified SQRT CSLA has reduced area. The results and analysis show that the Modified Linear CSLA and Modified SQRT CSLA provide better outcomes than the Regular Linear CSLA and Regular SQRT CSLA respectively. This project was aimed for implementing high performance optimized FPGA architecture. Modelsim 10.0c is used for simulating the CSLA and synthesized using Xilinx PlanAhead13.4. Then the implementation is done in Virtex5 FPGA Kit.

1.INTRODUCTION

The challenge of the verifying a large design is growing exponentially. There is a need to define new methods that makes functional verification easy. Several strategies in the recent years have been proposed to achieve good functional verification with less effort. Recent advancement towards this goal is methodologies. The methodology defines a skeleton over which one can add flesh and skin to their requirements to achieve functional verification. The report is organized as two major portions; first part is brief introduction and history of the functional verification of regular Carry select adder which tells about different advantages Carry select adder and RCA architecture and in this Regular Ckt one drawback is there overcome that complexity

problem we go for modified architecture of CSLA .Highly -increasing requirement for mobile and several electronic devices want the use of VLSI circuits which are highly power efficient. The most primitive arithmetic operation in processors is addition and the adder is the most highly used arithmetic component of the processor. Carry Select Adder (CSA) is one of the fastest adders and the structure of the CSA shows that there is a possibility for increasing its efficiency by reducing the power dissipation and area in the CSA. This research paper presents power and delay analysis of various adders and proposed a 32-bit CSA that is implemented using variable size of the combination of adders, thus the proposed carry select Adder (CSA) which has minimum Delay, and less power consumption hence improving the efficiency and speed of the Carry Select Adder. In recent years, the increasing demand for high-speed and low power arithmetic units in floating point co- processors, image processing units and DSP chips has resulted in the development of high-speed adders, as addition is an obligatory and mandatory function in these units. A compact and a high- performance adder play an important role in most of the hardware circuits. Adders are used in microprocessor system based application for arithmetic addition and for computation in large electronics circuit. Less efficient and low power adders would lead to an increase in the total power dissipation in the circuit and delay as well, so processing in these devices is required to be accomplished by making use of low-power; area-efficient circuits processing at a higher speed. On the basis of requirements such as area, delay and power Consumption, different types of adder, such as ripple Carry, the literature [1-7]. Ripple carry adders shows the most compact.design but slowest in speed, whereas carry look-ahead adder is the fastest one but it consumes more area. On the other hand, carry select adders act as a compromise between the two adders because it reduces the problem of carry propagation delay. However, the CSA generates partial sum and carry by using multiple pairs of Ripple Carry Adders (RCA) so it requires large area. CMOS circuits are most commonly used building blocks in digital integrated circuits. One of the major concerns in VLSI design is power consumption. Power consumption has become an important factor due to continuous decline in size of CMOS circuits and increase in chip density and frequency at which circuits are operating. This paper presents a comparative analysis of various adders and proposed design of a new 32 bit carry select adder by sharing common Boolean logic term which shows least power dissipation and PDP than other adders with less transistor count. This brief is structured as follows. Section II surveys various digital adders.

2. PROPOSED AREA EVALUATION METHODOLOGY OF MODIFIED 16-BIT LINEAR CSLA AND SQRT CSLA

The structure of the proposed 16-bit Linear and SQRTCSLA using BEC for RCA with carry in = 1 to optimize thearea is shown in

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Fig. 4.3. The 16-bit modified Linear CSLA has 4 groups of same size RCA and BEC. Each group contains one RCA, one BEC and MUX . . Inthe modified Linear CSLA, the group3 has one 4-bit RCA which has 3 FA and 1 HA for carry in =

O. Instead of another 4-bit RCA with carry in = 1 a 5-bit BEC is used which adds one tothe output from 4-bit RCA. The selection input of 10:5 mux is c7. If the c7=0, the mux select RCA output otherwise it select BEC output. The output of group3 are Sum [11 :8] and carryout, cll. Then the area count of group3 is determined as follows:

Gate count = 89
(FA + HA + MUX
+ BEC) FA =39
(3*13)
HA = 6 (1 * 6)
MUX = 20 (5 * 4)
NOT = 1,
AND = 3 (3 * 1)
XOR = 20 (4 * 5)
BEC (5-BIT) = NOT + AND + XOR = 24

Similarly the estimated area of the other groups in the modified Linear CSLA are evaluated and listed in

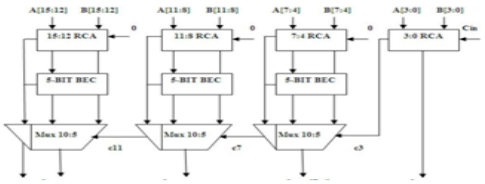

Figure. 1. Modified 16-bit Linear CSLA

GROUP	AREA ACCOUNT
Group 1	52
Group 2	89
Group 3	89
Group 4	89

Table 1. Area count of 16bit Linear CSLA

The structure of the 16-bit modified SQRT CSLA is shown in Fig. 5. It has 5 groups of different size RCA and BEC. Each group contains one RCA, one BEC and MUX. In the

GROUP	AREA ACCOUNT
Group 1	26
Group 2	43
Group 3	66
Group 4	89
Group 4	113

Modified SQRT CSLA, the group3 has one 3-bit RCA which\ has 1 HA and 2 HA for carry in =

O. Instead of another 2-bit RCA with carry in

Table 2. Area count for modified SQRT CSLA = 1 a 4-bit BEC is used which adds one to the output from 3-bit RCA. The selection input of 8:4 mux is c3. If the c3 = 0, the mux select RCA output otherwise it select BEC output. The output of group3 are Sum [6:4] and carryout, c6. Then the area count of group3 is determined as follows:

Gate count =
66 (FA + HA +
MUX + BEC)
FA =26 (2*13)
HA = 6 (1 * 6)
MUX =16 (4*4)
NOT = 1, AND
= 2 (2 * 1),
XOR = 15 (3 *
5) BEC (4-BIT)
= NOT + AND
+ XOR = 18

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Similarly the estimated area of the other groups in the modified SQRT CSLA are evaluated and listed in Table.

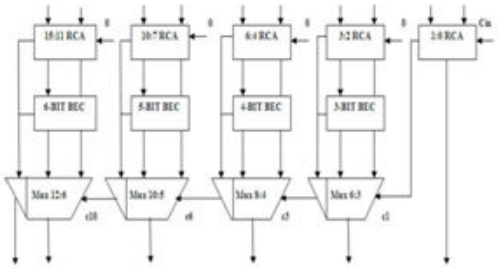

Figure 2. Modified 16-bit SQRT CSLA

3.SIMULATION RESULTS

In this system we use the BEC to reduce the RCA circuits Here based on the carry input the MUX will be select corresponding input In this design we give the MUX inputs are RCA output and BEC output Compare to regular design the area of the design is less conventional CSA, and conventional CRA. Analysis shows that it results in 48 to 52 percent Are has reduced and the power dissipation and 40% less PDP when implementation is done using modified SQRT BEC. The no of LUTS used in the circuit implementation is 437 out of available 1920 and the utilization factor is 22%, no of fully used LUT – FF pairs are 74 which is less usable factor, the no of bonded IOBS used 386 out of 66 and the utilization factor is 584% so this implementation considering the RTL is occupied less area and size is also reduced. That increased the system speed and efficiency and also less power requirement in the 128 bit carry select adder. The below result is from the RTL schematic view of Xilinx implementation.

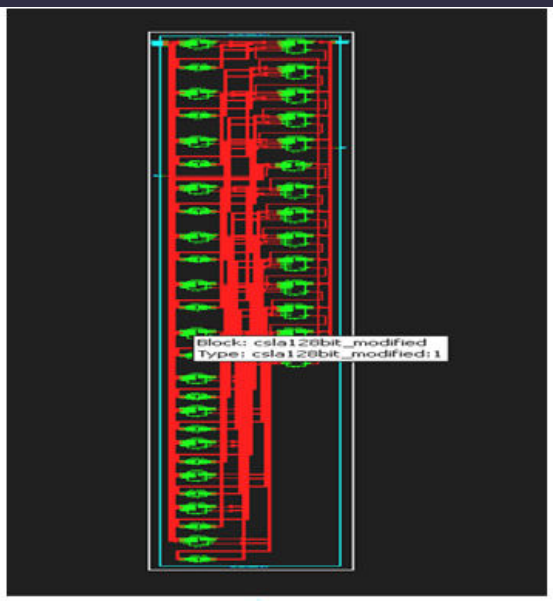

Figure4. RTL schematic view

SYNTHESIS RESULTS

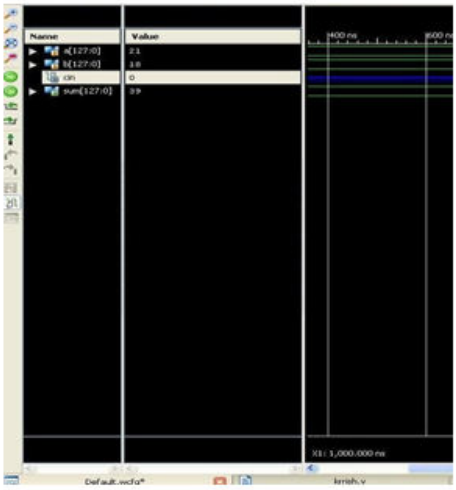

Figure 5.Basic RTL view and Simulation result

4.DESIGNSUMMARY:

In this system we use the BEC to reduce the RCA circuits Here based on the carry input the MUX will be select corresponding input In this design we give the MUX inputs are RCA output and BEC output Compare to

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Bit Size	Types	Area count of Linear CSLA	Area count of SQRT BEC CSLA
32-bit	Regular	871	868
	Modified	675	679
64-bit	Regular	1792	1736
	Modified	1387	1348
128- bit	Regular	3679	3472
	Modified	2811	2657

Table 7.1 Design Area comparison.

5. Advantages

- Low area (less complex city)
- More speed compare regular csla
- Less delay

6. Applications

- Arithmetic logic units
- High speed multiplications
- Advanced microprocessor design
- Digital signal proesses

7. CONCLUSION AND FUTURE SCOPE

In the design of Integrated circuits, area occupancy plays a vital role because of increasing necessity of portable systems. Carry Select Adder (CSLA) is a fast adder used in data processing processors for performing fast arithmetic functions. From the structure of the CSLA, the scope is to reduce the area of CSLA based on the efficient gate-level modification However; the Regular CSLA is still area-consuming due to the dual Ripple Carry Adder (RCA) structure. For reducing area, the CSLA can be implemented by using a single RCA and an add-one circuit instead of using dual RCA. Comparing the Regular Linear CSLA with Regular SQRT CSLA, the Regular SQRT CSLA has reduced area as well as comparing the Modified Linear CSLA with Modified SQRT CSLA with BEC; the Modified SQRT CSLA BEC has reduced area. The results and analysis show that the Modified Linear CSLA and Modified SQRT CSLA provide better outcomes than the Regular Linear CSLA and Regular SQRT CSLA respectively. This project was aimed for implementing high performance optimized FPGA architecture. We can even further implement by using 512bits also for more complex computations and for multiplications in several applications like

image processing and audio and video processing as well.

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