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DESIGN OF ADIABATIC MTJ-CMOS HYBRID CIRCUITS

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ABSTRACT:
Low-power designs are a necessity with the increasing demand of portable devices which are battery operated. In many of such devices the operational speed is not as important as battery life. Logic-in-memory structures using nano-devices and adiabatic designs are two methods to reduce the static and dynamic power consumption respectively. Magnetic tunnel junction (MTJ) is an emerging technology which has many advantages when used in logic-in-memory structures in conjunction with CMOS. In this paper, we introduce a novel adiabatic hybrid MTJ/CMOS structure which is used to design AND/NAND, XOR/XNOR and 1-bit full adder circuits. We simulate the designs using HSPICE with 32nm CMOS technology and compared it with a non-adiabatic hybrid MTJ/CMOS circuits. The proposed adiabatic MTJ/CMOS full adder design has more than 7 times lower power consumption compared to the previous MTJ/CMOS full adder.

Keywords: **Spintronics; Adiabatic; Low-Power; MTJ;**

1. INTRODUCTION

Most of these devices are battery operated and thus power consumption (battery-life) has become a critical design constraint. Therefore, researchers set out to discover new methods for designing low-power electronics. A method for designing low power electronics that reduces the leakage power consumption is to use non-conventional CMOS devices and using emerging nanotechnologies. Some new emerging technologies are very appropriate to be utilized in low power applications. Another method for reducing the dynamic power consumption is to recover the stored energy in the load capacitor instead of dissipating it as heat. This approach which operates based on energy recovery is known as adiabatic (reversible) circuit design. Main problem with CMOS devices scaling down is the increase in leakage power and reduction in gate control. Such that in nanoscale CMOS devices leakage power is an important component of the total energy consumption. Therefore, to continue chip density and performance scaling while maintaining low power, emerging devices and technologies such as quantum dot cellular automata (QCA), carbon nanotube field effect transistor (CNFET), single electron transistor (SET) and nano magnetic devices are attracting considerable attention as possible alternatives to CMOS devices. Among these new technologies spin based devices have attracted attentions as a potential successor for CMOS because of its outstanding characteristics such as near-zero standby power, non-volatility, high integration density, etc. The manipulation of the charge of electron has dominated the electronic

world for over six decades. Thanks to its solid physical foundation, incalculable charge-based electronic devices have been designed or truly applied for our life. One of the most well-known stories is about complementary metal-oxide-semiconductor (CMOS) technology, which plays a predominant role for integrated circuits nowadays. This relatively mature technology has been widely used in not only digital but also analog integrated circuits, for example, microprocessors, static random access memory (SRAM), image sensors and data converters. The evolution of CMOS technology is commonly described by the famous Moore's law that was observed by Gordon Moore in 1965. It predicts that the number of transistors in integrated circuits doubles approximately every two years, which is, however, often quoted as 18 months afterwards. This prediction based on observation has continued for a long time, in turn, it has become a motive force to drive the researchers to innovate and develop the technologies.

2. RELATED STUDY

In this background, novel technologies to replace the mainstream charge-based electronics are the hot topics for both academics and industries. Beyond the electrical charge, the spin freedom of electron attracts a broad attention and is considered to have a bright future. By being investigated for several decades, the spintronics was born from the discovery of Giant Magnetoresistance (GMR) effect and then rapidly developed. Figure 1.2 summarilizes the highlighted milestones for the development of the spintronics. The devices based on spintronics show the performance advantages in many aspects. The first one is low power. This is due to the non-volatility, which means that the information can be maintained without electrical power. With this feature, the system can be powered off in the idle state, which reduces greatly the standby power. Furthermore, spintronics can also allow reducing dynamic power that is normally caused by the large data traffic in the conventional Von-Neumann architecture. The possibility of spintronic devices to be 3D integrated above CMOS circuits at the back-end process can promise to significantly shorten the distance between memory and logic chip. Besides the power efficiency improvement, the potential advantages in terms of scalability and latency make the spintronic devices be used for various logic and memory applications. For example, spintronics has revolutionized ultra-high density Hard Disk Drives (HDDs) since the last 20 years. Magnetic tunnel junction (MTJ), one of the most important spintronic devices, is the basic element of magneto resistance random access memory (MRAM) which becomes a most promising candidate for the next generation of universal non-volatile memory. As a result of the tunnel magneto resistance (TMR) effect, the MTJ resistance depends on the relative magnetization orientations of two ferromagnetic layers in MTJ. Much of the academic and industrial research efforts are presently focused on developing efficient strategies for switching magnetization in MTJs. One promising method relies on using spin transfer torque (STT), which involves low threshold currents and well-understood mechanisms. Furthermore, only a bidirectional current is needed in this approached, which simplifies greatly the CMOS switching circuits and thereby allows for higher density than the other approaches. However, some unexpected effects have been discovered

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using this approach in small MTJs (e.g. lateral size of 40 nm), such as erroneous state switching with reading currents and short retention times. These problems are mainly related to the in-plane magnetic anisotropy, which cannot provide a sufficiently high energy barrier to ensure thermal stability. This issue limits greatly the potential for future miniaturization of MTJs. One compelling solution addressing this issue involves the perpendicular magnetic anisotropy (PMA) in certain materials (e.g. CoFeB/MgO), because it allows high energy barrier to be attained for small-size structure (< 40 nm) while maintaining the possibility of fast-speed operation, high TMR ratios and low threshold currents.

3. AN OVERVIEW OF PROPOSED SYSTEM

Beyond the STT switching mechanism, it has been discovered that a spin-polarized current can be generated by the SHE. Due to the spin-orbit coupling, the electrons with different spins deflect in different directions. However, this effect was usually too modest to limit its application. Recently, it was reported that a giant SHE in a high-resistivity from of tantalum (β-Ta) could generate a spin current strong enough to induce the switching of MTJ. Based on this prominent phenomenon, a three-terminal SHE device was proposed as shown in Figure 2.8(a). The electric current flowing horizontally induces a spin current to pass vertically through the inplane MTJ structure. As the spin polarization of spin current is governed by the direction of the electric current, the magnetization switching direction of MTJ depends thus on the sign of electric current. Although this three-terminal device would cause area efficiency degradation compared with the conventional MTJ, it exhibits various assets in many aspects. For example, by optimizing the thickness of Ta layer, the switching current can be decreased by nearly one order of magnitude compared with STT switching mechanism. The reduction of switching current and lower resistance of Ta layer can also lead to an advantageous switching energy. In addition, two terminal MTJ always suffers from the reliability issue due to different resistance requirements for writing and sensing operations: low resistance is expected for writing operation and high resistance is more suitable for sensing operation. Three-terminal device separates the writing and sensing operations structurally, solving properly the reliability challenges. Thanks to these assets, this SHE based MTJ structure is regarded to have great potential towards the future magnetic memory and non-volatile logic design.

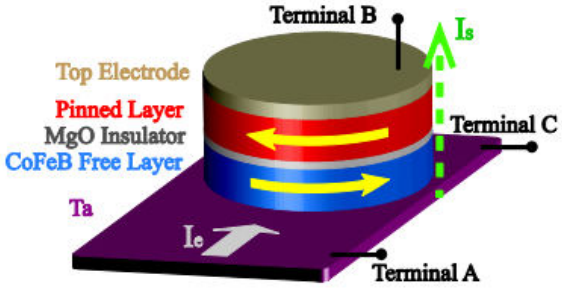

Fig.3.1. Three-terminal device based on the giant spin Hall effect.

Adiabatic logic is one of the low-power circuit design techniques at cost of slower speed of operation. The general schematic of an adiabatic technique is shown in Figure 2. In adiabatic circuits the load capacitance is charged by a constant current source unlike conventional CMOS where, the load capacitance is charged by a constant voltage source. Adiabatic logic reduces the overall power consumption of the circuit by employing a clocked AC power to charge the load capacitor and recovers energy from

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the charged capacitor in a slow manner to eliminate dynamic power dissipation.

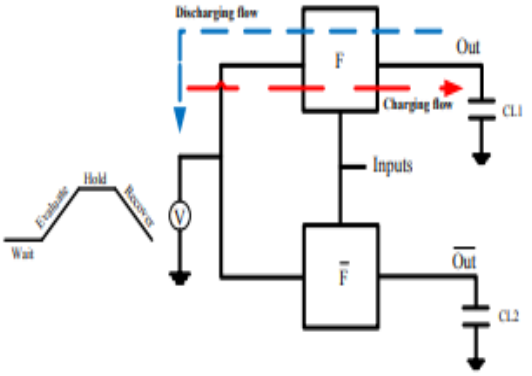

Fig.3.2. Circuit representing adiabatic charging/discharging.

In this section, we propose MTJ-based adiabatic circuits family. To the best of our knowledge this is the first attempt to design adiabatic magnetic circuits. MTJ-based circuits are generally composed of three parts as in Figure 3. The first part is a writing circuit, which is used for programming the memory elements. The second part constitutes of STT-MRAM cells and CMOS logic tree which as a logic control block. Finally, the last part is a sense amplifier (SA) that evaluates the output logic results.

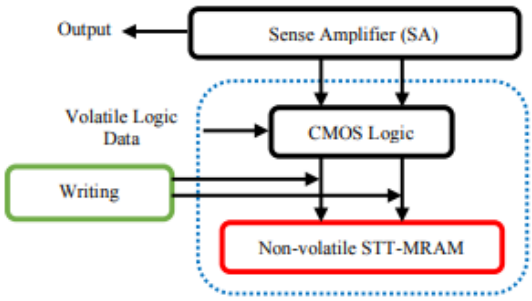

Fig.3.3. Structure of a MTJ based circuit.

The schematic design of the AND gate is shown in Figure. When the CLK is in the wait phase, both AND as well as NAND outputs are zero. Assume that the input pattern is "01" for "AB" then, T5 will be off and MTJ1 and MTJ2 will be in parallel and anti parallel states, respectively. With this input pattern, the left path is cut off and the AND output will be discharged to the ground and consequently the NAND output will charged to VDD in the evaluate phase. The outputs will remain the same in the hold phase whereas in the recovery phase, the NAND output will be discharged to the CLK supply power. Since T1 and T2 cannot discharge the outputs completely to zero, in the next wait phase the discharge signal will be VDD to share the outputs voltages and both outputs have the same amount of voltage.

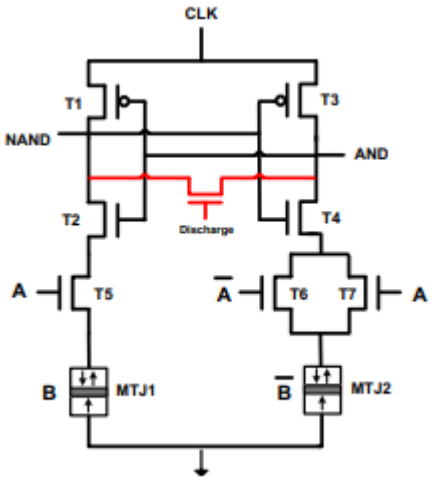

Fig.3.4. Proposed adiabatic hybrid MTJ/CMOS AND/NAND.

The proposed designs are simulated and compared with the MTJ/CMOS design in terms of power consumption. Simulations are conducted using the HSPICE circuit simulator with 32nm technology for CMOS transistors and the spice MTJ model presented for MTJ devices. Figure 8 shows the transient response of the proposed XOR design when the input B is VDD. It confirms the correct operation of our design. The comparison results of our proposed designs and the design are depicted in Figure 9. The graphs suggest that the proposed adiabatic hybrid MTJ/CMOS XOR, AND, and the full adder designs have almost 13, 6 and 7 times lower

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power consumption compared to the designs presented.

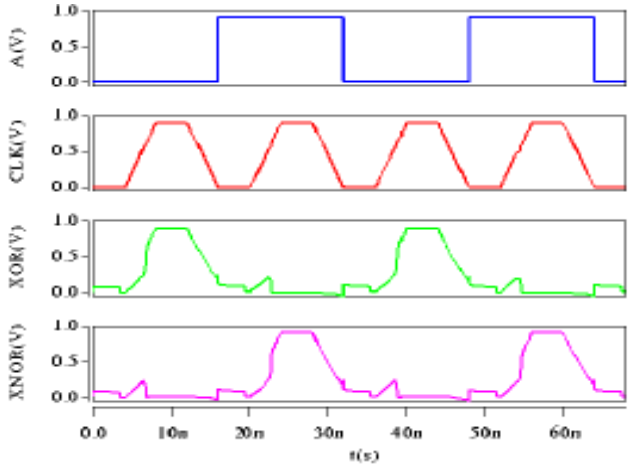

Fig.3.5. Transient response of the proposed adiabatic hybrid MTJ/CMOS.

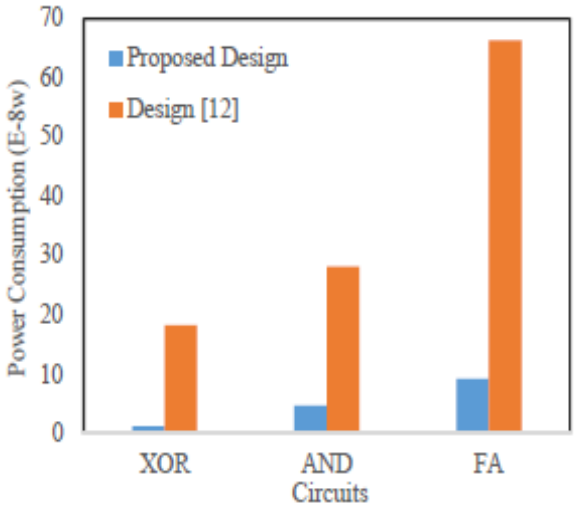

Fig.3.6. Power consumption of the proposed designs and designs.

4. CONCLUSION

Logic-in-Memory (LiM) structures that use magnetic tools along with adiabatic designs are 2 reliable methods to understand reduced power designs. A new structure for making adiabatic crossbreed MTJ-CMOS circuits exists in this paper. We have actually implemented AND/NAND, XOR/XNOR, along with complete adder circuits with this framework. Designs are substitute as well as compared with modern. We utilized Synopsys HSPICE simulator with 32 nm modern-day innovation files to evaluate our formats. The outcomes show that the recommended adiabatic MTJ-CMOS styles have lowered power use contrasted to modern, such that the recommended XOR, AND ALSO, along with complete adder have virtually 13, 6, along with 7 times reduced power consumption particularly contrasted to modern-day.

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