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Paper Authors

N.PRAMEELA RANI, N.G.N PRASAD
KAKINADA INSTITUTE OF ENGINEERING AND TECHNOLOGY,KORANGI,ANDHRAPRADESH,INDIA,533461

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DESIGN OF NANO CALCULATOR FOR ERROR DETECTION BY USING QCA

[1]N.PRAMEELA RANI, [2]N.G.N PRASAD
[1]M.TECH VLSID, DEPT OF E.C.E, KAKINADA INSTITUTE OF ENGINEERING AND TECHNOLOGY,KORANGI,ANDHRAPRADESH,INDIA,533461
[2]ASSOSIATE PROFESSOR, KAKINADA INSTITUTE OF ENGINEERING AND TECHNOLOGY,KORANGI,ANDHRAPRADESH,INDIA,533461

Abstract
Quantum-Dot cellular Automata (QCA) based cryptography is a new paradigm in the field of nanotechnology. The overall performance of QCA is high compared to traditional CMOS technology. In order to achieve data security during nano communication, a cryptography based application is proposed in this article. The devised circuit encrypts the input data and passes it to an output channel through a nano router cum data path selector, where the data is decrypted back to its original form. The results along with theoretical implication prove the accuracy of the circuit. Power dissipation and circuit complexity of the circuit is performed. We increasing the polarization i.e. make the three rotated cells inverter circuit more fault- free by adding extra rotated cells at the output section. In each case, the designed rotated cells inverters have more polarization (i.e. more fault free) than conventional inverters though it has same number of cells. Our finally designed high polarized rotated cells inverter has five cells and its polarization is greater than any type of conventional inverters designed till now.

Keywords: ***Manual; QCA, Majority gate cryptography, Encryption, Decryption, Nanorouter.***

1. INTRODUCTION
Continued and fast dimensional scaling of CMOS eventually will approach the fundamental limit [1]. Also, Short channel effects, high power dissipation, quantum effects are limiting the further scaling of current CMOS technology devices [2-3]. Emerging device technology can overcome the scaling limitation in the current CMOS technology [1]. Single Electron Transistor (SET) [4], Quantum-dot Cellular Automata (QCA) [5] and Resonant Tunneling Diodes (RTD) [6] are some of the "Beyond CMOS" technologies. Among these evolving nanotechnologies, Quantum-dot Cellular Automata is the most favorable technology [1]. QCA is transistorless computational paradigm which can achieve device density of 1012 devices/cm2 and operating speed of THz. QCA device paradigm replaces FET based logic and exploit the quantum effects of small size. Quantum-dot Cellular Automata is a mean of representing binary information on cells, through which no current flows, and achieving device performance by the coupling of those cells [5,7]. This paper presents the state of art survey on QCA basics, implementation, fabrication, tools, defect characterization,

fault model and testing. Also the paper addresses the issues in some of the methods and techniques. Further, the paper suggests the possible research area of QCA.

2. PREVIOUS WORK:

In existing literature, different works are proposed on router circuits in QCA. Nanocommunication that is obtained using QCA technology, a router circuit which works as data path selector circuit was proposed by Das, S., De, D., 2012. A single channel transfer of data from a different source to the expected destination is achieved. Four separate sources are designed in order to route to four different destinations, while utilizing a single channel. A nanorouter is proposed in Sardinha et. al., 2013. The router allows packet of data to be transferred. The building block of the proposed nanorouter comprises of crossbar switch, DEMUX and parallel-to-serial converter. The encryption and decryption processes are implemented using QCA based logic circuits as reported in Kamaraj et al., 2015. A formulation to generate cipher text for QCA based secure nano communication is demonstrated in Kamaraj et al., 2015. Using the nanorouter circuit proposed in Shah et. al., 2011, data from a large number of sources can be routed to their destination using a single path. Unlike current switching in CMOS technology, QCA encodes the binary information as per the position of individual electrons. QCA is the array of cells in which each cell consists of quantum dots also considered as sites that are positioned at the corners of the square cell. The charge is localized in the dots. Also, the cell consists of two mobile electrons that can tunnel between the dots. Electron tunneling out of the cell is not possible due to the potential barriers between cells. Two free electrons resides at the corners of the cells, always diagonally due to Coulombic repulsion.

CMOS METHODOLOGY:

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor. In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd). Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern. CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages.

3. PROPOSED SYSTEM

The proposed security is provided using cryptography. In cryptography (Debnath et al., 2017) the process of conversion of an ordinary text to a cipher text is called Encryption, and its vice versa is called Decryption (Das and De, 2012). This article

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is focused on designing a cryptographic architecture with symmetric key cryptography approach and its implementation in QCA. The architecture is composed of encoder, decoder, and a data path selector. A flowchart of the procedure is shown in Fig. 7. The encoder section contains four inputs and four keys, which undergoes binary conversion and thereafter XOR operation is per-formed within the inputs and keys to obtain the four cipher texts. Now, two select lines S0 and S1 determine which cipher text should be selected from inputs. Once more, two select lines S2 and S3 are present for selecting the output lines i.e. through which output line the output will be transmitted. The decoding procedure takes place here. The cipher text will be XOR-ed with the respective keys to obtain the original texts as depicted in Fig. 7. In the flowchart it is shown that when S0 and S1 or S2 and S3 are unable to select any line, the transmission will stop immediately. The block diagram of the proposed cryptographic architecture is shown in Fig. 8. The component of each part of the architecture shown in Fig. 8 is depicted in Fig. 9. It is seen that the codec is made up with four 2-input XOR gates. The nanorouter circuit has three 2-input multiplexer (Mardiris and Karafyllidis, 2010) and three 2-input demultiplexer circuits.

5. SIMULATION RESULTS

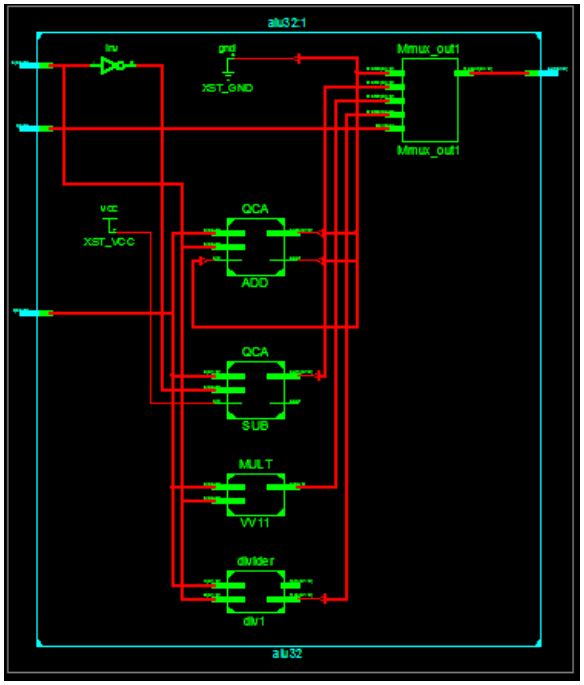

Fig.5.1.Output Results

Simulation results functionally have been obtained using the QCA Designer (Walus et al., 2004) that is a popular engine for QCA circuits. The simulation results of the proposed outlines are shown in Figure 4. The used criterions for the simulation are as follows: samples number: 12,800, convergence tolerance 0.001, radius of effect (bistable and coherence) 65 and 80 nm, threshold (lower and upper) −0.50 and 0.50, scale of cell is 18 nm, separation of layer is 11.50. The decoder circuit involves only 83 cells and covering an extent of 0.08 μm2 , the multiplexer involves of 18 cells and covering an extent of 0.02 μm2 , the flip-flop layout involves only 9 cells and covering an extent of 0.02 μm2 and the nano communication circuit involves of 275 QCA cells with an extent of 0.41 μm2 . It is very essential to create an operationally firm layout in QCA and there are certain concerns realized into account to rise the

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design stability. When building models in QCA, a substantial attempt should be made to maintain the wire length in a specified clocking region to a minimum.

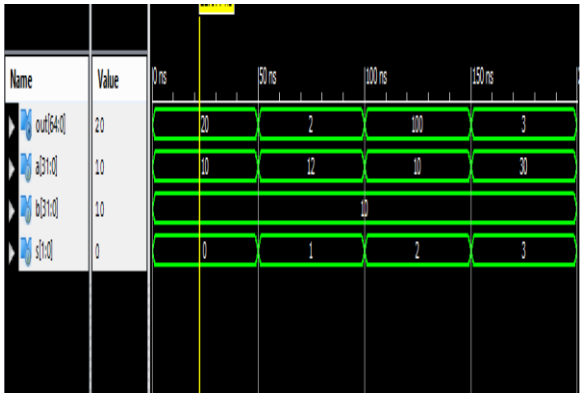

Fig .5.2. power dissipation.

CONCLUSION

Through this paper, the authors have presented a really powerful approach of multiplication, i.E. Urdhva- Tiryakbhyam Sutra based totally on QCA arithmetic. With this technique, the multiplier of any quantity of bits may be designed, and display the computational blessings given by QCA strategies. It is a way for hierarchical multiplier layout which definitely indicates the computational advantages presented through QCA methods. Since the objective changed into to lessen the postpone, the computational direction postpone for the proposed 32x32 bit QCA Wallace multiplier is discovered to be 54.004ns. The QCA Wallace multiplier is a lot extra green than QCA multiplier and Array multiplier in phrases of execution time (pace) and Area Delay Product. So we are able to say QCA arithmetic can be blanketed inside the education systems and help college students study arithmetic rapid and carry out higher in less time. In destiny, all the research centers are to promote research works in QCA arithmetic.

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