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TO AVOID THE SELF TRANSITIONS IN INTER CONNECTION OF VLSI CIRCUITS BY USING QUADRO CODING METHOD

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Abstract

CMOS VLSI circuits having profuse number of gates are interconnected with every part to perform the logical manipulation by input signal. The input signal changes from 0 to 1 or vice-versa, it will change and spread via the circuit and results in power disappearing in the circuit. The charging and discharging of parasitic capacitance is main cause of the power dissipation in the circuit, this is dynamic power dissipation in CMOS circuit. Deep Submicron (DSM) is the one of technology to reduce the area of system. The focus is to reduce the area of CMOS VLSI circuit. There are several methods for the reduction of dynamic power dissipation through energy transition in data buses. Among them a novel Multi coding technique for reducing dynamic power dissipation is proposed by reduction in switching activity of self transitions. In this method, the applied input data is coded in five different ways and the coding resulting in maximum reduction in transition activity is selected. Through this coding scheme the average transition activity is reduced. The coding technique gives better results for longer bus width.

Keywords: **Manual; QCA, Majority gate cryptography, Encryption, Decryption, Nanorouter.**

1. INTRODUCTION

In many digital processors power consumption in the bus is a major part of overall power dissipation. Several bus encoding techniques have been proposed from time to time to reduce the power consumption[1,2,3].The two types of power dissipation is presented such as Dynamic power dissipation and Static power dissipation. In this paper, the focus is on Dynamic power dissipation. The capacitance of interconnect can be classified as coupling capacitance and self capacitance. The coupling capacitance is the capacitance between the adjacent data lines while the self capacitance refers to the capacitance between the substrate and the wire itself [7].The dynamic power in VLSI chip decides the behavior of chip and is highly dependent on the load capacitance and the coupling capacitance i.e. bus line signal

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transitions. This disparity, caused due to the various inductive and capacitive effects, poses a major challenge to VLSI system designers. Much of the power in a bus is dissipated in the process of charging and discharging the high nodal and inter-wire capacitances. Hence, majority of the works [2, 3, 4, 5], which exist in the literature focus on minimizing the bus transition activity. A very popular method among them is the Bus Invert method [3], which does a conditional inversion of the bus lines to minimize the self transitions and thereby reducing the self energy. As we approach Deep Submicron (DSM) and Ultra Deep Submicron (UDSM) technologies, the effect of interwire capacitance becomes significant due the high proximity of the bus lines carrying signals. As a result, many attempts [4-9] to reduce the coupling transition activity also exists. In this paper, the authors propose a new coding technique which minimizes both coupling and self transition activities in the bus lines.

2. PREVIOUS WORK:

Many works have been concentrated on low power bus coding techniques. Quadro coding technique is used to reduce power dissipation[1]. Four type of coding are completed by using even and odd position of given data. Crosstalk reduction is done by using But-Invert coding[2]. These processes are complete by using one control bit. Making partition into two sub buses, then encode only one sub bus while leaving and remaining encode[3].In Bus-Invert coding the hamming distance is larger than half of the bus width, in that pattern is transmitted with each bit inverted. Rearrange the data by their position with respect to total number[4]. For 4-bit bus model the Coditional coded block ware used for coding[5]. There are tow types of the process such as Canonic Sign Digit and Binary Coded Canonic Sign Digit.The design of CMOS is genrated this bus is simply a circuit that connects one part of the circuit to the other[6,8]. A bus may consist of set of parallel lines with repeaters between them. Butterfly structure of FFT is design is genrated and using of Canonic Sign Digit and Banary Coded Canonic Sign Digit was coded[7]

Where ri (x) stand for the serial resistance per unit length of ith line, Cii (x) stand for the capacitance per unit length between the ith line and ground, Cij (x) stand for the capacitance per unit length between the ith line and jth line, mii (x) stand for the self inductance per unit length of the ith line, mij (x) stand for the mutual inductance per unit length between ith and jth line. As long as the resistive component of the wire is small and the switching frequencies are in the low to medium range, it is meaningful to consider only the capacitive component of the wire. For on-chip parallel buses, energy is dissipated in charging and discharging parasitic capacitances. The coupling capacitance between the wires dominates the total parasitic capacitance of wires in DSM technologies. The figure below shows the simplified bus energy model.

3. PROPOSED SYSTEM

The proposed technique called Quadro coding technique is based on reducing the number of transitions occurring on data bus when a new data is to be transmitted. By

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using the following technique self transitions from 0 1 and 1 0 can be reduced as new data is sent on the data bus compared to previous data. Let the data be n bits wide. The proposed coding technique is given as follows:

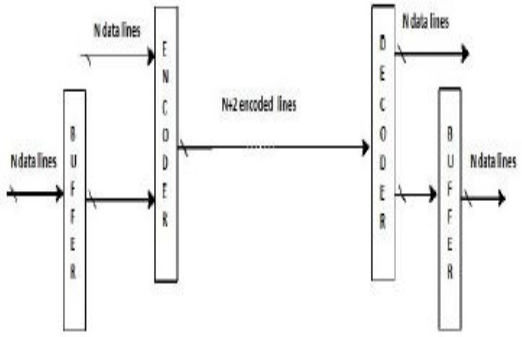


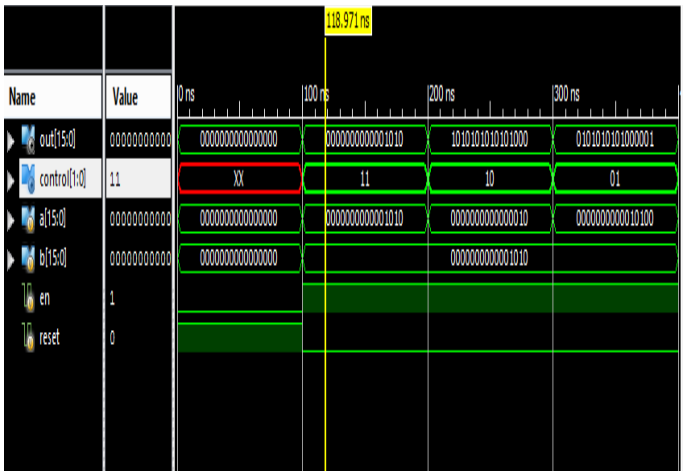
Fig.4.1. Block diagram of complete system

We know that the factors like VDD and f are specific to a particular technology and cannot be altered for a particular purpose so therefore for reducing power dissipation, our main focus will be reducing the transition activity α as whenever a data bit is transmitted on a bus wire, the charging and discharging of this wire capacitance, self capacitance and coupling capacitance, results in power consumption. Dual Coding Technique is introduced to reduce dynamic power dissipation by reducing Coupling Transition activity αC. Techniques to reduce power dissipation were well explored in the literatures like [7] offers a TSC (Two Stage Coding) technique. Literature [8] introduced a technique in which data bus is first divided into two group as odd group and even group and then invert the data or send it as it is according to cases. Paper [9] developed a mathematical model for a memoryless encoding scheme and proposed a novel partitioning method for reducing the transition energy. Literature [10] explored a technique in which input data bits coded in four different ways such as Original Data, Invert Data, Ex-Oring with some code words and Ex-Oring with another code words and then send all the four results in comparator mode, which compares power dissipation value.

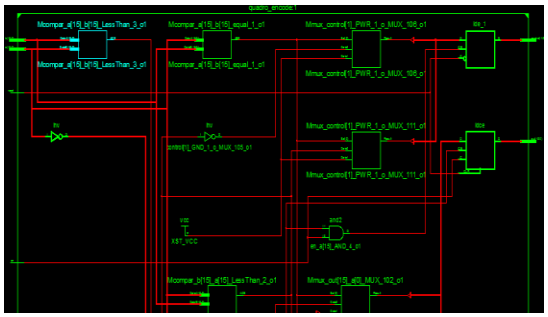
5. SIMULATION RESULTS

```
Timing constraint: Default OFFSET OUT AFTER for Clock 'reset'
  Total number of paths / destination ports: 2 / 2
--------------------------------------------------------------------------------
Offset:              0.754ns (Levels of Logic = 1)
  Source:            control_1 (LATCH)
  Destination:       control<1> (PAD)
  Source Clock:      reset rising

  Data Path: control_1 to control<1>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDE_1:G->Q            1   0.475   0.279  control_1 (control_1)
     OBUF:I->O                 0.000          control_1_OBUF (control<1>)
    ----------------------------------------
    Total                      0.754ns (0.475ns logic, 0.279ns route)
                                       (63.0% logic, 37.0% route)

--------------------------------------------------------------------------------
```

Time summary



encoder



Rtl schematic

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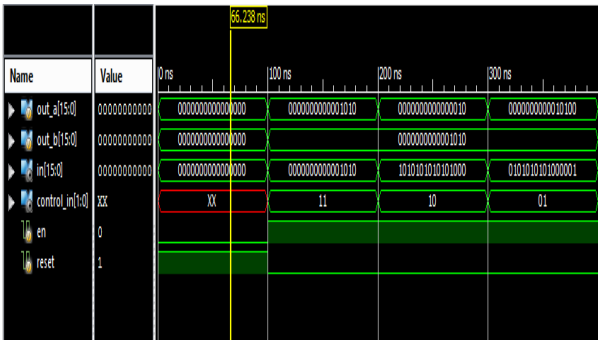
Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	56	63400	0%
Number of fully used LUT-FF pairs	0	56	0%
Number of bonded IOBs	52	210	24%
Number of BUFG/BUFGCTRLs	2	32	6%

Design summary



Decoder

CONCLUSION

This paper provides a unique coding method for reducing transition activity in on-chip buses. The approach has been tested on numerous bus widths and high-quality outcomes are determined for nine bit bus width, where the transition hobby has been reduced by as much as 36%. This big discount in transition hobby consequences in full-size energy saving as much as forty seven%. The electricity saving varies from forty seven% to twenty-five% for eight-bit to 32-bit information bus. It has been determined that the proposed approach is extra suitable for shorter duration buses in comparison to longer buses.

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