International Journal for Innovative Engineering and Management Research

A Peer Revieved Open Access International Journal

www.ijiemr.org

IJEMR Transactions, online available on 3rd Aug 2019. Link :http://www.ijiemr.org/downloads.php?vol=Volume-08&issue=ISSUE-08

Title **DESIGN AND IMPLEMENTATION OF FLIP FLOP CIRCUITS FOR HIGH EFFICIENCY BY USING QCA**

Volume 08, Issue 08, Pages: 79–83.

Paper Authors

B.KARUNA, R.VINAY KUMAR

KAKINADA INSTITUTE OF ENGINEERING AND TECHNOLOGY,KORANGI,ANDHRAPRADESH,INDIA,533461

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

DESIGN AND IMPLEMENTATION OF FLIP FLOP CIRCUITS FOR HIGH EFFICIENCY BY USING QCA

[1]B.KARUNA, [2]R.VINAY KUMAR
[1]M.TECH VLSID, DEPT OF E.C.E, KAKINADA INSTITUTE OF ENGINEERING AND TECHNOLOGY,KORANGI,ANDHRAPRADESH,INDIA,533461
[2]ASSOSIATE PROFESSOR, KAKINADA INSTITUTE OF ENGINEERING AND TECHNOLOGY,KORANGI,ANDHRAPRADESH,INDIA,533461

Abstract
Reversible logic and quantum dot cellular automata (QCA) together can be considered as the most promising technologies for future generation computers. As CMOS circuits are approaching limits in minimizing area and power dissipation, reversible logic and QCA technology have potential to replace CMOS. Moreover, limited research is done on reversible sequential circuits with QCA implementation. This paper targets design and implementation of a basic sequential element, a reversible dual edge triggered D flip flop, using QCA. The logical functionality, computational and power analysis of the proposed circuit has been investigated in this work. This is one of such first attempts to design, analyze and implement reversible sequential element using QCA. This design will facilitate the conception of complex reversible sequential circuits in the area of QCA circuits.
Keywords: **Flip-flop; Majority gate; Quantum Dot; Kink energy; Energy Dissipation**.

1. INTRODUCTION

QUANTUM dot cellular automata (QCA) is one of the emerging technologies that shows features to overcome the limitations like high computation throughput and power consumption faced in CMOS technologies. A lot of research has been done in designing universal logic gates, combinational circuits, sequential circuits and ALU using QCA and has shown its efficiency due to its small size and high computational speed. Apart from these advantages of QCA, it also has a great potential for low power consumption. Among several other alternatives, Quantum Dot Cellular Automata (QCA) is a revolutionary promising transistor less quantum paradigm that performs computation and routing information at Nano domain. The unique feature of QCA is that logic states are represented by a cell. A cell is a Nano scale device capable of transferring data by two state electron configurations. Alternatives to conventional CMOS technology is QCA which provides higher density, lower dissipation of power, higher clock frequency and better output results are needed. Quantum Dot Cellular Automata (QCA) technology is explored and introduced. When a new technology is introduced, new design principles are also necessary to consider. The design nature of QCA is not very complicated, instead it is simple than the conventional technologies.

2. PREVIOUS WORK:

After the introduction of QCA, numerous designs of combinational and sequential QCA circuits have been reported. However, there are very few papers which describe reversible circuits with QCA implementation. As currents and voltage levels are not utilized in QCA, the power consumption is negligible. Timler and Lent in 2002 depict power dissipation and gain in QCA cell. Nevertheless, a number of studies have focused on power analysis of QCA circuits. An upper bound power dissipation model for QCA circuits was reported by Srivastava et al. First ever tool for power analysis QCApro was illustrated by Srivastava et al. which brings transformation in QCA circuit analysis. Some articles demonstrated different methods of power calculation in QCA circuits. Few research papers have reported power analysis of certain logical gates such as XOR gates using QCA circuits. Reversible computation is known for its application in loss less computing and quantum dot cellular automaton (QCA) is known for its exceptional properties such as exceedingly high density and high operation speed with ultra-low power dissipation. Definitely merging reversibility in QCA domain will add tremendous benefits resulting in ultra low power, highly dense circuits for future generation computers. Implementation of few reversible gates such as Fredkin gate, Feynman gate and their power analysis is reported. Sequential circuits form core of the digital systems; thus in this paper authors have shown the implementation of basic building blocks of sequential circuits and their detailed analysis. The term CMOS stands for "Complementary Metal Oxide Semiconductor". CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application specific integrated circuits (ASICs).

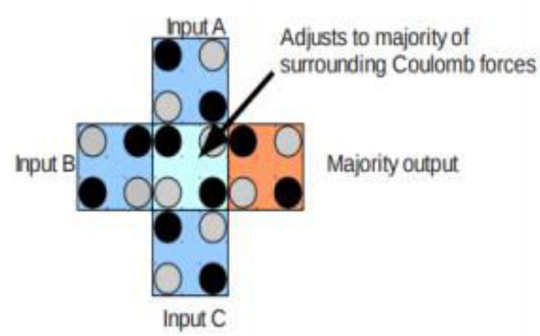

Fig.2.1. QCA model.

CMOS METHODOLOGY:

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor. In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd). Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern. CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages.

3. PROPOSED SYSTEM

QCA is a novel emerging technology in which logic states are not stored as voltage levels, but rather the position of individual electrons. Conceptually, QCA represents binary information by utilizing a bi-stable charge configuration rather than a current switch. Unlike conventional logic circuits in which information is transferred by electrical current, QCA operates by the Columbic interaction that connects the state of one cell to the state of its neighbors. Hence the information transfer (interconnection) is the same as information transformation (logic manipulation) in the QCA technology. The QCA cell in contrast to electronics based on transistors, QCA does not operate by the transport of electrons, but by the adjustment of electrons in a small limited area of only a few square nanometers. QCA is implemented by quadratic cells, the so-called QCA cells. In these squares, exactly four potential wells are located, one in each corner of the QCA cell. In the QCA cells, exactly two electrons are locked in. They can only reside in the potential wells. The potential wells are connected with electron tunnel junctions. There are two diagonals in a square, which means the electrons can reside in exactly two possible adjustments in the QCA cell. Regarding these two arrangements, they are interpreted as a binary '0' and binary '1', i.e. each cell can be in two states. The state '0' and the state '1', as shown in figure 3. A binary system is something familiar, as Boolean logic is used already in today's computers. There, a high voltage is often interpreted as binary '1' and a low voltage as binary '0'

5. SIMULATION RESULTS

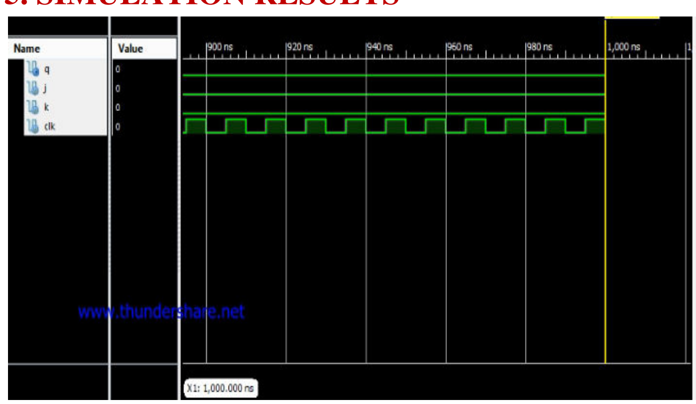

Fig.5.1.Output Results

The minimum energy requirement to dissipate the energy between the two neighboring cells is kink energy and is less

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

than from the equation 3 because if more energy is given at the input cell, then there will be more tunneling of quantum dots from one potential well to another potential well then there is a possibility of extra energy to dissipate due to the rotational tunneling and remains same polarization as before. This rotational tunneling may not happen in the previous cells because these cells are already adjusted accordingly and it is difficult to modify them again within the QCA design. We cannot predict the electron tunneling as well as we cannot distinguish that the same electron will remain same position. Ina cell of two electrons, they may exchange their position and it will happen when the applied dissipated energy is more than the required. In that case to stabilize the energy within the cell, the electrons may rotate their position.

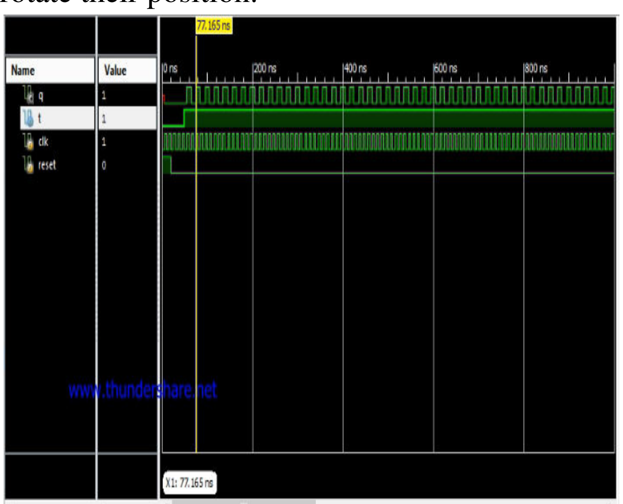

Fig .5.2. power dissipation.

CONCLUSION

In this paper we have developed a standard equation from SR flip flop and using that equation other flip flops like D, T and JK flip-flops are subsequently designed. This is a new approach of designing flip-flops with less hardware complexity in nanotechnology. Any memory storage device can be built using the flip-flops designed in the above mentioned approach. The layout has been generated and simulation results are verified using QCA Designer simulation tool. The stability of the circuit has been clearly determined by the 3-D plots of kink energy of the two possible combinations of the output cell. In future there is a scope for design other sequential circuits like registers, counters, memory blocks and other flip flops using this generalized block.

REFERENCES

[1] M. Furdek, M. Danko, P. Glavica, L. Wosinska, B. Mikac, N. Amaya, G. Zervas, and D. Simeonidou, "Efficient optical amplification in selfhealing synthetic ROADMs," in 2014 International Conference on Optical Network Design and Modeling, May 2014, pp. 150–155.

[2] S. M. Bowers, K. Sengupta, K. Dasgupta, B. D. Parker, and A. Hajimiri, "Integrated self-healing for mm-wave power amplifiers," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 3, pp. 1301–1315, 2013.

[3] I. Ivan, C. Boja, and A. Zamfiroiu, "Self-healing for mobile applications," Journal of Mobile, Embedded and Distributed Systems, vol. 4, no. 2, pp. 96–106, 2012.

[4] K. Khalil, O. Eldash, and M. Bayoumi, "Self-healing router architecture for reliable network-on-chips," in IEEE International Conference on Electronics, Circuits and Systems (ICECS). IEEE, 2017.

[5] S. Narasimhan, S. Paul, R. S. Chakraborty, F. Wolff, C. Papachristou, D.

J. Weyer, and S. Bhunia, "System level self-healing for parametric yield and reliability improvement under power bound," in Adaptive Hardware and Systems (AHS), 2010 NASA/ESA Conference on. IEEE, 2010, pp. 52–58.
[6] M. R. Boesen, J. Madsen, and P. Pop, "Application-aware optimization of redundant resources for the reconfigurable self-healing eDNA hardware architecture," in 2011 NASA/ESA Conference on Adaptive Hardware and Systems (AHS), June 2011, pp. 66–73.
[7] Q.-Z. Zhou, X. Xie, J.-C. Nan, Y.-L. Xie, and S.-Y. Jiang, "Fault tolerant reconfigurable system with dual-module redundancy and dynamic reconfiguration," vol. 9, no. 2, 2011, pp. 167–173.
[8] T. Koal, M. Ulbricht, P. Engelke, and H. T. Vierhaus, "On the feasibility of combining on-line-test and self repair for logic circuits," in 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS), April 2013, pp. 187–192.
[9] K. Khalil, O. Eldash, and M. Bayoumi, "A novel approach towards less area overhead self-healing hardware systems," in International Midwest Symposium on Circuits and Systems (MWSCAS). IEEE, 2017.