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HIGH SPEED AND LOW POWER IMPLEMENTATION OF APPROXIMATE MULTIPLIERS USING ADAPTIVE FILTER

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Abstract: This paper presents a precise analysis of the critical path of the least - mean - square (LMS) adaptive filter for deriving its architectures for high - speed and low-complexity implementation. It is shown that the directform LMS adaptive filter has nearly the same critical path as its transpose-form counterpart, but provides much faster convergence and lower register complexity A multiplier has a significant impact on the speed and power dissipation of an arithmetic processor. Precise results are not always required in many algorithms, such as those for classification and recognition in data processing. Moreover, many errors do not make an obvious difference in applications such as image processing due to the perceptual limitations of human beings. Multiplication is often a fundamental function for many of these applications. An adaptive filter is used to the convergence rate and misalignment noise of with arbitrary correlation-multiplier non-linearity. A Tabu search algorithm and scheduling algorithm is then investigated as an application of the multiplier.

Index Terms: **Adaptive filters, least mean square algorithms, LMS adaptive filter**

I. INTRODUCTION

Filters of some sort are essential to the operation of most electronic circuits. It is therefore in the interest of anyone involved in electronic circuit design to have the ability to develop filter circuits capable of meeting a given set of specifications. In circuit theory, a filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Ideally, a filter will not add new frequencies to the input signal, nor will it change the component frequencies of that signal, but it will change the relative amplitudes of the various frequency components and/or their phase relationships. Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject signals in other frequency ranges. Such a filter has a gain which is dependent on signal frequency Arithmetic units such as adders and multipliers are key components in a logic circuit. The speed and power consumption of arithmetic circuits significantly influence the performance of a processor. High-performance arithmetic circuits such as Carry Look Ahead Adders (CLAs) and Wallace tree multipliers have been widely utilized. However, traditional arithmetic circuits that perform exact operations are encountering difficulties in performance improvement. Approximate arithmetic that allows a loss of accuracy

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can reduce the critical path delay of a circuit. Since most approximate designs leverage simplified logic, they tend to have a reduced power consumption and area overhead. Thus, approximate arithmetic is advocated as an approach to improve the speed, area and power efficiency of a processor due to the error-resilience of some algorithms and applications. As a significant arithmetic module, the multiplier has been redesigned to lots of approximate version. The often conflicting advantages and disadvantages of these designs make it difficult to select the most suitable approximate multiplier for a specific application

Thus, approximately redesigned multipliers are reviewed in this paper and a comparative evaluation is performed by considering both the error and circuit characteristics. Energy minimization is one of the main design requirements in almost any electronic systems, especially the portable ones such as smart phones, tablets, and different gadgets. It is highly desired to achieve this minimization with minimal performance (speed) penalty. Digital Signal Processing (DSP) blocks are key components of these portable devices for realizing various multimedia applications. The computational core of these blocks is the arithmetic logic unit where multiplications have the greatest share among all arithmetic operations performed in these DSP systems. Therefore, improving the speed and power/energy-efficiency characteristics of multipliers plays a key role in improving the efficiency of processors. Applying the approximation to the arithmetic units can be performed at different design abstraction levels including circuit, logic, and architecture levels, as well as algorithm and software layers. The approximation may be performed using different techniques such as allowing some timing violations (e.g., voltage over scaling or over clocking) and function approximation methods (e.g., modifying the Boolean function of a circuit) or a combination of them . In the category of function approximation methods, a number of approximating arithmetic building blocks, such as adders and multipliers, at different design levels have been suggested

II. ADAPTATION ALGORITHM

The basic configuration of an adaptive filter, operating in the discrete time domain n, is illustrated in Figure 1. In such a scheme, the input signal is denoted by x(n), the reference signal d(n) represents the desired output signal (that usually includes some noise component), y(n) is the output of the adaptive filter, and the error signal is defined as e(n) =d(n) − y(n). The error signal is used by the adaptation algorithm to update the adaptive filter coefficient vector w(n) according to some performance criterion. In general, the whole adaptation process aims at minimizing some metric of the error signal, forcing the adaptive filter output signal to approximate the reference signal in a statistical sense. There are several adaptation algorithms with different performance criterion. Due to its low complexity and proven robustness, Least Mean Square (LMS) algorithm is used hereLMS algorithm is a noisy approximation of steepest descent algorithm. It is a gradient type algorithm that updates the coefficient vector by taking a step in the direction of the negative gradient of the objective function.

$$w(n+1) = w(k) - \frac{\mu}{2} \frac{\delta Jw}{\delta w(n)}$$

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LMS Algorithm:

For each n

$$\mathbf{w}_{n+1} = \mathbf{w}_n + \mu \cdot e_n \cdot \mathbf{x}_n$$

Where

$$e_n = d_n - y_n \quad y_n = \mathbf{w}_n^T \cdot \mathbf{x}_n$$

Where, the input vector xn, and the weight vector wn at the nth iteration are, respectively, given by

$$\mathbf{x}_n = [x_n, x_{n-1}, \ldots, x_{n-N+1}]^T$$
$$\mathbf{w}_n = [w_n(0), w_n(1), \ldots, w_n(N-1)]^T$$

dn is the desired response, yn is the filter output, and en denotes the error computed during the nth iteration. μ is the step-size, and N is the number of weights used in the LMS adaptive filter.

2.1 Implementation of Direct - Form Delayed LMS Algorithm

In the case of pipelined designs with m pipeline stages, the error e(n) becomes available after m cycles, where m is called the "adaptation delay." The DLMS algorithm therefore uses the delayed error en−m, i.e., the error corresponding to (n − m)th iteration for updating the current weight instead of the recent-most error. The weight-update equation of DLMS adaptive filter is given by

$$\mathbf{w}_{n+1} = \mathbf{w}_n + \mu \cdot e_{n-m} \cdot \mathbf{x}_{n-m}.$$

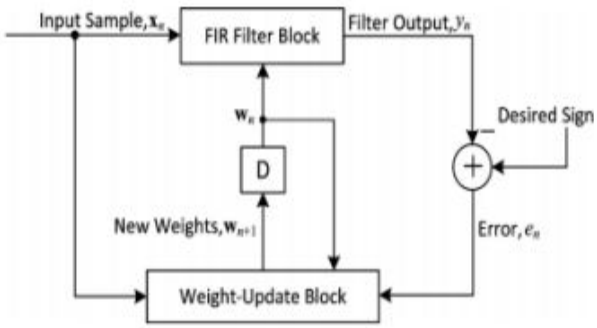

Fig 1: Structure of the conventional LMS adaptive filter

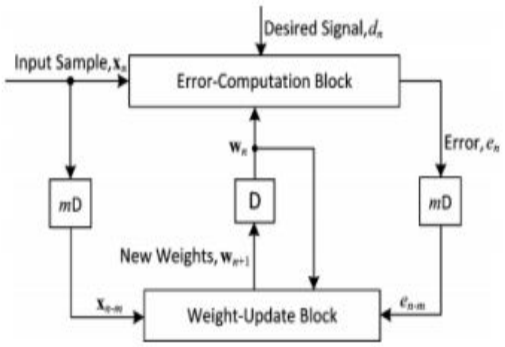

Fig 2: Generalized block diagram of direct form DLMS adaptive filter

Since all weights are updated concurrently in every cycle to compute the output according to (1), direct-form realization of the FIR filter is a natural candidate for implementation. However, the direct-form LMS adaptive filter is often believed to have a long critical path due to an inner product computation to obtain the filter output. This is mainly based on the assumption that an arithmetic operation starts only after the complete input operand words are available/generated. For example, in the existing literature on implementation of LMS adaptive filters, it is assumed that the addition in a multiply-add operation can proceed only after completion of the multiplication, and with this assumption, the critical path of the multiply-add operation (TMA) becomes (TMULT + TADD) , where TMULT and TADD are the time required for a multiplication and an addition, respectively. Under such assumption, the critical path of the directform LMS adaptive filer (without pipelining) can be estimated as

$$T = 2\,T_{MULT} + (N+1)\,T_{ADD}$$

A generalized block diagram of direct-form DLMS adaptive filter is shown in Fig.2.It consists of an errorcomputation block (shown in Fig. 3) and a weight-update block (shown in Fig. 4). The number of delays shown in Fig. 2

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corresponds to the pipeline delays introduced due to pipelining of the error-computation block.

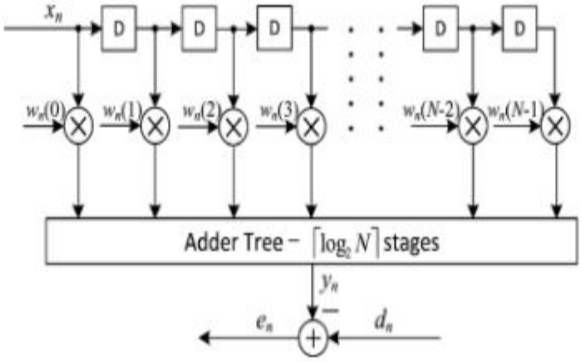

Fig 3: Error - computation block of Fig .2

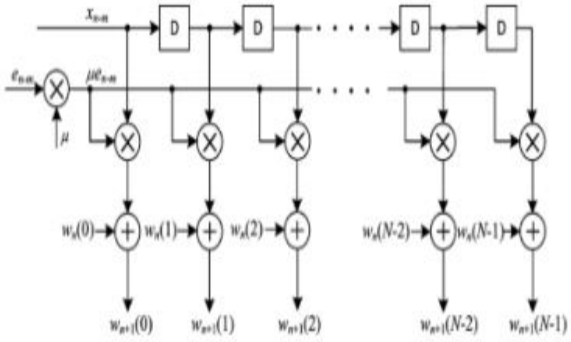

Fig 4: Weight – update block of Fig . 3

2.2 Implementation of Transpose-Form Delayed LMS Algorithm

The transpose-form FIR structure cannot be used to implement the LMS algorithm given by (1), since the filter output at any instant of time has contributions from filter weights updated at different iterations, where the adaptation delay of the weights could vary from1to .It could, however, be implemented by a different set of equations as follows:

$$y_n = \sum_{k=0}^{N-1} x_{n-k} w_{n-k}(k)$$

$$w_{n+1}(k) = w_n(k) + \mu e_n x_{n-k}$$

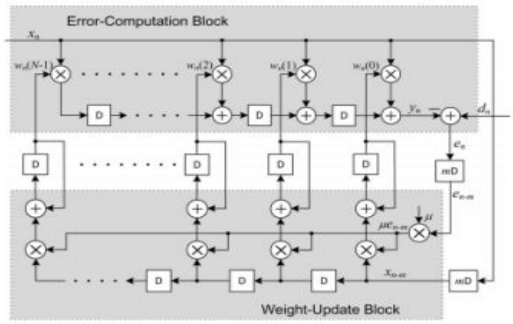

Fig 5: Structure of transpose-form DLMS adaptive filter

If additional delays are introduced in the error computation at any instant, then the weights are required to be updated according to the following equation

$$w_{n+1}(k) = w_n(k) + \mu e_{n-m} x_{n-m-k}$$

III. PROPOSED SYSTEM

The approximation of a multiplier offers an effective approach to obtain low hardware utilization. The adaptive filter used to convert the value in binary. As constrained by a low error rate, all three designs have a very high accuracy, so both truncation and approximation are used in the multiplier design to further reduce power, area and delay. In proposed two techniques are used Tabu search algorithm and scheduling algorithm. The designs are used to improve the error rate and increase the performance.

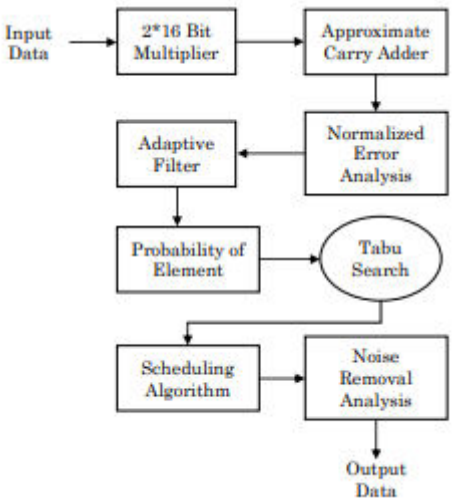

Fig 6: block diagram

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Tabu search can be seen as an extension of hill climbing heuristics. The main difference between the two methods is that, unlike hill climbing heuristics, Tabu search does not stop in local optima but it keeps moving to the best solution inside the neighborhood of the current solution, while expecting that this non-improving move can lead to the identification of a better local optimum further in the process. In order to avoid cycling between a solution and a local optimum that has been previously visited by the algorithm, Tabu search uses information structures called Tabu lists. This list stores a given number of moves that would lead to a previous local optimum. The size and contents of Tabu lists depend on the problem but they are usually not very long (typically short-term memory is used for the lists) and mostly they contain the inverse of the last few modifications made to the current solution. Based on the characteristics of the problem in hand, some Tabu constraints are defined and Tabu lists are constructed according to these constraints. Tabu constraints are usually stated to make reversal or in some cases repetition of some moves impossible.

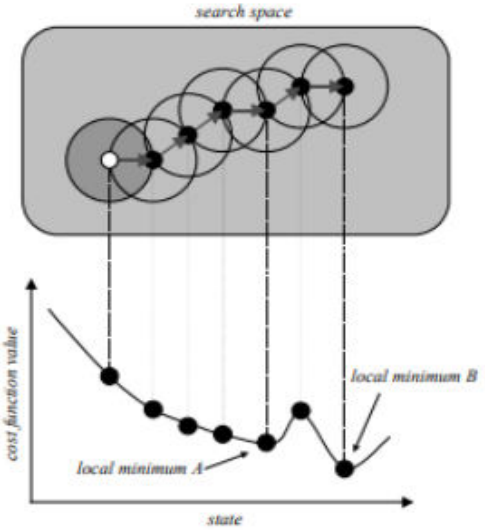

Fig 7: Searching Process

An adaptive filter is a digital filter that has self adjusts uniqueness. Adaptive filters, on the other hand, have the ability to adjust their impulse response to filter out the correlated signal in the input. They necessitate little or no a priori information of the indication and noise uniqueness. (They necessitate a signal (desired response) that is correlated in some sense to the signal to be estimated). Moreover adaptive filters have the ability of adaptively track the signal under non-stationary conditions.

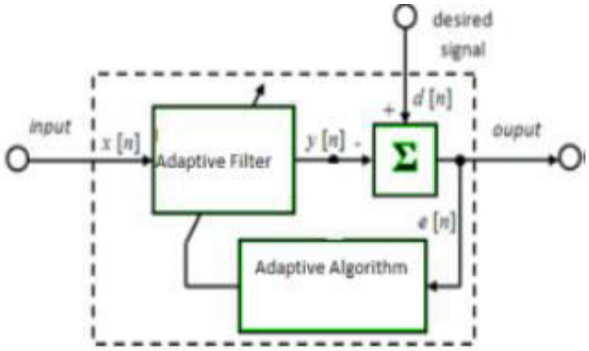

Fig 8: Adaptive Algorithm

Adaptive filters are composed of three basic modules such as filtering structure, performance criterion and adaptive algorithm. The filtering structure determines the output of the filter from given input samples. FIR is preferred over the IIR for filtering due to stability measures. Then, the performance criterion is chosen according to the application and it is used to derive the adaptive algorithm. The three generally used performance criteria are mean squared error, least squares and weighted least squares. Finally, the adaptive algorithm is used to update the filter coefficient based on the performance criterion to improve the performance. The three generally used performance criteria are mean squared error, least squares and weighted least squares. Finally, the adaptive algorithm is used to update the filter coefficient based

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on the performance criterion to improve the performance. Scheduling involves the purpose of establish and the production levels for each unit over a given scheduling period. The schedule is subject to a number of system and unit constraints. To make the paper self-contained and to develop the algorithm for the case with a bound on maximum demand, we first briefly explain a simpler problem without a bound on Maximum Demand.

The partial product perforation method is applied to various multiplier architectures in order to explore how their power consumption, area, delay, and accuracy behave, considering the perforation configuration variables j and k. This analysis targets to expose the optimal architecture– configuration pair for determined error values regarding both power dissipation and area complexity. This is critical, since different configurations may not have the same impact on multiplier architecture, e.g., architecture may be the power optimal one when accurate calculations are performed, but suboptimal when partial product perforation is applied.

A critical issue for the approximate computing is the error imposed during computations and how it affects the final result. In this section, an error evaluation analysis of the partial product perforation technique is presented. The previous analysis provides rigorous expressions of error metrics, enabling a fast error analysis of differing product perforation configurations. In this section, we introduce two methods to decrease the error induced from the application of partial product perforation. They are implemented as extra components complementing the multiplication circuit, thus their area, power, and delay overheads as well as the error reduction they offer, do not depend on the architecture of the multiplier

IV. SIMULATION RESULTS

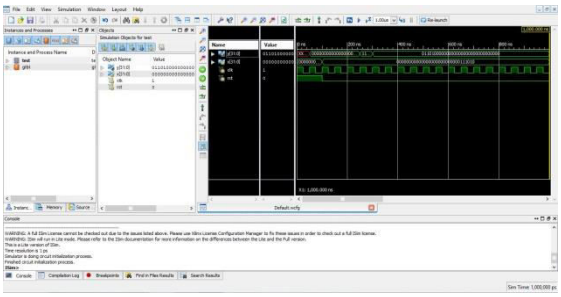

Fig 9: Simulation result of the proposed system

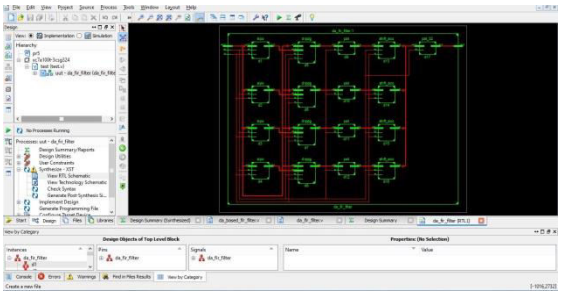

Fig 10: RTL schematic of the proposed system

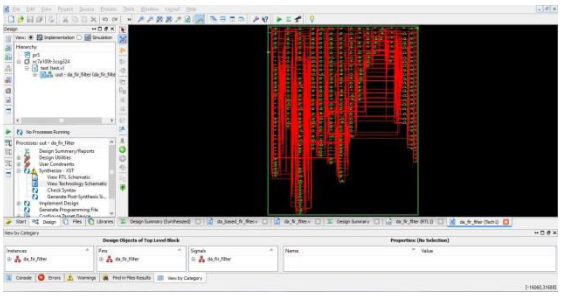

Fig 11: Technology schematic of the proposed system

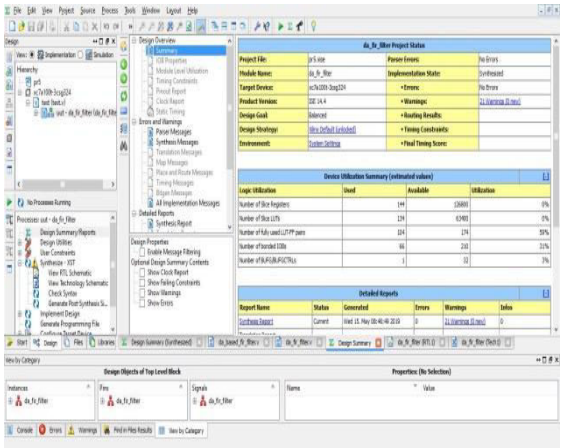

Fig 12: Summary report of the proposed system

Table 1: comparison of the lms adaptive filters

	LUT	Delay	Area
Convolutional LMS	22	37.766 ns	383308 kb
Proposed LMS	27	12.378 ns	376852 kb
Modified LMS	134	5.987 ns	376540 kb

V. CONCLUSION

Approximate circuits have been considered for error-tolerant applications that can stand a little defeat of correctness with improved performance and energy efficiency. Multipliers are key arithmetic circuits in many such applications such as digital signal processing (DSP). Approximate unsigned multipliers are comparatively evaluated for both error and circuit characteristics. Among the considered approximate multipliers, truncation on part of the partial products is an effective way to reduce circuit complexity. It is shown that by utilizing an appropriate error recovery, the proposed approximate multiplier achieves similar processing accuracy as traditional exact multipliers but with significant improvements in power and performance. Precision is improved and mean relative error figures are small. Approximate compute gives maximum peak signal to noise ratio.

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