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PERFORMANCE ANALYSIS AND IMPLEMENTATION OF HIGH SPEED FULL-ADDER USING MODIFIED GDI TECHNIQUE

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ABSTRACT: This paper presents a design which provides full swing output for logic 1 and logic 0 for 1-bit full adder cell and reduces power consumption, delay, and area. In this design full adder consists of two XOR gate cells and one cell of 2x1 multiplexer (MUX). The performance of the proposed design compared with the different logic style for full adders through Tanner tool based on TSMC 65nm technology models The simulation results showed that the proposed full adder design dissipates low power, while improving delay and area among all the design taken for comparison.

I.INTRODUCTION

A adder is one of the significant building blocks in the construction of a binary Multipler . In ecent times, applications are aimed at battery operated devices so that power dissipation becomes one of the primary design constraints [3]–[10]. In the past processor speed, circuit speed, area, performance, cost and reliability were of prime importance. Power consumption was of secondary concern. However, in recent years power consumption is being given equal importance. The reason for such a changing trend is attributed probably due to the rapid increase in portable computing devices and wireless communication systems which demand high speed computations and complex functionality with low power consumption. In addition to this high performance processors consume severe power which in turn increases the cost associated with packaging and cooling.

Subsequently there is a rise in the power density of VLSI chips thereby disturbing the reliability. It has been found that every 10o rise in operating temperature roughly doubles the failure rate of components made up of Silicon due to several Silicon failure mechanisms such as thermal runaway, junction diffusion, electro migration diffusion, electrical parameter shift, package related failure and Silicon interconnect failure [11]. From the environment point of view, the lesser the power dissipation of electronic components, lesser will be the heat dissipated in rooms which in turn will have a positive impact on the global environment. Also, lesser electricity will be consumed. Therefore, for further optimization of performance of a full subtractor in terms of power consumption, delay time as well as Power

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Delay Product (PDP), a new low power, high speed energy efficient full subtractor is being proposed using Gate Diffusion Input (GDI) technique. GDI is a novel modus operandi for low power digital circuits. This procedure allows reduction in power consumption, propagation delay and transistor count of digital circuit. The method can be used to minimize the number of transistors compared to conventional Complementary Pass-transistor Logic (CPL) and Dual Pass transistor Logic (DPL) CMOS design. The proposed subtractor has a transistor count of 14 a reduction of 72.00%, 63.16% and 58.82% compared to a full subtractor composed of CMOS logic, transmission gates and CPL, proposing a reduction in area. In order to establish the technology independence of the design the proposed subtractor has been simulated using 150nm technology.

II. GATE DIFFUSION INPUT (GDI)

Gate Diffusion Input (GDI) method is based on the utilization of a simple cell as shown in Fig. 1 which can be used for low power digital circuits [3]. This technique is implemented in twin-well CMOS or Silicon on Insulator (SOI) technologies. In this process, the bulks of both NMOS and PMOS transistors are hardwired to their diffusions to reduce the bulk effect that is dependence of threshold voltage on source-to-bulk voltage [12]. The dependence of transistor threshold voltage on source-to-bulk voltage is as follows:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) - \eta V_{DS}$$

Where VSB is source-body voltage, Vth0 is threshold voltage at VSB=0, γ is linearized body coefficient, ΦF is the Fermi potential and η is Drain nduced Barrier Lowering (DIBL) coefficient. Using this procedure power consumption can be reduced along with delay time thereby delivering a reduced power delay product. Consequently area of the circuit is minimized.

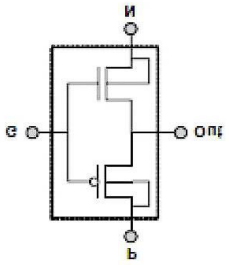

Figure 1: Basic GDI Cell

It should be noted that though the circuit resembles with standard CMOS inverter, there are certain important differences compared to conventional one. The GDI cell contains 3 inputs— P which is the input to the outer diffusion node of the PMOS transistor is not connected to Vdd while N which is the input to the outer diffusion node of the NMOS transistor is not connected to GND, and G which is the common gate input of both the NMOS and PMOS transistors. The Out node which is the common diffusion of both the transistors may be utilized as input or output port depending on the circuit configuration.

The ports P and N delivers 2 extra pins which yield the GDI design more compliant than the usual CMOS design [3]. Fig. 2 shows the transient response of a GDI cell which is quite similar to that of a standard CMOS inverter [13], [14]. This analysis is based on the Shockley model in which the drain current ID is represented as shown below

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$$I_D = \begin{cases} I_{D0}\left(\frac{W}{L}\right) e^{(qV_{GS}/KT)} \\ \quad (V_{GS} \le V_{TH} : \text{subthreshold region}) \\ K\{(V_{GS} - V_{TH})V_{DS} - 0.5V_{DS}^2\} \\ \quad (V_{DS} < V_{GS} - V_{TH} : \text{linear region}) \\ 0.5K(V_{GS} - V_{TH})^2 \\ \quad (V_{DS} \ge V_{GS} - V_{TH} : \text{saturation region}) \end{cases}$$

Where K denotes device trans conductance parameter, VTH denotes threshold voltage, W denotes channel width and L denotes channel length.

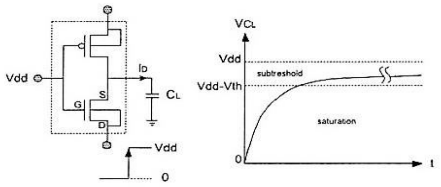

Figure 2: Transient response of a GDI cell

However, it is to be mentioned that in GDI cell Vds has to be considered as a variable of input voltage in Shockley model [3] in contrast with CMOS inverter analysis [15] where Vgs was considered as an input voltage.

III.LOGIC GATES BASED ON GDI METHOD

Table I shows the various operations that can be performed with a basic GDI cell.

TABLE I. DIFFERENT OPERATIONS OF BASIC GDI CELL

N	P	G	Out	Operation
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}$+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}$B+AC	MUX
'0'	'1'	A	$\bar{A}$	NOT

From table I, it can be noticed that using only 2 transistors various functions can be performed. For instance, OR gate can be designed using a single GDI cell whereas in case of designing of an OR gate gate can be designed using only 2 transistors and even a Multiplexer MUX) can be devised using a single GDI cell. Thus, a simple alteration to the input configuration of the GDI cell would yield myriad variety of Boolean functions. Multiple-input gates can be implemented by combining several GDI cells.

IV PROPOSED SYSTEM

Full adder is a combinational circuit that performs the arithmetic operation of 3 number of bits. Addition considered an essential operation in arithmetic and logic unit digital signal processing and. The 1-bit full adder contains three input bits and two output bits, the first two bits of the inputs are A and B called operands and the third input bit Cin is a bit carried in from the previous less-significant stage, output bits called sum is the result of addition operation and carry out which will be the input carry to the next addition operation, and the expression:

$$SUM = A \oplus B \oplus Cin$$

$$COUT = A\,\overline{(A \oplus B)} + Cin\,(A \oplus B)$$

The proposed design consists of 16 transistors including two XOR gate cells to produce sum and one multiplexer cell to produce carry out, as shown in figure (1), the block diagram shown in figure (2), and the truth table of proposed full adder presented in table I

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A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table I. Truth Table Of Proposed Full Adder

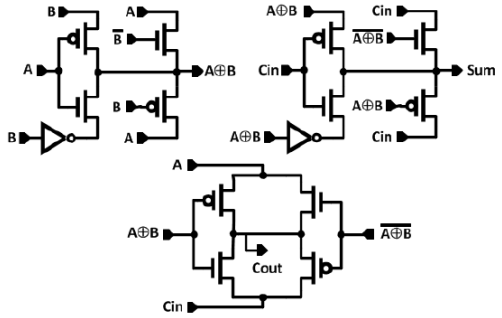

Fig.3. Proposed design for 1-Bit Full Adder

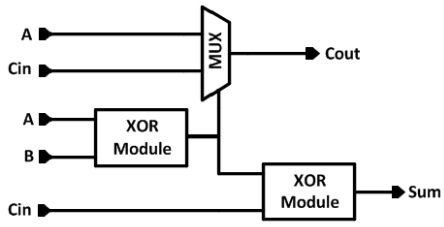

Fig. 4. Block Diagram For Proposed Full Adder

The major benefit of using GDI technique is that a large number of functions can be implemented using this technique. We can see from the table 2 that GDI can be used for implementing various designs such as MUX, AND, OR etc. The most complex design among these is the designing of MUX, which can be done using 2 transistors. Whereas using other conventional techniques it requires 8-10 transistors for designing a MUX. The main drawback of GDI technique is that of swing degradation. This is due to threshold loss and to eliminate this we have to use silicon on insulator or twin-well process to realize, which is very expensive. Designing a full adder the major building block is XOR gate using GDI technique.

V IMPLEMENTATION

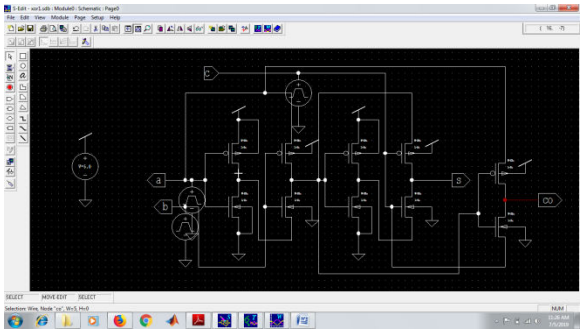

Fig 5 Circuit Design

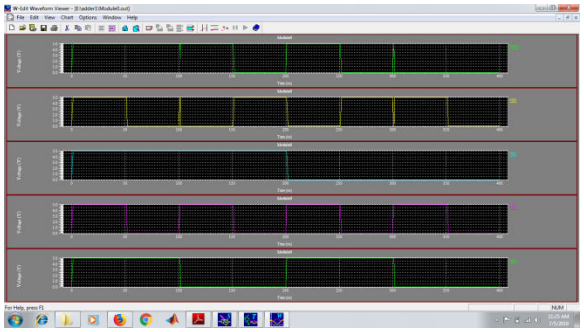

Fig 5 Simulation Result

VI CONCLUSION

The goal of this paper was to design a full adder with high speed performance using GDI technique. From the performance analysis table it is clear that the proposed design system is the best among the discussed designs in terms of area, delay and power dissipation. Since the results were obtained as an outcome of simulation, the readings are precise. This design will have an improved speed and also the efficiency of the system is more compared to all the conventional techniques. Further

modifications can be made in the design by adding a few more transistors.

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