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A NOVEL METHOD OF VOLTAGE DYNAMIC VOLTAGE RESTORER (DVR) BASED ON FIVE LEVEL MLI CONVERTER FOR POWER QUALITY IMPROVEMENT

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Abstract— In the present electric power grids, power quality issues are recognized as a crucial concerns and a frequently occurring problem possessing significant costly consequence such as sensitive load tripping and production loss. Consequently, demand for high power quality and voltage stability becomes a pressing issue. Dynamic voltage restorer (DVR), as a custom power device, is one of the most effective solutions for "restoring" the quality of voltage at its load-side terminals when the quality of voltage at its source-side terminals is disturbed. In this paper, a new DVR topology based on double flying capacitor multicell (DFCM) converter for medium-voltage application has been proposed. The advantage of the proposed DVR is that it does not need any line-frequency step-up isolation transformer, which is bulky and costly, to be connected to medium-voltage power grid. The design and implementation of multilevel voltage source converter based dynamic voltage restorer (DVR) is dealt with in MATLAB Simulink. The objective of this study is to stabilize the voltage by compensating the sag, swell and harmonics in the system. Cascaded Multilevel Converter based DVR is used for harmonics control. This work proposes the enhancement of power transfer capability and maintaining unity power factor. Relative Harmonic analysis is also discussed based on the total harmonic distortion (THD) calculations. Now days the use of sensitive electronic equipment has increase which has lead to power quality problems. The various power quality disturbances are transients, interruptions, voltage sag, voltage swell, voltage collapse, harmonics etc. To solve these power quality problems various custom power devices are used. Dynamic voltage restorer (DVR) is a custom power device used for the Compensation of voltage sag and swell. Power quality problem is an occurrence manifested as a non-standard voltage, current or frequency. One of the major problems dealt here is the voltage sag. Dynamic Voltage Restorer provides a cost effective solution for protection of sensitive loads from voltage sags currents, although the applied voltage being sinusoidal. MATLAB/SIMULINK tool is used for evaluating the performance of the proposed control scheme.

Index Terms – Double Flying Capacitor Multicell Converter; Dynamic Voltage Restorer; Multilevel Power Converters; Power Quality; Voltage Sag.

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I.INRTODUCTION

In recent years, the number of sensitive loads integrated to the power grid has been increased [1]–[3].Consequently, the demand for high power quality and voltage stability becomes a significant issue. In the present power grids, voltage sags are recognized as a serious threat and a frequently occurring power-quality problem and have costly consequence such as sensitive loads tripping and production loss [4]–[7].Voltage sags are results of transient phenomenon in power grid such as short circuits in the upstream power transmission line or parallel power distribution line connected to the point of common coupling (PCC), inrush currents involved with the starting of large machines, sudden changes of load, energizing of transformers or switching operations in the grid [8]–[10]. According to the IEEE STD 1159-2009, voltage sag (also called voltage dip in the IEC terminology) is defined as a decrease of 0.1 to 0.9 p.u. in the rms voltage at system frequency and with the duration of half cycle to one minute [11].Due to the above mentioned effects of voltage sags on sensitive loads, compensating voltage sags and minimizing their effects is necessary. Traditional methods of suppressing voltage variations include tap-changing transformers and uninterruptible power supplies (UPS) [12]. However, tap-changing transformer is bulky, costly and not fast enough to eliminate the voltage sag effects at load side. On the other hand, UPS is bulky and expensive device whose power rating should be same as load power rating [13]. Furthermore, there are custom power devices such as static synchronous compensator (STATCOM), distribution-STATCOM (D-STATCOM), unified power quality conditioner (UPQC), and dynamic voltage restorer (DVR) as power electronics based solutions to minimize costly outcomes of voltage sags [12]. In comparison, DVR is more effective and direct solutions for "restoring" the quality of voltage at its load-side terminals when the quality of voltage at its source-side terminals is disturbed [14]–[17].DVRs compensate voltage sags by injecting the proper amount of voltages in series with the supply voltage, in order to maintain the load side voltage within the specification [18]–[21]. Typically, a DVR consists of an energy storage device and an inverter which is coupled via a series transformer to grid. The purpose of inverter is injecting the series voltage with a controlled magnitude and phase angle to restore the quality of load voltage and avoid load tripping [2], [22], [23].It is worth mentioning that for medium voltage applications it is needed to use step up line-frequency transformer at the output of DVR to be able to connect DVR to medium-voltage power grid. However, this transformer is bulky and heavy and can be a concern in cases with limited area. To avoid this issue, this paper proposes new DVR topology based on double flying capacitor multicell (DFCM) converter for medium-voltage application. With this approach, there is no need to utilize line-frequency step-up transformer at the output of DVR to match power grid voltage rating. This paper is organized as follows.

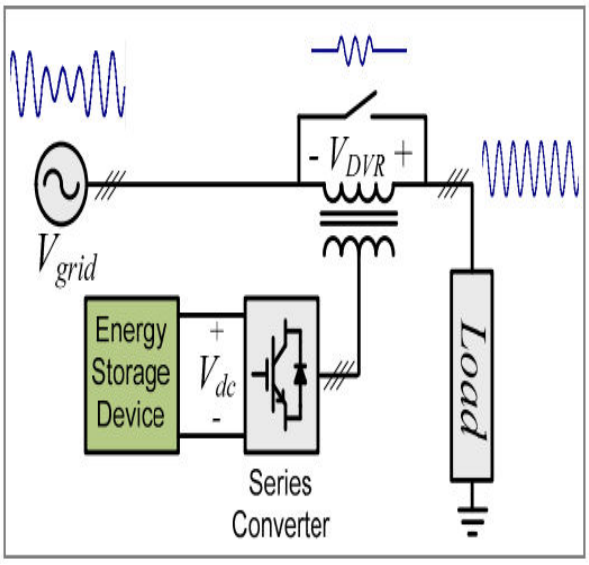

Figure.1.General topology of DVR

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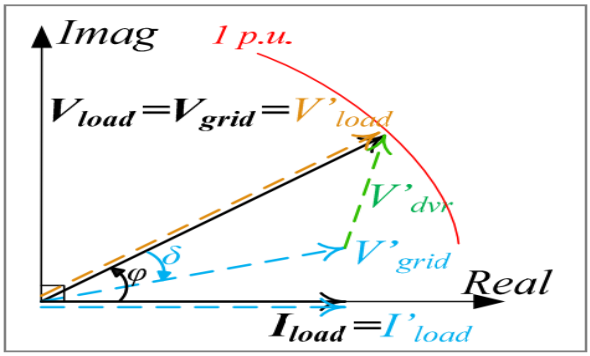

Figure 2.Phasor diagram of pre-sag compensation strategy

II.PRE-SAG COMPENSATION METHOD

The basic concept of DVR is shown in Figure 3.1. A commonly used method for compensating voltage sags is restoring the load voltage to the level and condition before the sag [2], [18]. Therefore, the amplitude and the phase of the voltage before the sag have to be exactly restored [2],[18]. The phasor diagram of the pre-sag compensation strategy is shown in Figure 2. In this figure, dashed quantities (*Vg' rid* ,*Vload'* , *Vdvr'* and *Iload'*) indicate variables after the sag. The phasors prior to the sag are represented by *Vgrid*,*Vload*and *Iload* . Moreover, angle of φ is phase angle difference between the load voltage and load current phasors and angle of δ is phase jump of grid voltage during the voltage sag. All of the load and grid voltage phasors are line-to-neutral voltages. For this strategy, the PLL is synchronized with the load voltage. As soon as a failure occurs, the PLL will be locked and so, the phase angle can be restored [22].The magnitude of DVR injected series voltage in this compensation method is not minimal and it depends on both amount of voltage drop and phase jump during the voltage sag because the phase jump of the grid voltage has also to be compensated by the DVR. Consequently, DVR has to be designed for the highest possible voltage sag compensation. Furthermore, voltage rating of dc link in DVR controlled with this method needs to be larger than one controlled with in-phase compensation method. Moreover, this compensation strategy leads to the lowest distortions at the load-side because both phase angle and magnitude of the voltage at the load-side are restored during the sag. Thus, the sensitive load doesn't sense any voltage disturbance. This method is so reliable and proper to protect sensitive loads without having any possible transient and circulating currents. Moreover, even if the phase jumps of the grid voltage in each phase are not the same, DVR controlled with pre-sag compensation method can eliminate the voltage disturbance completely. This strategy is able to compensate any kind of voltage sags including balanced or unbalanced voltage sags with or without any phase-variations in each phase of grid voltages.Regarding the amount of power exchanged between DVR and power grid, pre-sag compensation method injects both active and reactive power depends on magnitude of injected voltage, grid voltage phase jump and phase angle difference between load voltage and load current phasors. The reason for injecting active power is that the injected voltage phasor is not certainly perpendicular to the load current phasor in this method as like as in-phase compensation method. Consequently, it needs the active power to be supplied at dc link side otherwise this method can't compensate deep voltage sags for a long time. Thus, without supporting the active power at the dc link, dc link voltage will drop during the compensation and as a result, the maximum producible voltage of DVR will decrease and the modulation index of series converter will increase continuously and therefore, over-modulation may occur.The power rating of DVR controlled by pre-sag compensation method and the amount of the exchanged active power between DVR and power grid are as follows:

$$S_{DVR} = \sum_{k=a,b,c} \left[V'_{grid,k} \cdot I_{load} \right] \quad (1)$$

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$$P_{DVR} = P_{load} - P_{grid} = \begin{bmatrix} 3 \cdot V_{load} \cdot I_{load} \cdot \cos(\phi) \\ -\sum_{k=a,b,c} \left[V'_{grid,k} \cdot I_{load} \cdot \cos(\phi - \delta_k) \right] \end{bmatrix} \quad (2)$$

Where, δk is the phase jump in phase k. The magnitude of injected voltage is:

$$V'_{DVR,k} = \sqrt{2} \cdot \sqrt{(V_{load})^2 + (V'_{grid,k})^2 - 2 \cdot V_{load} \cdot V'_{grid,k} \cdot \cos(\delta_k)} \quad (3)$$

and the phase angle of injected voltage phasor is:

$$\angle V'_{DVR,k} = \arctan\left(\frac{V_{load} \cdot \sin(\varphi) - V'_{grid,k} \cdot \sin(\varphi - \delta_k)}{V_{load} \cdot \cos(\varphi) - V'_{grid,k} \cdot \cos(\varphi - \delta_k)} \right) \quad (4)$$

III. PROPOSED DVR BASED ON DFCM CONVERTER

Figure 3.3 illustrates general scheme of proposed DVR which is based on DFCM converter. The main advantage of the proposed DVR is that it has the capability of direct connection to medium-voltage power grid without any step-up line-frequency transformer which is bulky and heavy. This advantage is obtained thanks to utilization of DFCM converter as a core inverter of DVR to inject series

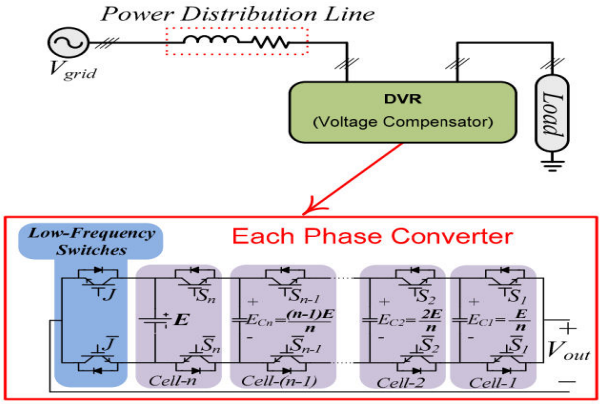

Figure 3 Proposed DVR based on DFCM converter for medium-voltage applications

IV. DVR REFERENCE VOLTAGE DETERMINATION

The control system of DVR has two main parts; the first one is voltage sag detection part and the second part of DVR control system is determining the reference of DVR series injected voltage. The approach to determine reference signal of DVR series injected voltage is based on the type of energy storage device and its ability to support active power. One of the methods for compensating voltage sags is restoring the load voltage to the level and condition before the sag, called pre-sag method [2],[18]. Therefore, the amplitude and the phase angle of the voltage before the sag have to be exactly restored. For this strategy, the PLL is synchronized with grid voltage and its phase angle is backed up and stored in memory continuously. As soon as a voltage sag is detected, the PLL will be locked to the phase angle stored in the memory and so, the phase angle can be restored [2], [18]. The magnitude of DVR injected series voltage in the pre-sag compensation method depends on both amount of voltage drop and phase jump during the voltage sag; because the phase jump of the grid voltage has also to be compensated by the DVR. In the synchronous reference frame (SRF)-based method, the first step of voltages to compensate voltage disturbances. Generally, FC voltages in FC-based converters are more diverse whenever the number of cells is high and so it is not more practical to have high number of cells. To negate this disadvantage, a topology called DFCM converter has been proposed in [33] wherein the number of FCs and power switches is half of those in the conventional topology of an FCM converter for generating the same stepped output voltage.Determining the reference of DVR series injected voltage is to measure the line-to-neutral grid voltages and transfer them from *abc* coordinate system to SRF as follows:

$$\begin{bmatrix} V_{grid,d} \\ V_{grid,q} \\ V_{grid,0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120) & \cos(\omega t + 120) \\ \sin(\omega t) & \sin(\omega t - 120) & \sin(\omega t + 120) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} V_{grid,a} \\ V_{grid,b} \\ V_{grid,c} \end{bmatrix} \quad (5)$$

where, Vgrid a , , Vgrid b , , Vgrid c , are the measured line-to neutral grid voltages of phases a, b

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and c, respectively and Vgrid d , , Vgrid q , , Vgrid,0 are the d-component, q-component and zero-component of grid voltages in the SRF, respectively. The phase angle of phase a voltage in pre-sag state (no-fault condition) is stored as the reference angle as follows:

$$\theta^{ref} = \arctan\left(\frac{V_{grid,d}|_{dc}}{V_{grid,q}|_{dc}}\right) \quad (6)$$

where, Vgrid,d$|_{dc}$ and Vgrid,q$|_{dc}$ are dc values of d- and q-components of grid voltages in SRF, respectively. After a voltage sag is detected using the proper detection method, the reference fundamental amplitude of line-to-neutral grid voltages (V_{g1}^{ref}) and the obtained reference angle (θ^{ref}) are used to determine the values of reference grid voltages in the SRF as follows:

$$V_{grid,d}^{ref} = V_{g1}^{ref} \cdot \sin\left(\theta^{ref}\right) \quad (7)$$

$$V_{grid,q}^{ref} = V_{g1}^{ref} \cdot \cos\left(\theta^{ref}\right) \quad (8)$$

Where,$V_{grid,d}^{ref}$ and$V_{grid,q}^{ref}$ are the reference d- and q components of grid voltages in the SRF, respectively. Next, the differences between the dq0 values of line-to-neutral grid voltages and the dq0 values of reference line-to-neutral grid voltages are taken into account as dq0 values of DVR reference injected voltages as follows:

$$V_{dvr,d}^{ref} = V_{grid,d}^{ref} - V_{grid,d} \quad (9)$$

$$V_{dvr,q}^{ref} = V_{grid,q}^{ref} - V_{grid,q} \quad (10)$$

$$V_{dvr,0}^{ref} = -V_{grid,0} \quad (11)$$

Where, $V_{dvr,d}^{ref}$, $V_{dvr,q}^{ref}$ and $V_{dvr,0}^{ref}$ are the reference dcomponent, q-component and zero-component of DVR series injected voltages in the SRF, respectively. These values are transferred to abc coordinate system and then, three single-phase reference voltages of DVR are obtained as follows:

$$\begin{bmatrix} V_{dvr,a}^{ref} \\ V_{dvr,b}^{ref} \\ V_{dvr,c}^{ref} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 1 \\ \cos(\omega t - 120) & \sin(\omega t - 120) & 1 \\ \cos(\omega t + 120) & \sin(\omega t + 120) & 1 \end{bmatrix} \cdot \begin{bmatrix} V_{dvr,d}^{ref} \\ V_{dvr,q}^{ref} \\ V_{dvr,0}^{ref} \end{bmatrix} \quad (12)$$

Where, $V_{dvr,a}^{ref}$, $V_{dvr,b}^{ref}$ and $V_{dvr,c}^{ref}$ are DVR reference injected voltages of phase a, b and phase c, respectively.

V.FIVE LEVEL INVERTER

A multilevel inverter is a power electronic converter built to synthesize a desired AC voltage from several levels of DC voltages which the DC levels were considered to be identical in that all of them were batteries, solar cells, capacitors, etc. The multilevel inverter has gained much attention in recent years due to its advantages in lower switching loss better electromagnetic compatibility, higher voltage capability, and lower harmonics [1]-[3]. Several topologies for multilevel inverters have been proposed; the most popular being the diode-clamped [4], [5], flying capacitor [6], and cascade H bridge [7] structures. Besides the three basic multilevel inverter topologies; other multilevel converter topologies have been proposed, most of these are hybrid circuits that are combinations of two of the basic multilevel topologies. The schemes of multilevel inverters are classified in to two types the multicarrier sub-harmonic pulse width modulation (MCSH PWM) and the multicarrier switching frequency optimal pulse width modulation (MC SFO PWM) [8], [9]. The MC-SH PWM cascaded multilevel inverter strategy reduced total harmonic distortion and the MC-SFO PWM cascade multilevel inverter strategy enhances the fundamental output voltage [10].The THD will be decreased by increasing the number of levels. It is obvious that an output voltage with low THD is desirable, but increasing the number of levels needs more hardware, also the control will be more complicated. It is a trade-off between price, weight, complexity and a very good output voltage with lower THD. Fig. 1 shows single phase topology of the diode

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Clamped, flying capacitor, a cascaded H-bridge, and cascade hybrid multilevel inverter that they have the number of switches, diodes, and capacitors as shown in table I (a 5- level multilevel inverter).

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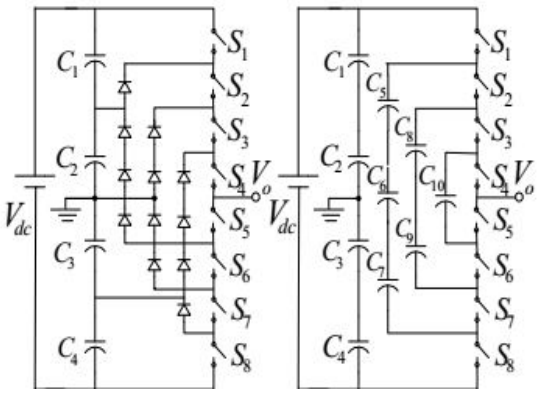
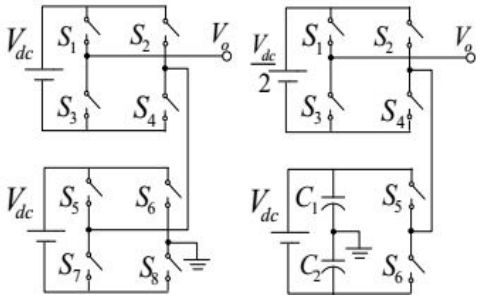


(a) Diode Clamped (b) Flying capacitor multilevel inverter multilevel inverter



(b) Cascaded H-bridge (d) Cascaded Hybrid multilevel inverter multilevel inverter

Fig.4 five-level multilevel inverter.

VI.MATLAB/SIMULINK RESULTS

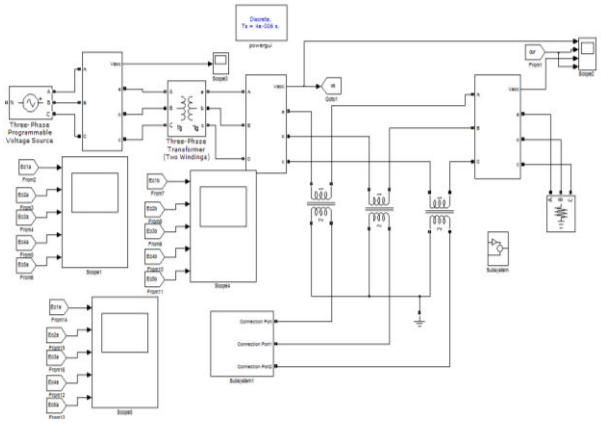


Fig6: Matlab/Simulink modelling of first case study performed for voltage sag mitigation using pre-sag compensation method

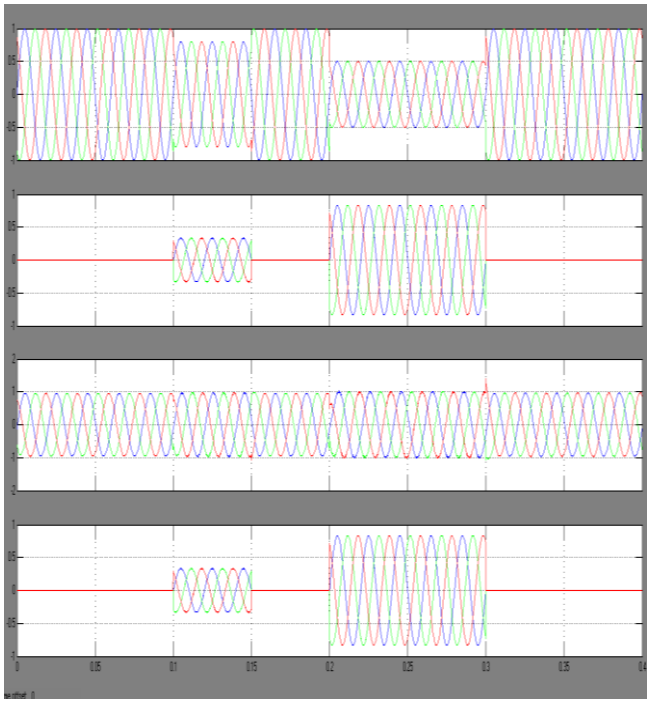


Fig 7: Simulation waveforms of first case study performed for voltage sag mitigation using pre-sag compensation method: (a) grid voltages; (b) DVR injected voltages; (c) sensitive load voltages; (d) DVR reference voltages in per unit.

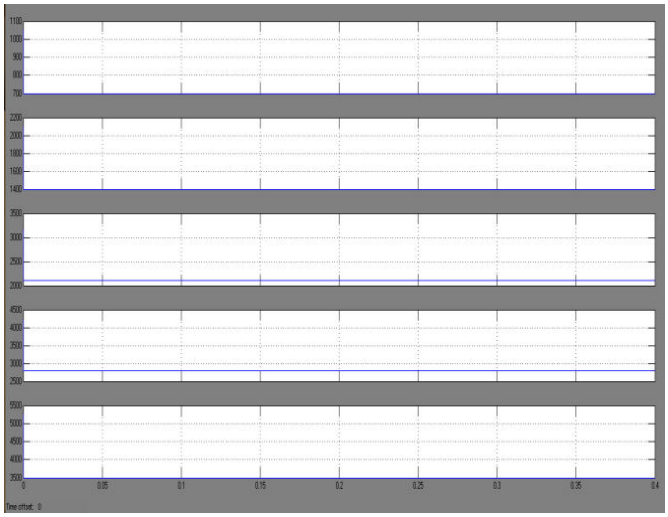


Fig 8. Simulation waveforms of the first case study performed for voltage sag mitigation using pre-sag compensation method: flying-capacitor voltages in phase a of the DFCM converter.

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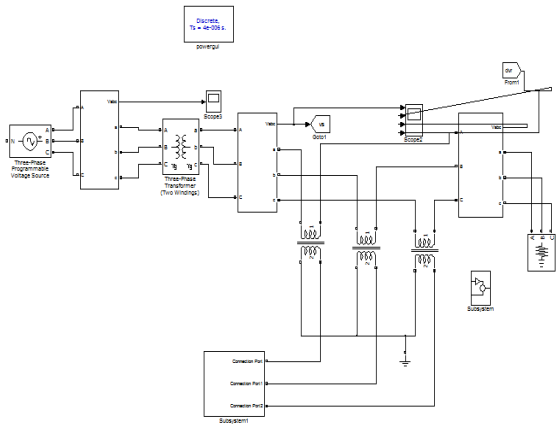

Fig 9 Simulink modelling of the second case study performed for voltage sag mitigation using pre-sag compensation method

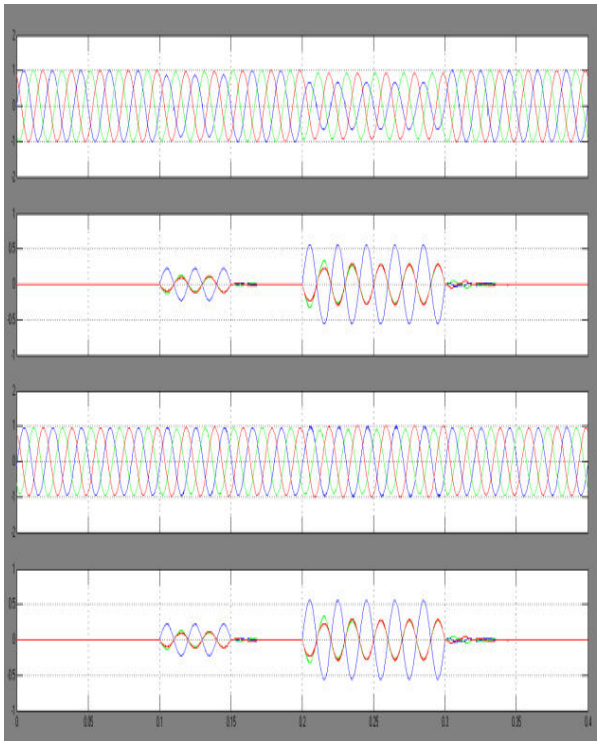

Fig 10. Simulation waveforms of the second case study performed for voltage sag mitigation using pre-sag compensation method: (a) grid voltages; (b) DVR injected voltages; (c) sensitive load voltages; (d) DVR reference voltages in per unit

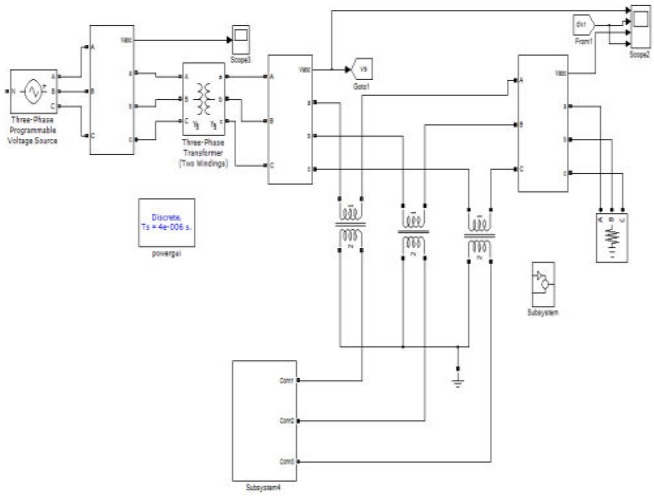

Fig 11 .Simulink modelling of DVR Based on Five Level MLI Converter

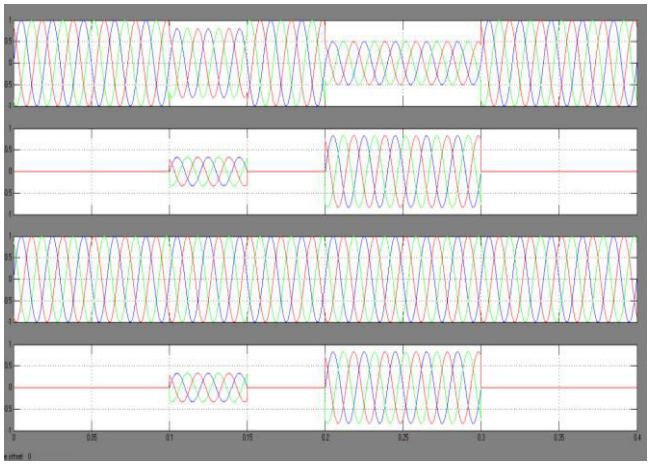

Fig 12. Simulation waveforms of the second case study performed for voltage sag mitigation using pre-sag compensation method: (a) grid voltages; (b) DVR injected voltages; (c) sensitive load voltages; (d) DVR reference voltages in per unit

VII. CONCLUSION

Power quality problems are one of the major concerns in present electric power grids. To suppress the power quality problems, DVRs are suitable devices to compensate these voltage disturbances, protect sensitive loads and restore their voltage during voltage sag. In this paper, a new topology of DVR suitable for medium-voltage applications is proposed. The proposed configuration of DVR is

based on DFCM converter whose dc link is fed from battery. The advantage of the proposed DVR is that it can connect to medium-voltage power grid without any line-frequency step-up isolation transformer which is bulky and costly. Furthermore, the procedure and method of pre-sag compensation is reviewed, investigated and discussed in detail. The amplitude of the injected voltage by DVR and amount of active power exchanged between DVR and power grid for pre-sag compensation method are analyzed. In addition, DVR reference voltage determination method is discussed in detail and the requisite equations to calculate the reference voltage are derived. Finally, the proposed topology is tested under different power quality problems. It has been shown that proposed DVR utilizing discussed DVR reference voltage determination method can compensate voltage sag effectively and protect the sensitive loads.

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